# DØ Layer 0 - innermost layer of Silicon Microstrip Tracker

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**Abstract**

A new single layer of silicon strip detector has been built and will be installed into the existing silicon microstrip tracker in DØ as the innermost layer. We report on the motivation, design, and performance of this new detector.

*Key words:* Silicon Microstrip Tracker, DØ, Radiation damage
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## 1 Introduction

The DØ has built single layer silicon strip detector named Layer 0 or L0. The construction finished in August 2005. The L0 will be installed inside the barrel part of the existing silicon microstrip tracker (SMT) [1] consisting of 4 super-layers of barrel, 12 central disk, and 4 forward disk detectors.

There are mainly three motivations to have L0. Because of its proximity to the beam interaction point, adding the L0 significantly improves impact parameter resolution, as shown in Fig. 1, resulting in better sensitivity to $\Delta M_S$ mixing measurement or higher efficiency for $b$-jet tagging. The addition of another layer also provides better pattern recognition, especially in high luminosity operation. We expect therefore the reduction of fake tracks. Finally the first layer of the SMT was expected to start to loose its functionality with the luminosity of 4-5 $fb^{-1}$ or $11 - 15 \times 10^{12}/cm^2$ 1 MeV neu-

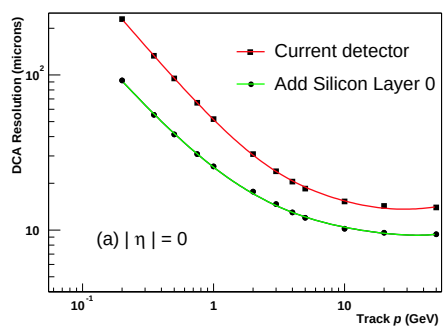


Fig. 1. The impact parameter resolution for the central track with and without L0 as a function of the momentum in Monte Carlo simulation. The data with the current detector is confirmed to be in agreement with the top curve.

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tron equivalent. Figure 2 shows the depletion voltage as a function of fluence measured at the Fermilab 8 GeV booster (proton beam) a few years ago. The SMT uses

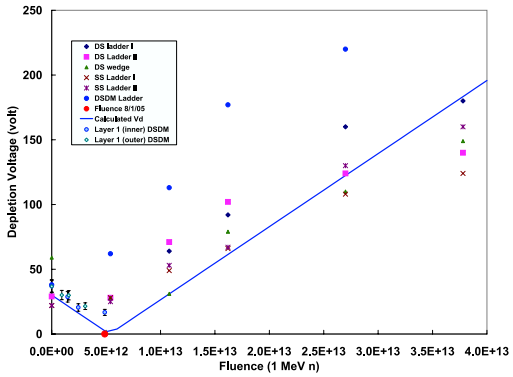


Fig. 2. The depletion voltage for various silicon sensor types as a function of fluence. The closed (open) circles show the result for the DSDM sensor used in the first layer of SMT obtained by the booster beam test (bias current scan in the actual detector). The blue line indicates the prediction by the Hamberg model.

various types of silicon sensor technology. Most of the silicon sensor behaves as predicted by the Hamberg model, however, the DSDM sensor used in the first layer shows abnormally high depletion voltage, limiting the lifetime because the coupling capacitor breaks down with the voltage between 150 and 200 V. The recovery of tracking capability from the possible loss of the first layer was another motivation for the L0. It turns out, however, that the actual sensors used at DØ do not show such abnormal depletion voltage [1], as also shown in Fig. 2. Therefore, the third motivation is now less relevant.

The idea behind L0 is to use R&D effort and human resources invested to Run 2b silicon upgrade project, which was canceled in 2003. For example, the rad hard single sided sensor, SVX4 readout chip developed for Run 2b, and so on are used in L0. These investments enable us to design and complete to build L0 within two years.

## 2 Design

As L0 must be installed into the existing detector, the space constraints are super severe. The inner radius is determined by the beam pipe ($r = 15$ mm), and the outer by the support of the existing detector ($r = 23$ mm). These constraints do not allow us to place the readout chip on the sensor because of the lack of space as well as not enough cooling. The choice for us is to use Kapton flex circuit as the analog cable to transmit tiny signal from the sensor directly mounted on the carbon fiber support structure to the readout chip mounted on a hybrid outside the fiducial region.

The L0 has 6-fold geometry with the inner layer at $r = 16.0$ mm and the outer layer at $r = 17.6$ mm, as shown in Fig. 3, covering 98.5% of acceptance. The readout pitch is

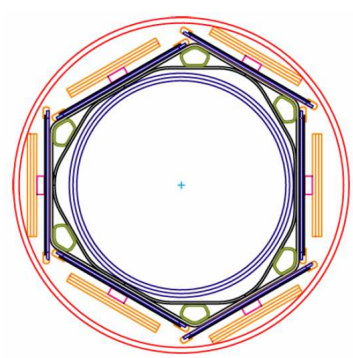

Fig. 3. The cross section of L0. The 6 planes near the beam pipe indicate the sensors, and the other 6 narrow plane indicate the analog cable.

71 $\mu$m for the inner and 81 $\mu$m for the outer

[1] The difference between the booster beam test and the measurement at DØ is the annealing time. We believe that there was not enough time for the sensors to release surface charge trapped at the beam test.

sensors. The number of readout strips are 256 for both types of sensors. For a given $\phi$ sector, there are four 7 cm long sensors covering the central part, and four 12 cm long sensors for forward parts (two for one end, the other two for another end) to equalize the occupancy, resulting in 48 sensors or modules in total. All the sensors are single sided and AC coupled sensors fabricated by Hamamatsu.

Each hybrid locates on the $\phi$ same as the corresponding sensor. Therefore four hybrids are aligned side by side for each end of the support. The resulting lengths of the analog cables are 20, 27, 34, and 36 cm, depending on the location of the module. The analog cable is fabricated by Dyconex. The pitch is 91 $\mu$m, and therefore we use a pair of analog cables for single module by stacking them with 45 $\mu$m offset. Because the analog cable is longer for the shorter sensor, the capacitive load is almost the same for all the types of modules with the typical value of 22 pF, half contribution from the sensor and another half from the analog cable.

We use SVX4 as the readout chip, which is a 0.25 $\mu$m technology silicon chip and the last SVX series developed by Fermilab and LBNL [2]. The SVX4 has 128 input channels, and ENC $= 300 + 41 \times C$ electrons, where $C$ is the load capacitance at 69 ns of the fixed preamp rise time [2], confirmed to be rad-hard up to 20Mrad. SVX4 can suppress any coherent noise by dynamic pedestal subtraction event by envent. A hybrid is based on BeO substrate, and holds two SVX4 to accommodate the readout from single sensor. The SVX4 needs 2.5V power with differential output signals, while SVX2 [3],which is used in SMT, needs 3.3V and 5V power with single ended signal. Since the SVX4 must be read out through the existing DAQ system, the additional card downstream of hybrid, named as adapter card, works as the interface to accommodate such difference above.

The use of analog cable brings us extreme difficulty to achieve low noise system, because it works as a good antenna, while we are dealing with $\sim$ 23000 electrons as signal. In addition, the impedance of carbon fiber for high frequency AC (53MHz readout in our case) turns out to be very small. There is no difference among carbon fiber, stainless steel, and aluminum. Therefore, the support structure has to be grounded, and the grounding scheme is the most important electrical issue.

All the studies indicate that the low inductance grounding connection to the SVX4 on hybrid has the most significant effect to reduce noise. For example, Fig. 4 shows noise for a module on the prototype support structure as a function of number of wires (order of cm long) connecting ground of the hybrid and the support. To achieve

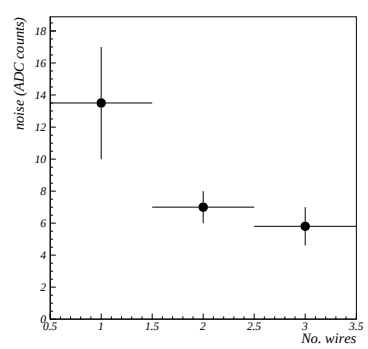


Fig. 4. The noise as a function of number of wires connecting the ground between the hybrid and the reference grounding plane. The vertical scale is arbitrary.

[2] The rise time will be much slower in the actual L0 operation where the bunch crossing is 396 ns. The Run 2b expected 132 ns of bunch spacing.

low inductance grounding connection, the hybrid has ground pads in backplane that is glued onto the copper rail on the Kapton flex circuit which is cocured together with the support structure. The ground of sensor is similarly connected to the support structure using Kapton flex circuit.

Another important result is the proximity of the analog cable to the grounded support structure. To avoid coupling of noise generated by the finite impedance of the structure, space under the analog cable has to be maintained and optimized, given the allowed space constraints. The layers of Kapton mesh are inserted, leading to 0.36 mm separation under the analog cable.

## 3 Performance

With the various tricks discussed above, L0 does not have any coherent pickup noise when L0's ground is tied together with the common detector ground, as shown in Fig. 5. The RMS of pedestal is less than

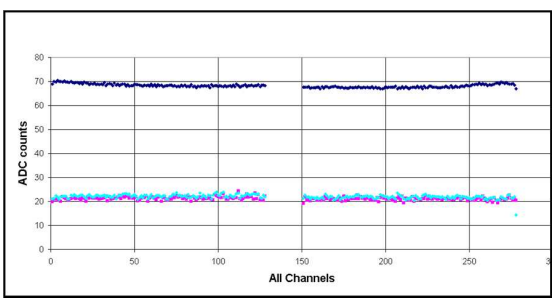


Fig. 5. The pedestal (dark circles), total noise ×10 (squares), and differential noise ×10 (diamonds) of a module in unit of ADC counts. The rise time is faster than the optimal.

2 ADC counts, when the testing is performed with the optimal rise time setting, while a MIP creates about 30 ADC count of signals which is verified by the cosmic ray testing.

Because L0 is read out from both ends of the detector, while the support structure is electrically uniform, grounding loop may exist in the DØ collision hall. In order to break such loop, L0's ground must be isolated from the common detector ground. This grounding scheme increases the sensitivity to external noise, especially for the noise pickup from the power lines of SVX4. A noise filter based on coils has been built for the power lines, and confirmed to eliminate coherent pickup noise.

After the construction, mechanical measurements have been conducted. The outer aperture has been measured to verify that L0 will fit into the desired space. The installation procedures have been tested using the mockup with multiple successes.

## 4 Conclusions

L0 has been designed to satisfy the tight space constraints with the special grounding efforts to establish low noise system. The mechanical specification was cleared. The system has been tested and demonstrated the low noise.

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