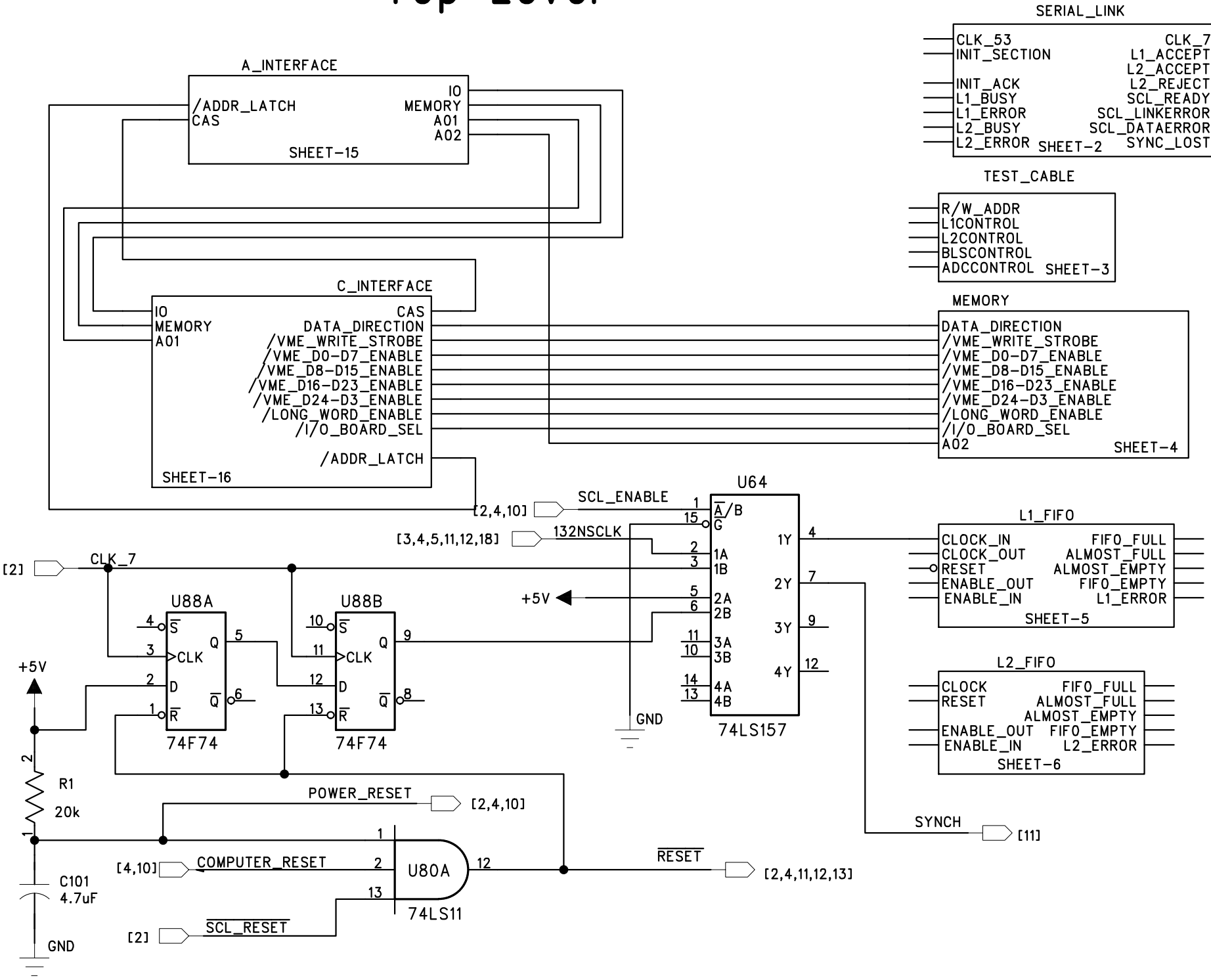
Top Level


SERIAL_LINK
CLK_53
INIT_SECTION
INIT_ACK
L1_BUSY
L1_ERROR
L2_BUSY
L2_ERROR
CLK_7
L1_ACCEPT
L2_ACCEPT
L2_REJECT
SCL_READY
SCL_LINKERROR
SCL_DATAERROR
SYNC_LOST
SHEET-2
A_INTERFACE
/ADDR_LATCH
CAS
IO
MEMORY
A01
A02
SHEET-15
TEST_CABLE
R/W_ADDR
L1CONTROL
L2CONTROL
BLSCONTROL
ADCCONTROL
SHEET-3
C_INTERFACE
IO
MEMORY
A01
CAS
DATA_DIRECTION
/VME_WRITE_STROBE
/VME_D0-D7_ENABLE
/VME_D8-D15_ENABLE
/VME_D16-D23_ENABLE
/VME_D24-D3_ENABLE
/LONG_WORD_ENABLE
/I/O_BOARD_SEL
/ADDR_LATCH
SHEET-16
MEMORY
DATA_DIRECTION
/VME_WRITE_STROBE
/VME_D0-D7_ENABLE
/VME_D8-D15_ENABLE
/VME_D16-D23_ENABLE
/VME_D24-D3_ENABLE
/LONG_WORD_ENABLE
/I/O_BOARD_SEL
A02
SHEET-4
[2,4,10]
SCL_ENABLE
[3,4,5,11,12,18]
132NSCLK
U64
A/B
G
1A
1B
2A
2B
3A
3B
4A
4B
1Y
2Y
3Y
4Y
74LS157
GND
+5V
[2]
CLK_7
U88A
S
CLK
D
R
Q
74F74
U88B
S
CLK
D
R
Q
74F74
L1_FIFO
CLOCK_IN
CLOCK_OUT
RESET
ENABLE_OUT
ENABLE_IN
FIFO_FULL
ALMOST_FULL
ALMOST_EMPTY
FIFO_EMPTY
L1_ERROR
SHEET-5
L2_FIFO
CLOCK
RESET
ENABLE_OUT
ENABLE_IN
FIFO_FULL
ALMOST_FULL
ALMOST_EMPTY
FIFO_EMPTY
L2_ERROR
SHEET-6
SYNCH
[11]
+5V
R1
20k
POWER_RESET
[2,4,10]
[4,10]
COMPUTER_RESET
U80A
74LS11
RESET
[2,4,11,12,13]
C101
4.7uF
GND
[2]
SCL_RESET