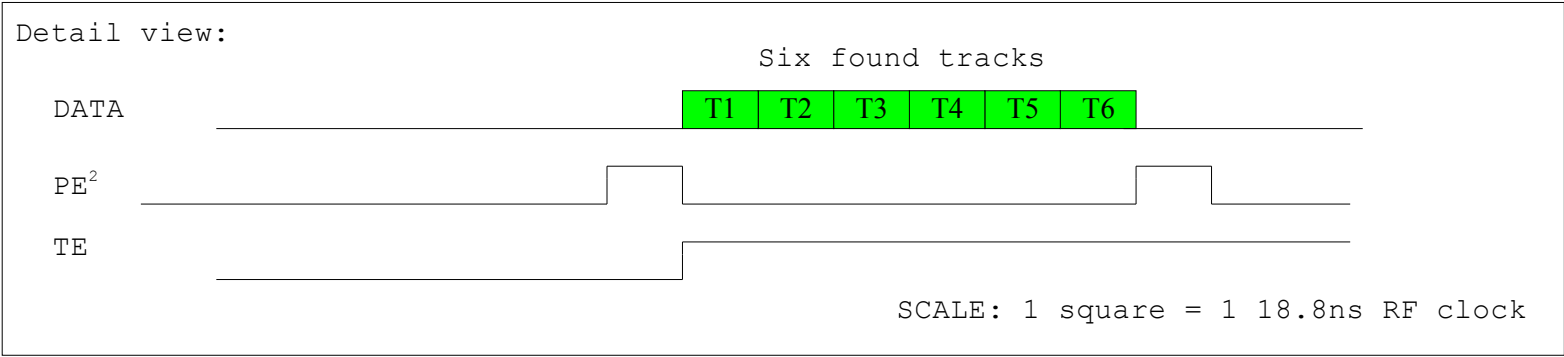
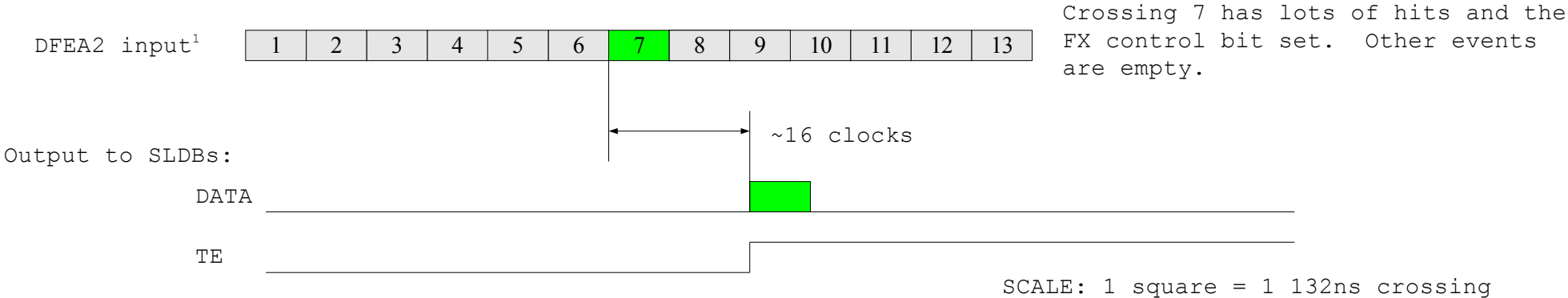
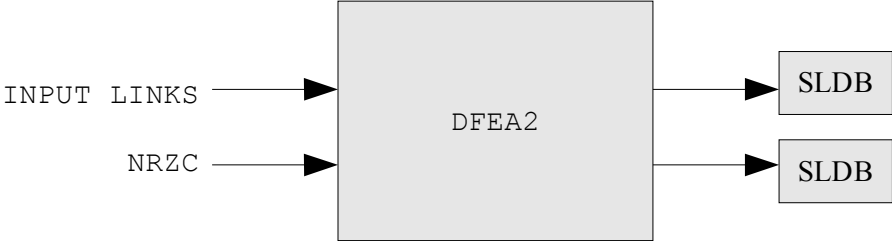


Simulating L1muon Outputs

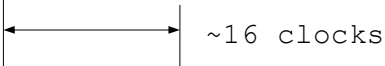
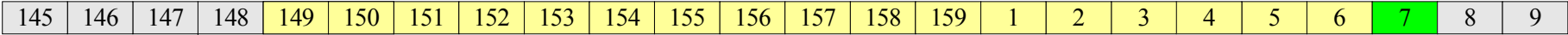


1. As measured at the front FPGA inputs
 2. PE is always asserted on the last timeslice.

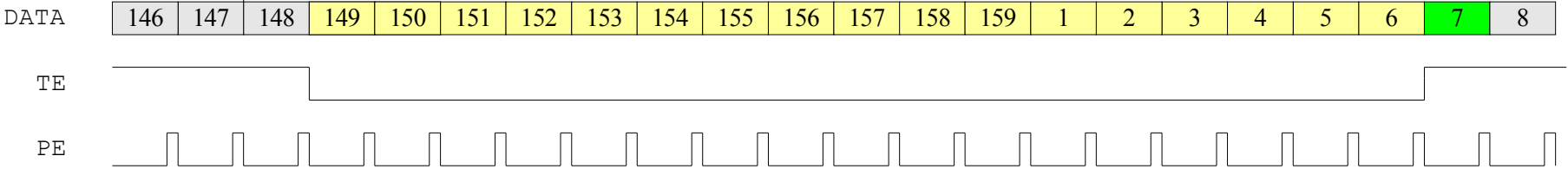
Simulating L1muon Outputs: the SYNC GAP

The transmit enable (TE) signal is a delayed and inverted copy of the sync gap.

DFEA2 input



Output to SLDBs:

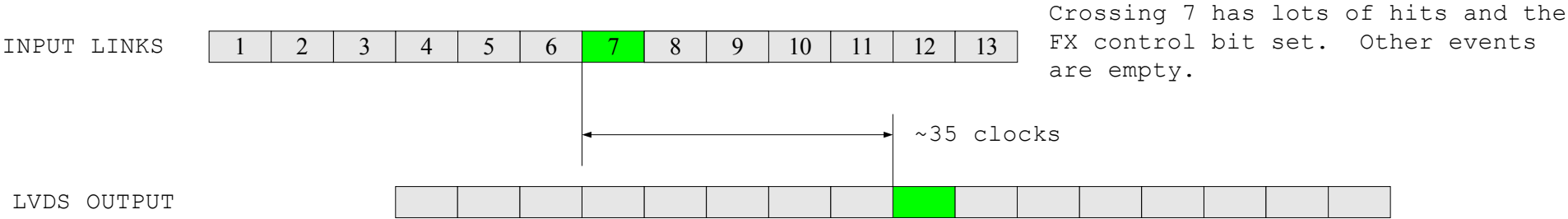


- L1 crossing
- L1 crossing with SG bit asserted
- L1 crossing with FX bit asserted

SCALE: 1 square = 1 132ns crossing

159 crossings per turn; SyncGap is 17 crossings 149-6 inclusive.

Simulating L1 output to CTOC



Crossing 7 has lots of hits and the FX control bit set. Other events are empty.

SCALE: 1 square = 1 132ns crossing

This output record should have lots of track counts set, the occupancy count should be non-zero and the FX control bits should be set. Adjacent records should be empty (just headers and parity words).