D0 Status Report

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All Experimenters' Meeting
25 September 2006

Data Taking

Day	Delivered Lum (pb^{-1})	Recorded Lum (pb^{-1})	Efficiency (%)	Comment
18 Sep	2.70	2.44	91	
19 Sep	6.28	5.89	94	Record daily delivered and recorded Luminosity. Muon trigger problems
20 Sep	4.78	4.24	89	Record D0 initial Luminosity, 222E30 Controlled Access for CAL and CFT
21 Sep	2.57	2.22	86	Problems with VLPC cryostats between stores. Short downtime for SMT HV and L2.
22 Sep	4.51	3.82	85	Loss of pond water leads to cooling problems. PDT trips due to high Humidity
23 Sep	3.74	3.23	87	Continued PDT problems. AFE PS disables two AFE boards for six hours
24 Sep	4.23	3.67	87	1/6th of SMT out due to PS failure. Two hours down for MUO/L2 readout.

18-24 Sep	28.8	25.5	89	3rd best weekly recorded Luminosity

VLPC Cryostat

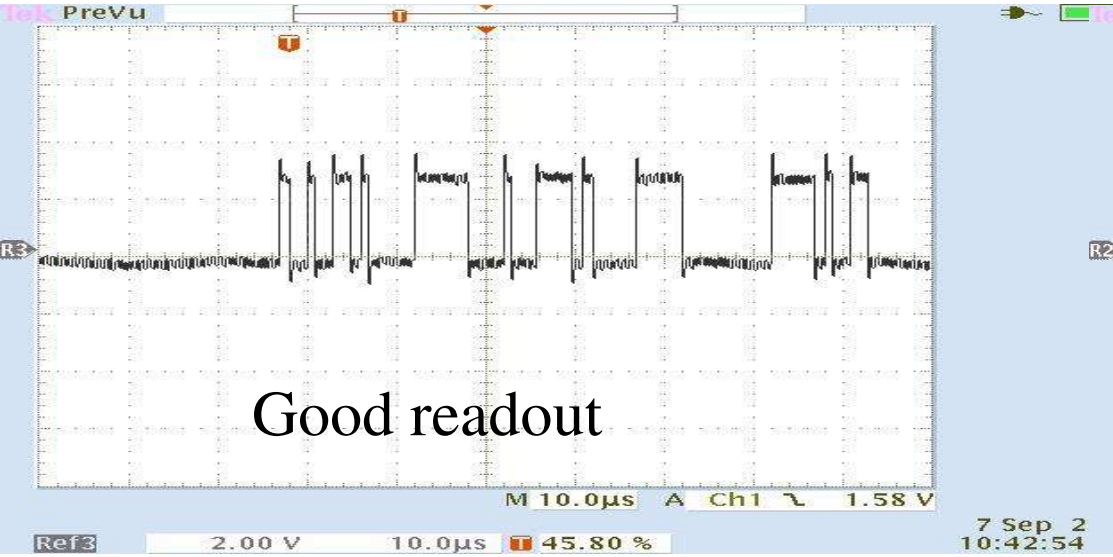
- There were temperature problems with the CFT west Cryostat leading to high helium flow.
  - No leaks were noticed on controlled access.
  - Several techniques were used in an attempt to control and understand the high flow rate.
  - It was noticed that the nitrogen intercept had too high temp.
    - The flow rates for the intercept indicated a possible blockage.
    - This was then warmed to 195 K.
  - Upon cool down, the cryostat was back to normal.
- No data lost or compromised due to this issue.

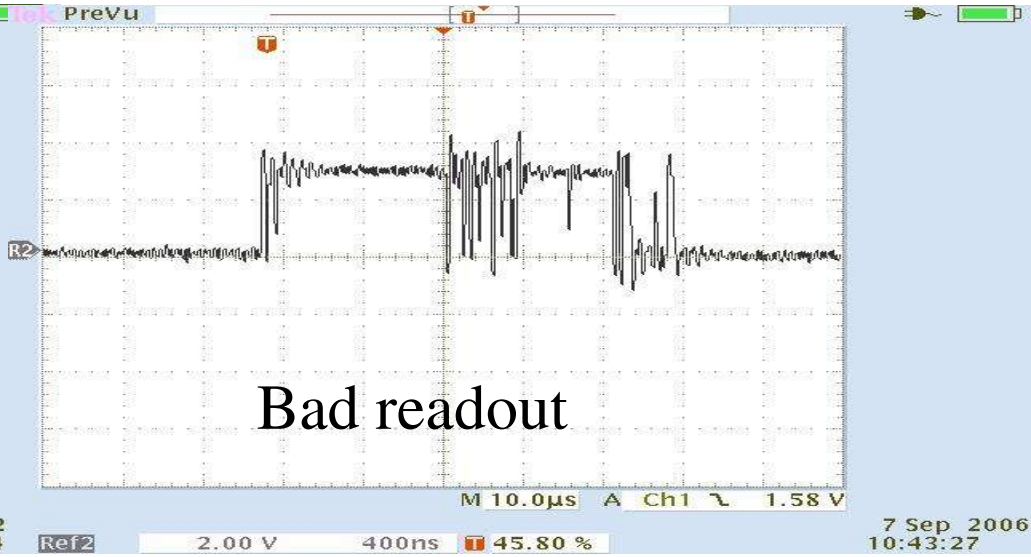
Access Request

- The 30 August trigger framework (TF) trip lead to high currents in Silicon HDIs. These currents are kept low by reading out the detector. When the TF failed, the heartbeat that reads out the Silicon could not function. This Lead to 40 HDIs with readout errors such that they can only partially be read out.
  - A study of the HDI's removed during the shutdown has shown that these 40 HDI's and potentially other disabled HDI's may be recoverable.
    - A 12 hour access will be needed for this investigation.
- D0 currently has 60 disabled HDIs and 40 that can only be partially be read out. There are 432 barrel HDIs.

Possible HDI Recovery

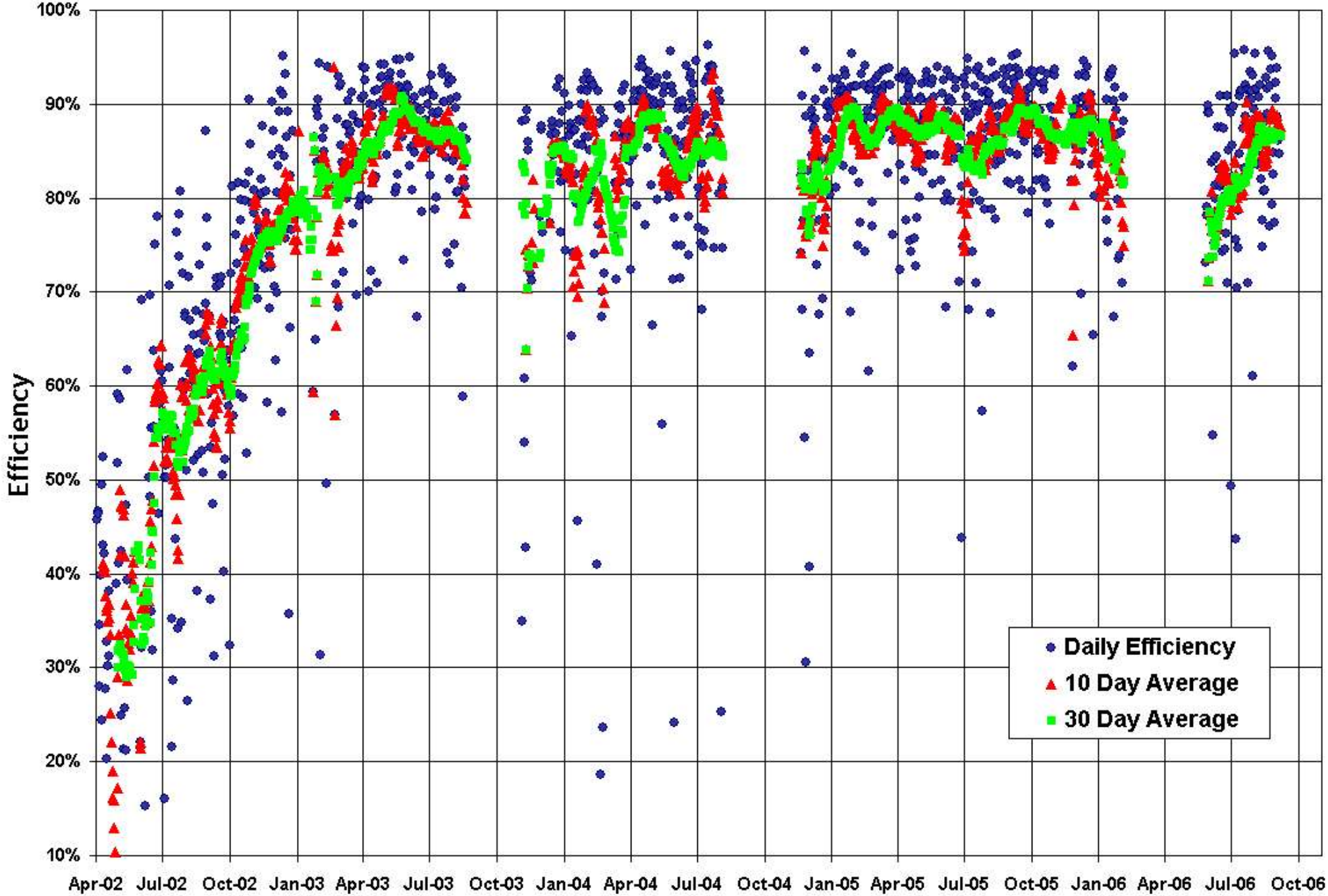
- All SVX2 chips on an HDI are serially connected with a priority passing line. The last chip is connected to the interface board (IB) and then to the sequencer
  - Tests show the drive transistor is possibly too small or IB signal comparator needs adjustment.
  - and a shift in either the drive transistor or comparator could cause loss of data or loss of end of read out signal.
  - Need to look at the raw chip signals to test this.

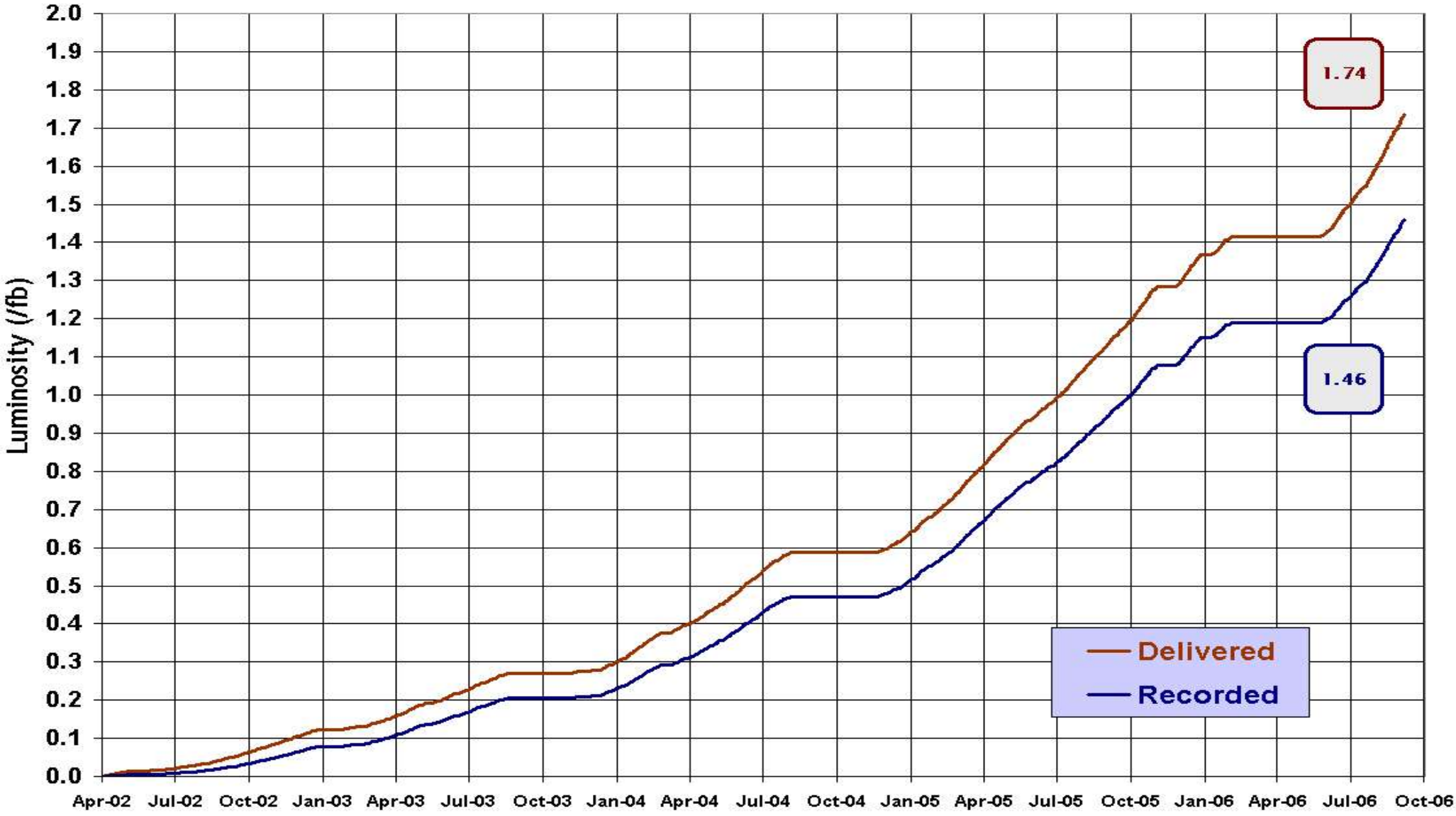




Daily Data Taking Efficiency

19 April 2002 - 24 September 2006





On Friday, 29 September, D0 will update its luminosity constant.
There will be a detailed report at the AEM in two weeks.