

PROGRESS ON ADF BOARD DESIGN

Denis Calvet
calvet@hep.saclay.cea.fr

CEA Saclay, 91191 Gif-sur-Yvette CEDEX, France

Saclay, 16 May 2002

D0 L1 Calorimeter Trigger upgrade Run IIb

PLAN

ANALOG SPLITTER

ADF BOARD AND CRATES

DIGITAL FILTER

SCL INTERFACE

INTERFACE WITH TAB

FUTURE WORK

ANALOG SPLITTER

PURPOSE

Duplicate the analog signal of some towers to connect the current CTFE's and a prototype ADF card non intrusively

Passive splitter: send EM+ to CTFE and EM- to ADF

Pro: simple

Con: divide by 2 the amplitude measured, unipolar signals

Active splitter: duplicate the differential signals

Pro: transparent, test ADF card with realistic differential input

Con: more complex

Choice: **Active splitter**

DESIGN AND SPICE SIMULATION COMPLETED

1 fully diff. amplifier of gain $-\sqrt{2}$ driving in parallel 2 fully diff. stages of gain $-\sqrt{2}$

Need 0->6V in output but only +-5V in CTFE crate: make +-12V with DC/DC converter

STATUS

Ready to start schematic capture, PCB design, get components...

8 channels (i.e. 4 trigger towers) per splitter

ADF BOARDS AND CRATES

CRATE AND BACKPLANE

Goal is to accomodate 32 channels on a 6U card

CTFE cables are stiff and heavy: robustness is needed

There will be ~340 cables per crate: **need good mechanics**

OPTIONS 1

6U ADF cards with full height 6U rear transition cards

Custom or standard backplane on P2

Candidate crate: Wiener 6023 Plenum bin (9U height)

Pros: all I/O at rear of the crate; standard mechanics

Cons: adds 80 cards, tortuous cabling, expensive crate

OPTIONS 2

6U ADF cards without rear transition cards: front panel I/O

Standard 3 (or 5) rows VME backplane - Bussed signals on P2

Pros: common VME crate, inexpensive

Cons: lack of robustness, bending or twisting cables, hard to replace one card

ADF BOARDS AND CRATES (CON'T)

OPTIONS 3

6U ADF cards with rear-side I/O using a custom transition backplane on P2

Pros: all I/O at rear of the crate, only 4 backplanes to make (instead of 80 cards), short PCB stubs

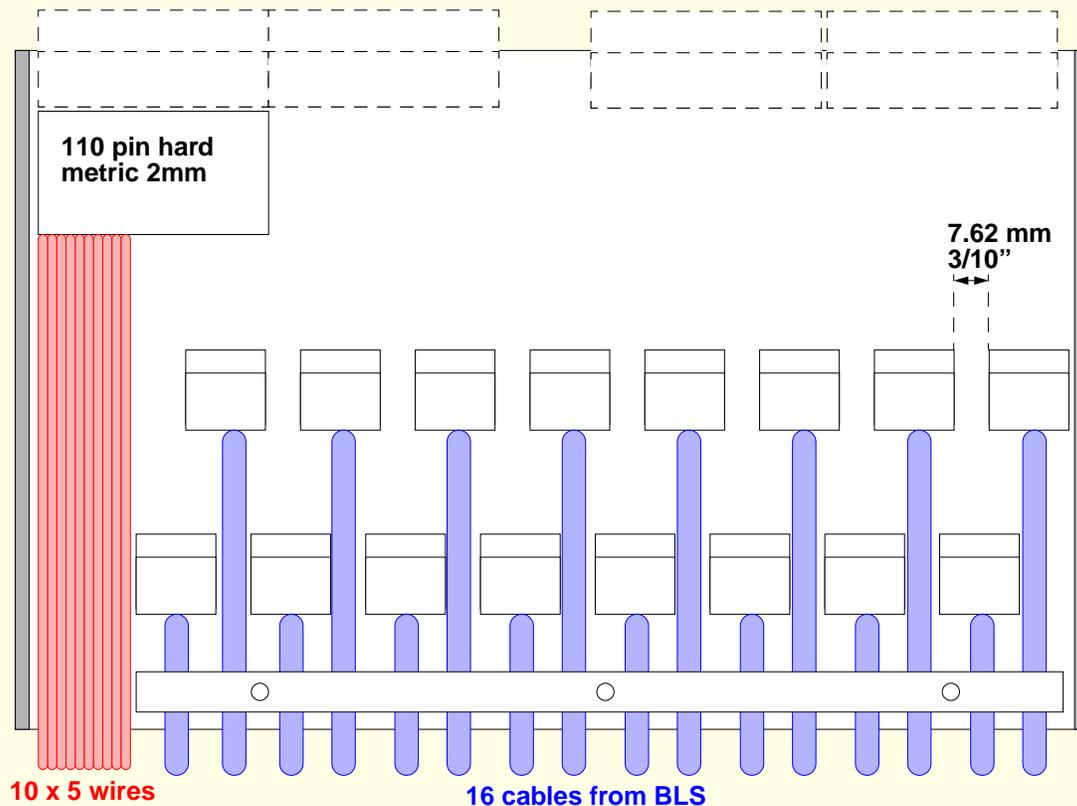
Cons: some mechanical issues to solve: protrudes at the bottom of the crate; hard to fit connectors on both sides because of overlap...

OPTION PURSUED AT PRESENT: OPTION 3

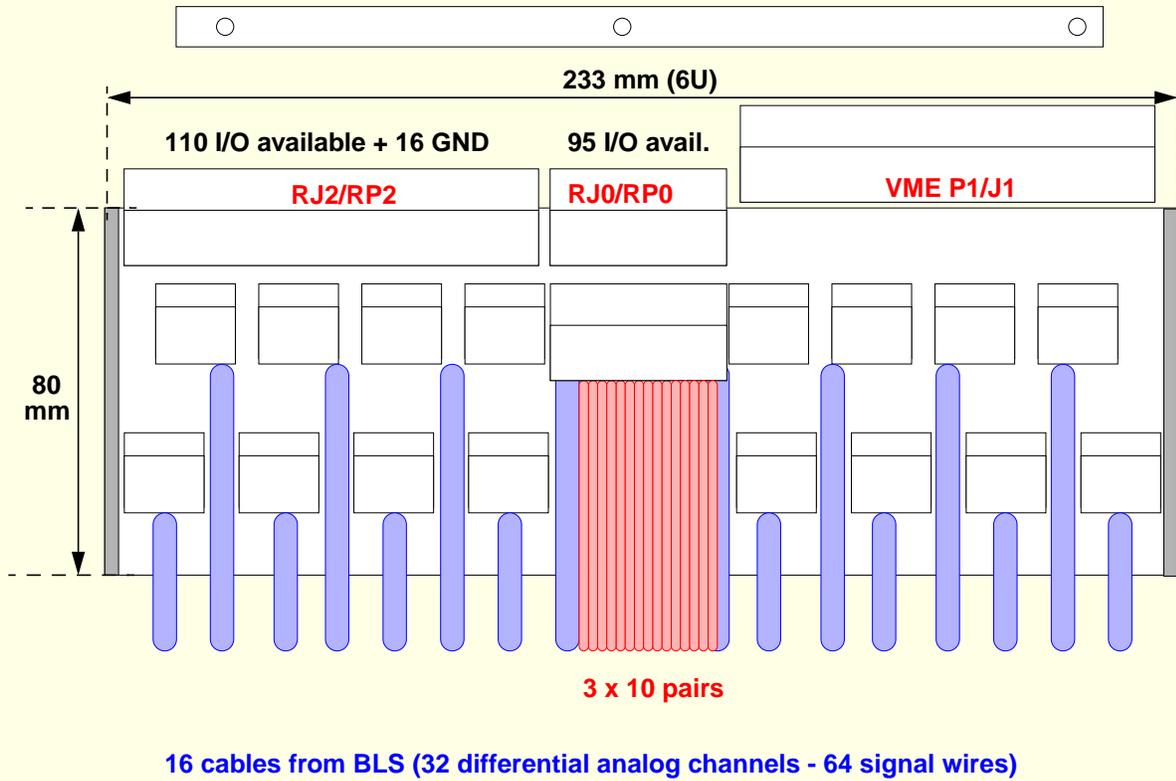
Standard VME 64x (5 row connectors) backplane

- geographical addressing
- 3.3 V power supply
- unused bussed signals on P1
- rear side J0 to directly connect 2 hard metric 2 mm cables (to TAB)
- use 64 J2 pins for analog input of 32 channels
- use other J2 available pins for GND shield (and a few bussed signals?)

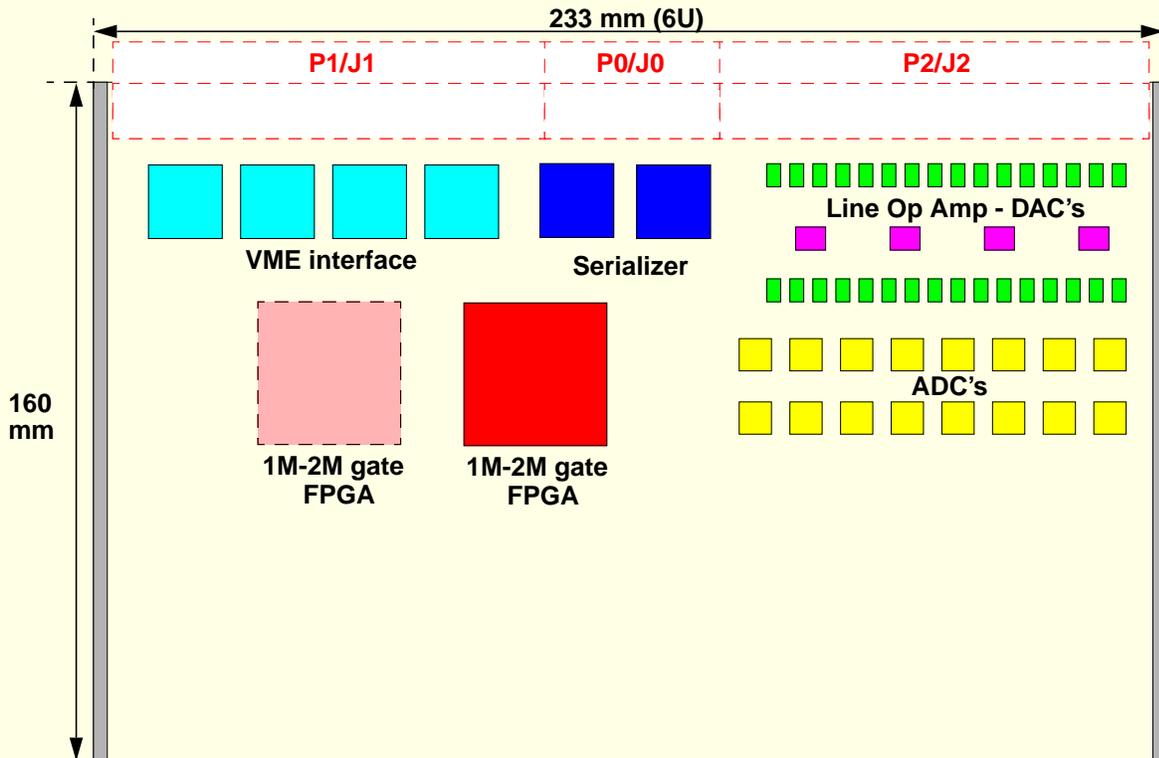
REAR SIDE I/O TRANSITION CARD

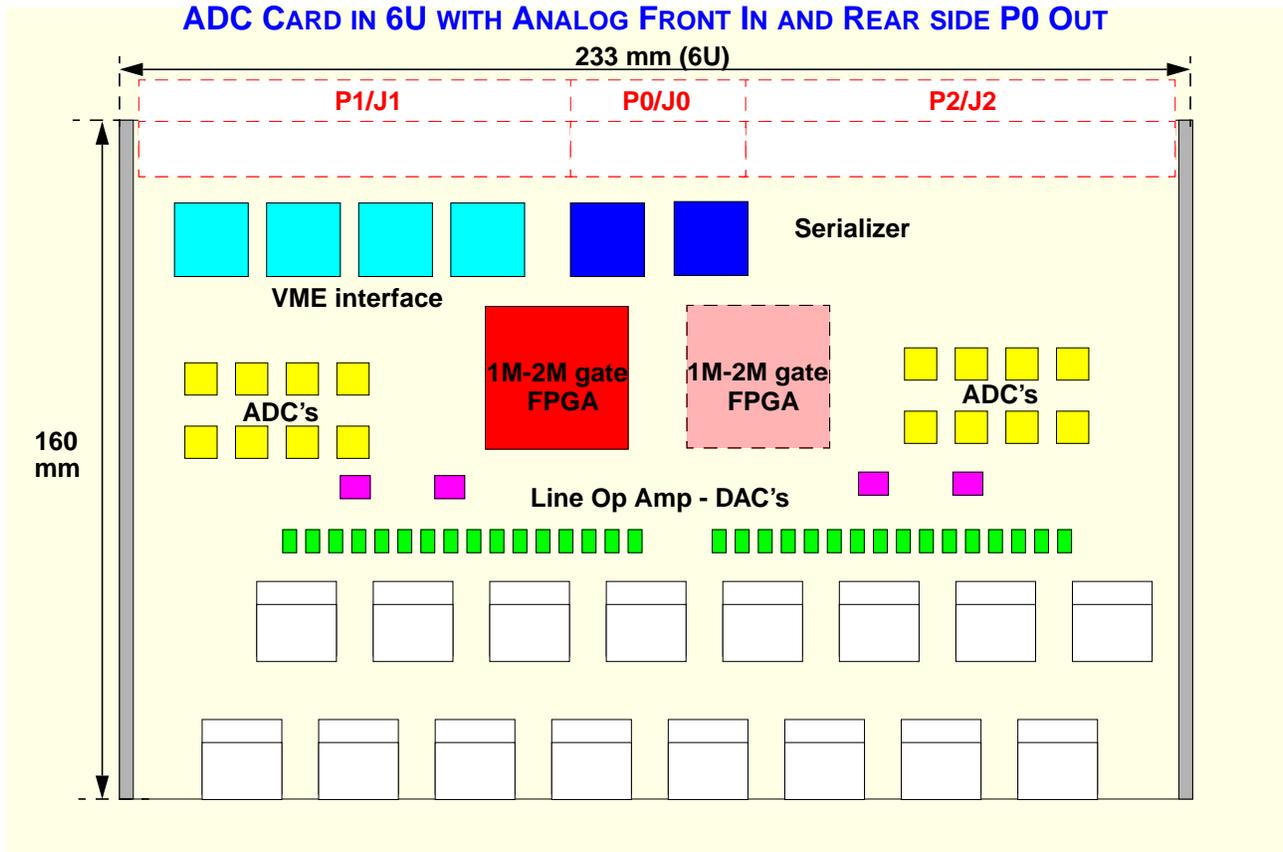
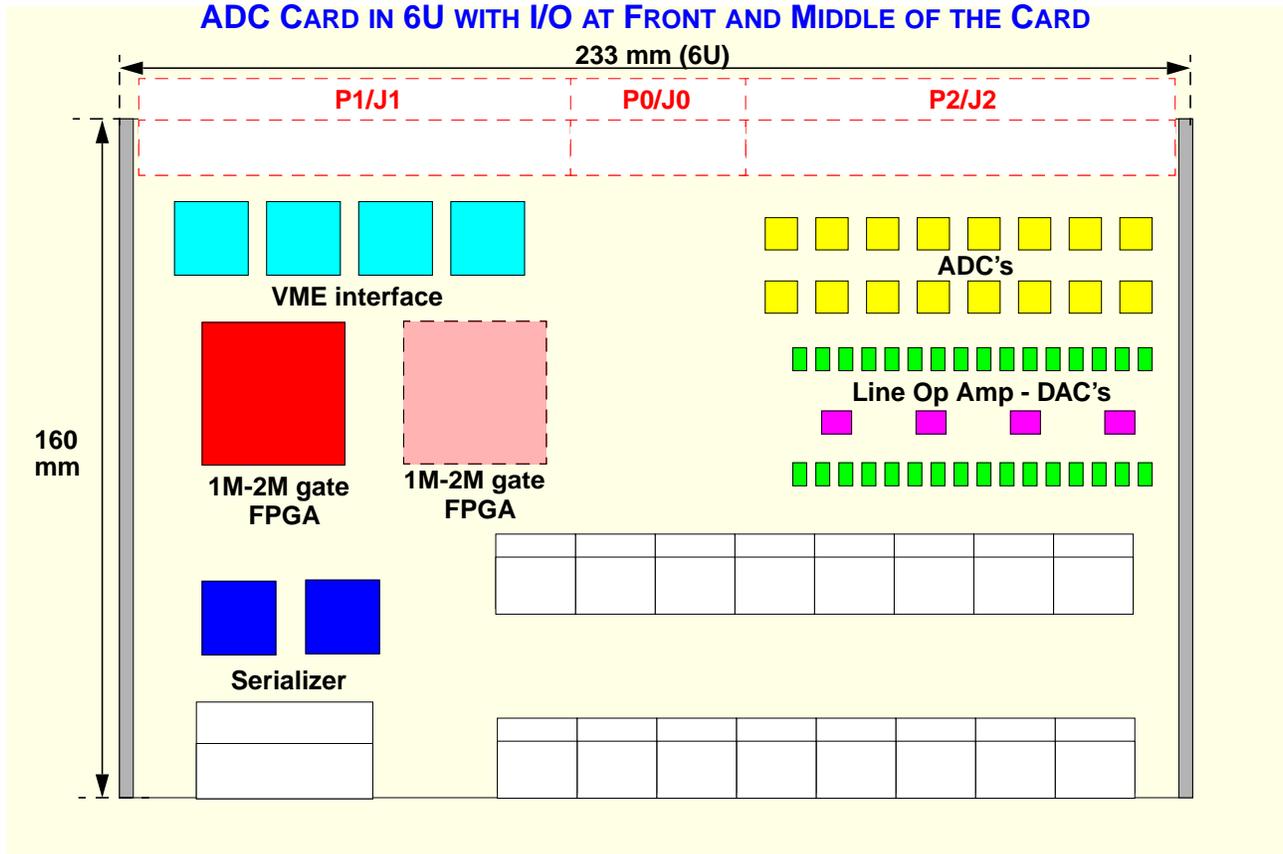


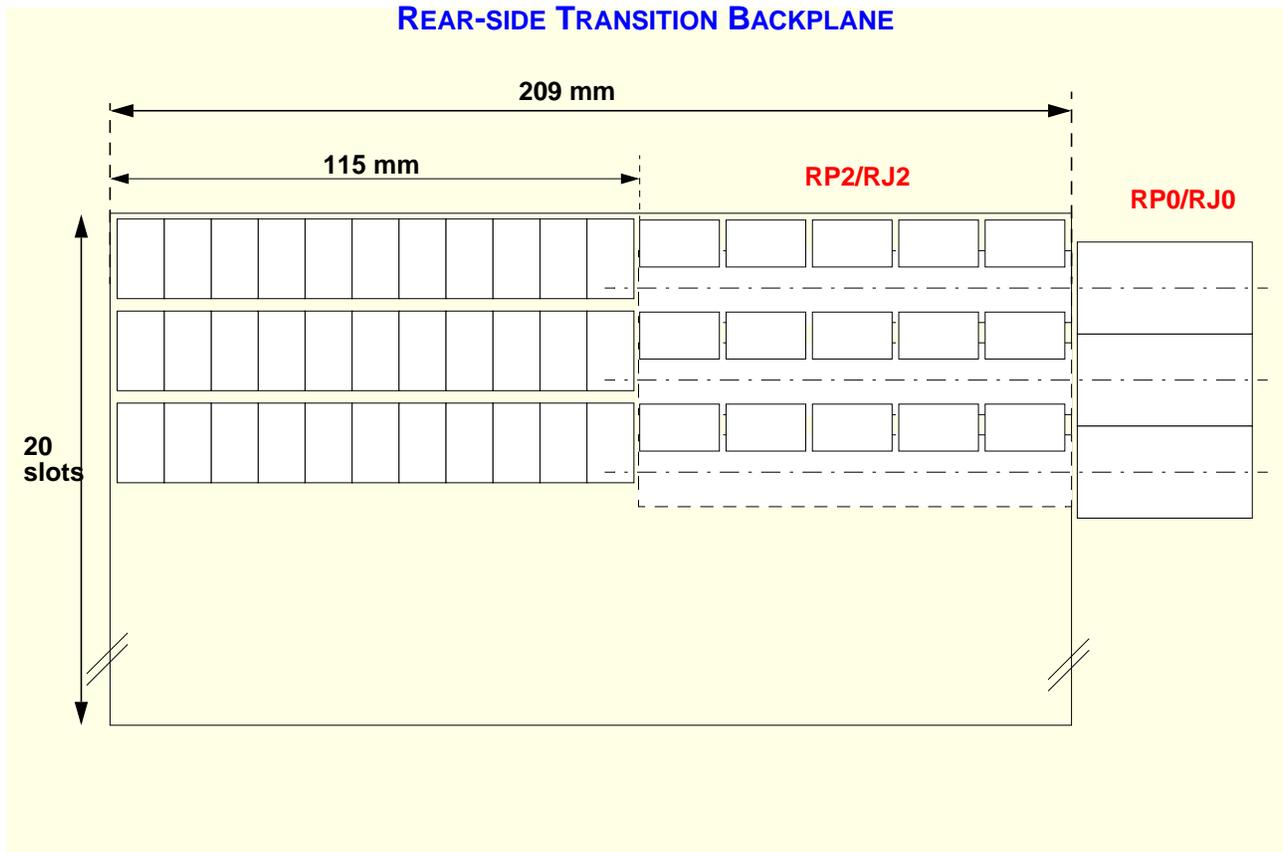
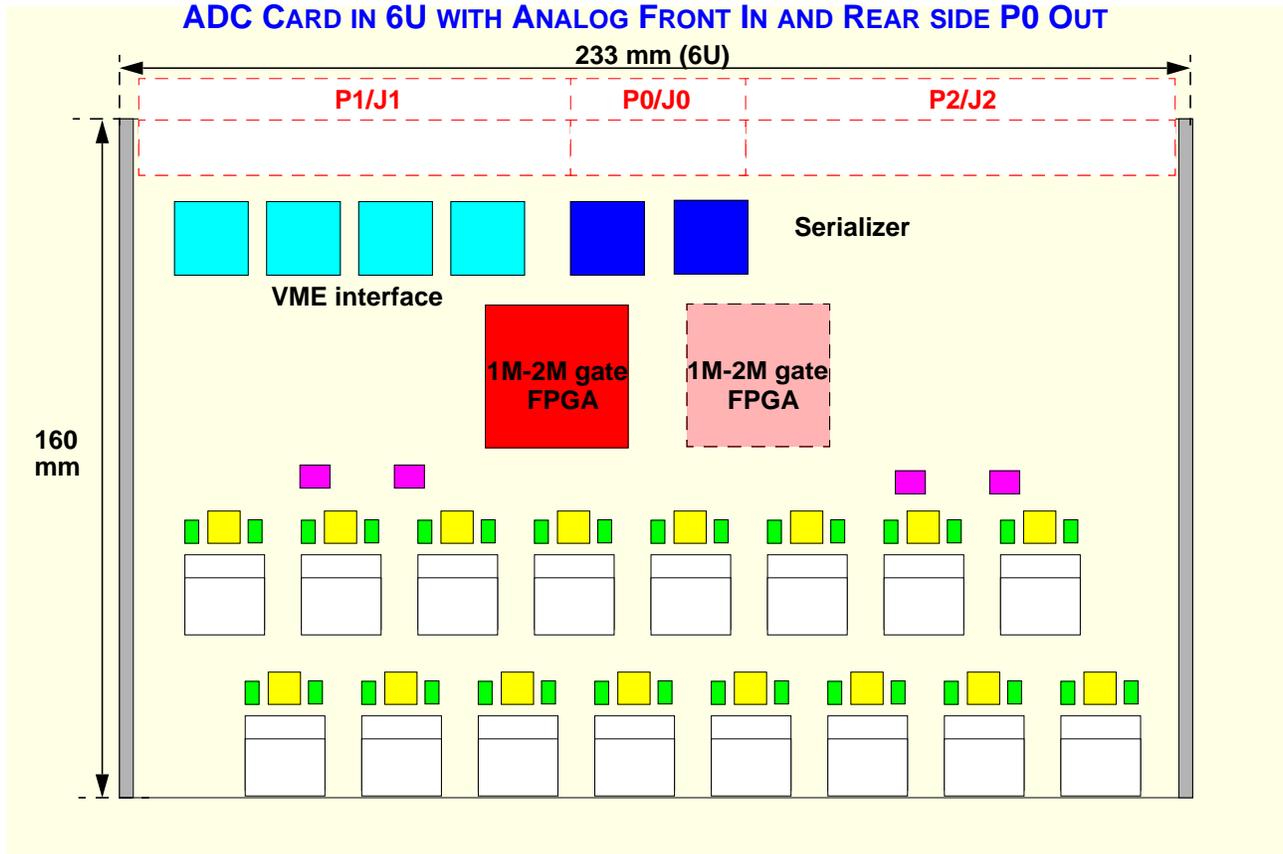
IEEE P1101.11 REAR SIDE I/O TRANSITION CARD



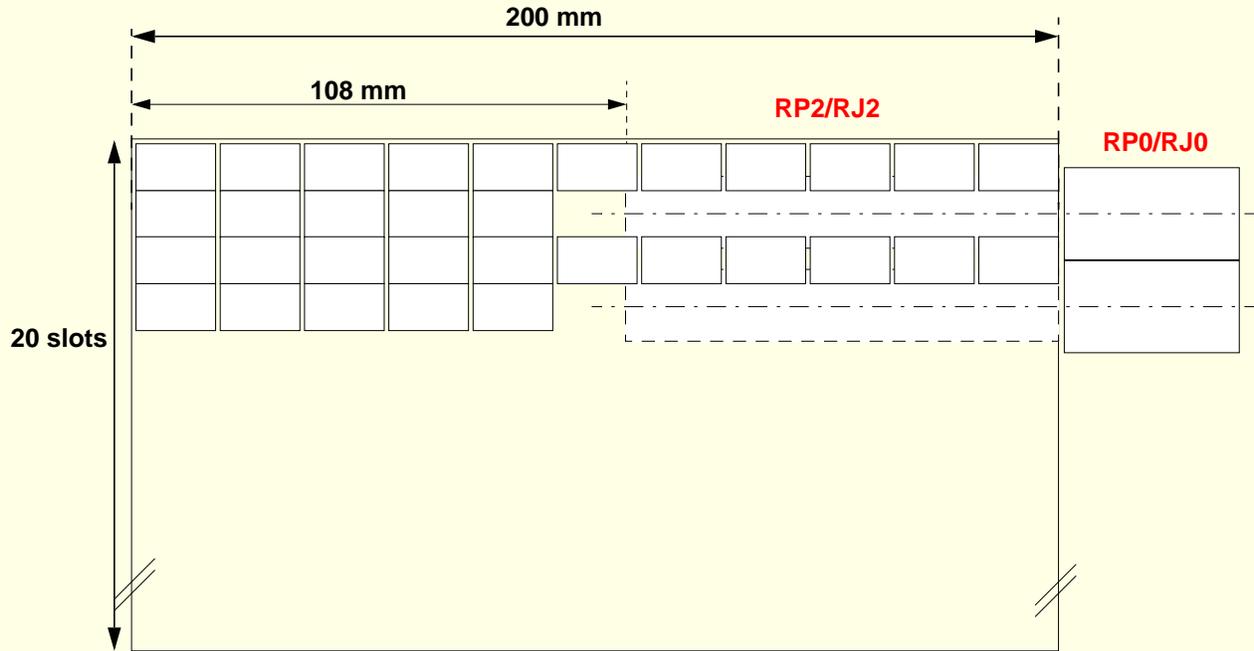
ADC CARD IN 6U WITH REAR-SIDE I/O



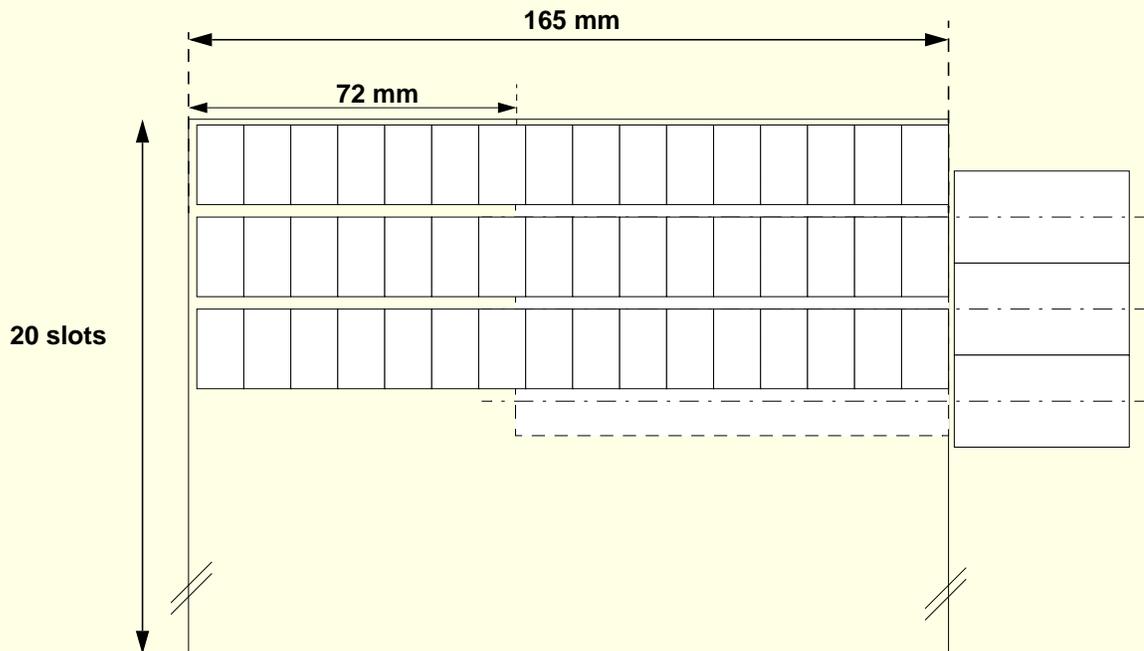




REAR-SIDE TRANSITION BACKPLANE (2)



REAR-SIDE TRANSITION BACKPLANE (3)



DIGITAL FILTER

ALGORITHM

Matched filter at BC x 2 followed by 3 point peak detector and final Et Look-up-Table

10 bit ADC; sampling rate: BC x 4 (~30 MHz)

Up to 8 tap filter - 6-8 bit unsigned coefficients, programmable coefficients

TEST AND DEBUGGING

Turn on/off peak detector

Load internal memory with raw samples, play, stop and read back

ADF to TAB link driven by: constant value, or Et result or pseudo-random gen.

CALIBRATION AND MONITORING

Record all raw samples, filter output and Et during L1 latency

Freeze buffer upon L1 or monitoring request

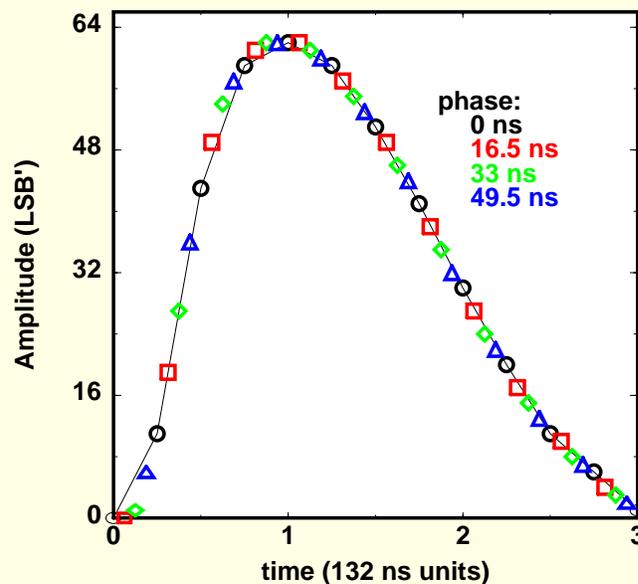
Optionally send the raw data that caused a L1 via ADF to TAB links

Data acquisition mode with self trigger when Et > programmable threshold

Per channel latency adjustment

Eventually, programmable channel swap before serializer driving TAB link, etc.

PER CHANNEL PHASE ADJUSTMENT



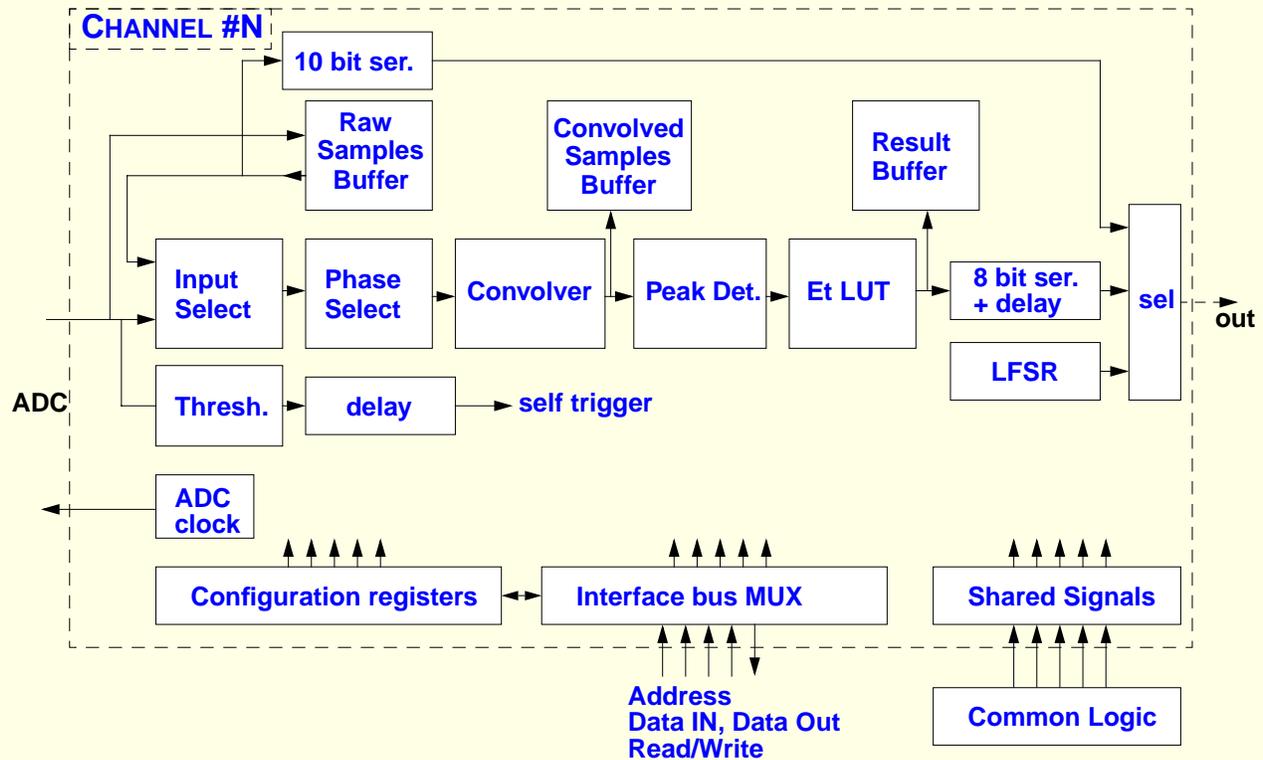
ADC Sampling

- Sampling at BC x 4 and processing at BC x 2

- Per channel ADC clock inversion

-> phase ajustement of 0 ns; 16.5 ns; 33 ns; 49.5 ns

CHANNEL FUNCTIONAL DIAGRAM



STATUS ON FPGA AND FIRMWARE

VHDL CODING

Most of the logic for one channel coded and simulated

Need to add the bus interface and few other things

Goal is to run all the logic at $BC \times 8$ (i.e. 60 MHz)

Current latency is $\sim 5 BC + 1.25$ for ADC + 1 for cable + 1 to TAB = $\sim 8-9 BCs$

FPGA TARGET

Need (dual-port) memories, fast multiply-accumulate -> Virtex II family

Convolver with 1 multiplier: need to run MAC at 121 MHz for 8 tap filter:

~ 100 MHz achieved after synthesis -> could do 5-6 tap only

-> change design and use now a parallel filter with 2 multipliers

Not enough pins/memory blocks for 32 channels in 1M gate device

-> 4 devices 250k gate offer a good number of RAMs, Multipliers and IO pins

-> alternative: 2 devices 1 M gate or 1 device 3 M gate

SCL INTERFACE

TIMING CARD

Can be shared with TAB

Timing signals needed to make more than the basic tests of ADF card

If timing card included in the GAB: test of the ADF dependant on the GAB

-> do not share timing with TABs and make SCL interface for the ADF?

- try to make this board simple, no need for slow control
- acts as a relay to distribute global signals
- need to include digital delay lines for global synchronization?

GLOBAL SIGNALS PROPOSED FOR THE ADF CARDS

BC clock, L1 Accept, L1 Qualifier (freezes buffers when L1 accept for monitoring)

Reset, Busy/error

Suspend/Resume

Monitoring trigger or self trigger

- > can use 10 pair 2 mm cable similar to ADF -> TAB cable and plug it directly on RJ0 in each ADF crate

ADF TO TAB LINKS

CABLE AND CHIPSET

National Semiconductor Channel link 48 bit chipset

10 pair 2 mm HM cable from AMP?

Any gain to use 8 pairs?

PROTOCOL

32 bit streams for data

1 bit lane for framing (8 bit frames and 10 bit frames will be mixed)?

1 bit lane to indicate if 8 bit or 10 bit frames are sent?

Parity?

Some counter (BC or L1A...) to detect loose of synchronization?

PLANS

Analog Splitter

Design PCB, get components and assemble cards

-> try to be ready by September to connect splitters at D0 during shutdown

Crates

Almost finalized: 6U VME 64x 5 rows connectors + custom rear-side transition backplane

-> solve remaining issues; purchase crate + Bit3 PCI/VME interface; make backplane

ADF board

Start board schematic and layout as soon as FPGA target is known

-> need also to address download bootstrap interface, and power supply circuits

FPGA firmware

Complete design and simulation of one channel and fit 8-16-32 channels in FPGA

-> work in progress

To be thought: SCL timing card; Software: monitoring, download, calibration...