
Universe IIB / IID
Device Errata and Design Notes



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Product: Universe IIB / IID (CA91C142X)
Title: Universe IIB/ IID Device Errata and Design Notes
Document: 8091142_ER001_07
Status: Revision 7.0
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Introduction

This document describes the errata in the Universe IIB (CA91C142B) and Universe IID (CA91C142D).

As this information will change over time, please ensure that you have the most recent version of this document by visiting the Tundra web site at www.tundra.com. Be sure to register in the Tundra Designers' Support Tools section to receive automatic e-mail notification when updates occur to this document.

Errata

Table 1: Summary of Device Errata

| Errata # | Description | Addressed in Universe IIB | Address in Universe IID |
|----------|---------------------------------------------------------------------------------------------------------------|---------------------------|-------------------------|
| 1 | Incorrect propagation of IACKIN#/IACKOUT# through the daisy chain when in BIMODE | No | No |
| 2 | Incorrect negation of VOE# during MBLT slave writes through the VME slave channel in a heavily loaded system. | No | No |
| 3 | Improper PCI cycle termination in 64 bit PCI applications | No | Yes |
| 4 | ESD Sensitivity | No | Yes |
| 5 | DY4 AUTO-ID Incompatibility | No | No |
| 6 | Incorrect Operation of Vown/Vack | No | No |
| 7 | Incorrect deassertion of LOCK# during exclusive accesses. | No | No |
| 8 | PCI REQ# line driven incorrectly during Reset | No | No |

Design Notes

Table 2: Summary of Device Design Notes

| Note # | Description |
|--------|-----------------------------------------------|
| 1 | Universe IIB/IID Maximum Junction Temperature |
| 2 | Universe IIB/IID power sequencing guidelines |

Errata

1. Incorrect Propagation of IACKIN#/IACKOUT# through the daisy chain when in BIMODE.

When an interrupt is generated in a multiple board VME system, the interrupt handler will initiate an IACK cycle to service this interrupt and generate IACKOUT# onto the daisy chain. If the Universe is configured to be in BIMODE, it will NOT propagate the IACKOUT# signal through the daisy chain when it receives IACKIN*. As a result, the interrupter will not receive IACKIN# and DTACK# will not be generated. The IACK cycle will not terminate properly and a bus error (BERR#) will occur due to a VMEbus system time out.

When generating interrupts in a multiple VME board based system, the Universe MUST NOT be configured in BIMODE.

2. Incorrect negation of VOE during MBLT slave writes through the VME slave channel in a heavily loaded system.

In a heavily loaded system, when an external master initiates a VME MBLT coupled write cycle through the VME slave channel, if the VME Master negates the write signal without enough hold time on the last data phase, this will cause the Universe to negate its VOE# signal prematurely which will disable all the buffers. Any subsequent VME cycles to the Universe IIB will end up with a VME bus error, as the Universe will not respond to any cycle. The VOE# signal is negated when a cycle is generated to the Universe with both data strobes (DS0#, DS1#) asserted.

As per the VME64 specification (Rule 2.49), a VME master is supposed to provide 10ns hold time from the negation of DS1# to the negation of the write signal, whereas the VME slave should expect 0ns hold for the negation of the write signal to the negation of DS1#. The Universe requires a 5ns hold time from DS1# negation to WRITE# negation in violation of the above rule.

Enabling the Universe's internal DSx# filter will aggravate this behaviour as the internal DSx# signals are delayed further from the external DSx# signals.

3. Improper PCI cycle termination

In 64 bit PCI bus applications the Universe may exhibit incorrectly terminated cycles on the PCI bus when the Universe is acting as a PCI Initiator. The incorrect PCI bus termination is logged as a Master Abort in the PCI_CSR of the Universe. This errata is isolated to 64 bit PCI bus applications.

The issue is aggravated by elevated ambient temperature (above 40C), reduced 5V supply voltage (approximately 4.75 V), PCI clock speed of 33MHz, increased PCI bus loading and specific data patterns. The worst case pattern has been identified as alternating Fis and 0ís

This errata can be captured on an analyser as follows:

- i Trigger the scope from the output trigger of the analyser
- i Set the trigger for the analyser to be the following:
 - i LEVEL 1: Find Frame Low 1 Time Else on Not Frame goto Level 1
 - i LEVEL 2: Find rising edge of TRDY
 - i LEVEL 3: Find (Frame =1, IRDY=0 DEVSEL=1 TRDY=1 STOP=1) 9 times else goto level 1.

Notes: You may need to change the number of times to find the pattern in Level 3.

Please contact Applications Engineering at Tundra Semiconductor Corporation (support@tundra.com), if you observe the above described errata.

4. ESD Sensitivity

The Universe IIB (CA91C142B) does not meet 2000V ESD tolerance as per MIL STD 883 Method 3015 Human Body Model test. The most sensitive ESD tolerance is 500V HBM seen on the AVDD and AVSS pins.

The following precautions are recommended when handling the Universe IIB devices to reduce ESD exposure:

- ï Wear wrist straps while seated.
- ï Wear footwear or heel straps while standing.
- ï Wear ESD smocks.
- ï Regularly check wrist straps and footwear.
- ï Ensure ESD dissipative flooring and work surfaces.
- ï Ensure work surfaces and equipment connected to electrical ground.
- ï Use ESD compliant chairs and carts, or "drag-chain" to the floor.
- ï Ensure humidity in all inspection and assembly areas maintained between 30% and 70%.
- ï Minimize inspection and handling.
- ï If inspection is required, keep parts within trays (if possible).
- ï No conductive or electrostatic generating materials in close proximity to unprotected product, e.g. shop travelers, labels, cardboard, Plexiglas, wood, CRT screens, etc.
- ï Ionization systems should be in place to help dissipate residual charge built up on any material that is static generating and in close proximity to Universe IIB devices.
- ï A field strength meter can be used to check items that come into contact with the Universe IIB; this tool may be very useful in confirming safe surfaces and those that contain residual charges that may need neutralizing ionizers.

New devices are currently being manufactured to correct the ESD sensitivity of Universe IIB.

Universe IID (CA91C142D) ESD sensitivity meets or exceeds 2000 V HBM

5. DY4 AUTO-ID Incompatibility

When the Universe is the system controller (syscon), IACKOUT should be asserted on the 7th SYSCLK clock edge, however it is asserted on the 5th edge, which will cause subsequent cards to come up at one slot address too low. The incorrect count may cause problems in software, if not taken into account when DY4 Auto-ID is used.

6. Incorrect Operation of Vown/Vack

When setting the VOWN bit and changing the request level by modifying the VRL bits in the MAST_CTL register simultaneously, there is approximately a 40ns delay of the assertion of the new VRL value. The VMEbus arbiter will see the Universe request on the 'old' request level, and if the bus is not busy, the arbiter will immediately issue a bus grant which will be acknowledged by the Universe on the 'old' request level. If the bus is busy, or the grant comes back after the delay in the assertion of the VRL bits, the UNIVERSE will have switched to the 'new' request level.

Adhering to the VMEbus specification, the Universe will not acknowledge bus grants on any other level than the one it is on; the Universe will propagate the bus grant coming in on the 'old' bus request level down the bus grant daisy-chain. Also, the UNIVERSE will not release the BR [old]* line because it has not received a grant from the arbiter on its current request level yet. The Universe will continue to request the bus on the 'old' level indefinitely, and the arbiter will continue to issue grants on the 'old' request level, which will either time out, or be acknowledged by a Master further down the daisy-chain.

Workaround:

To avoid this situation, set the VRL bits in MAST_CTL register in the first of two writes. This will allow time for the Universe to change bus request levels before requesting the VMEbus. On the second write to MAST_CTL, set the VOWN bit.

7. Incorrect Deassertion of LOCK# During Exclusive Accesses

Under particular conditions, the Universe may deassert PCI LOCK# incorrectly during exclusive accesses initiated from the VMEbus. These conditions are described below:

During a read modify write cycle to the Universe device by a VMEbus master, a PCI agent simultaneously accesses the Universe device as a PCI slave to perform a read/write cycle to the VMEbus. The Universe device acquires the PCI bus to complete the RMW cycle before the PCI agent is granted the PCI bus.

If the above conditions occur and the Universe device is retried on the PCI bus by the PCI target long enough to cause a VMEbus timeout during the read modify write cycle, then any subsequent attempts to complete the VMEbus RMW read while the PCI agent attempts to complete the PCI read/write cycle will cause the Universe to assert LOCK# and deassert it within 1 PCI clock cycle.

This is in violation with the PCI 2.1 specification which states that LOCK# must be asserted the clock following the address phase and kept asserted to maintain control. LOCK# must be released only if the initial transaction of the LOCK# is terminated with Retry, Target-Abort, or Master-Abort.

Work-around:

There are two possible solutions to avoid the above situation. The first is to ensure that the PCI target does not retry the VME Read Modify Write long enough to cause a VMEbus timeout error. The second is to program the Universe's PCI master interface to generate a Master Abort prior to a bus error timeout occurring on the VMEbus. This is done by programming the MAXRTRY field in the MAST_CTL register (offset 0x400).

7. PCI REQ# Line Driven Incorrectly during Reset

During a PCI Reset (RST# asserted) or power on reset (PWRRST#), the Universe will incorrectly drive the REQ# signal high. This is in violation of the PCI 2.1 specification which states this signal must be tristated during reset.

Design Notes

1. Universe IIB/IID Maximum Junction Temperature

Tundra recommends that the maximum junction temperature of the Universe IIB and IID devices not exceed 150 C by using adequate heat dissipation techniques such as heat sinks and forced airflows. Long term reliability with operation at a junction temperatures above 150 C has not been characterized.

2. Universe IIB/IID power sequencing guidelines

When designing with the Universe IIB/IID devices, care should be taken when powering the device to ensure proper operation. Designers should make sure that no signals are applied to any Universe IIB/IID signal pins prior to stable power being applied to the device.

In a mixed 3.3V and 5V design, it is recommended that 5V power be stable prior to other devices coming out reset. Should other devices come out of reset before the 5V power is stable, designers should make certain that no signals are driven to the Universe IIB/IID signal pins, including possible signals from the VME backplane.