

The DØ Silicon Track Trigger

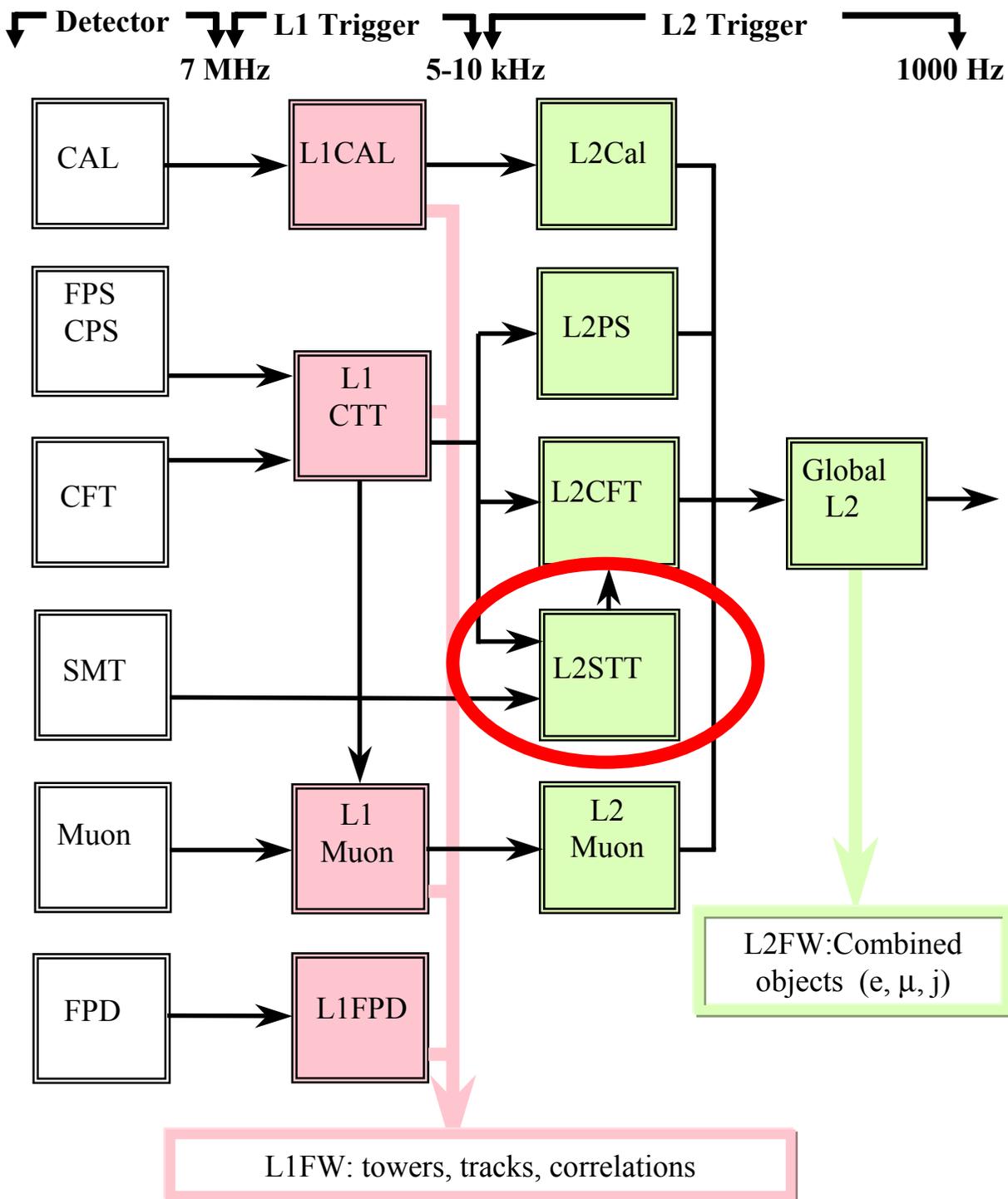
- Introduction
- Overview of STT
- STT Hardware Design
 - ◆ Motherboard
 - ◆ Fiber Road Card
 - ◆ Silicon Trigger Card
 - Cluster Algorithm
 - ◆ Track Fit Card
 - Track Reconstruction

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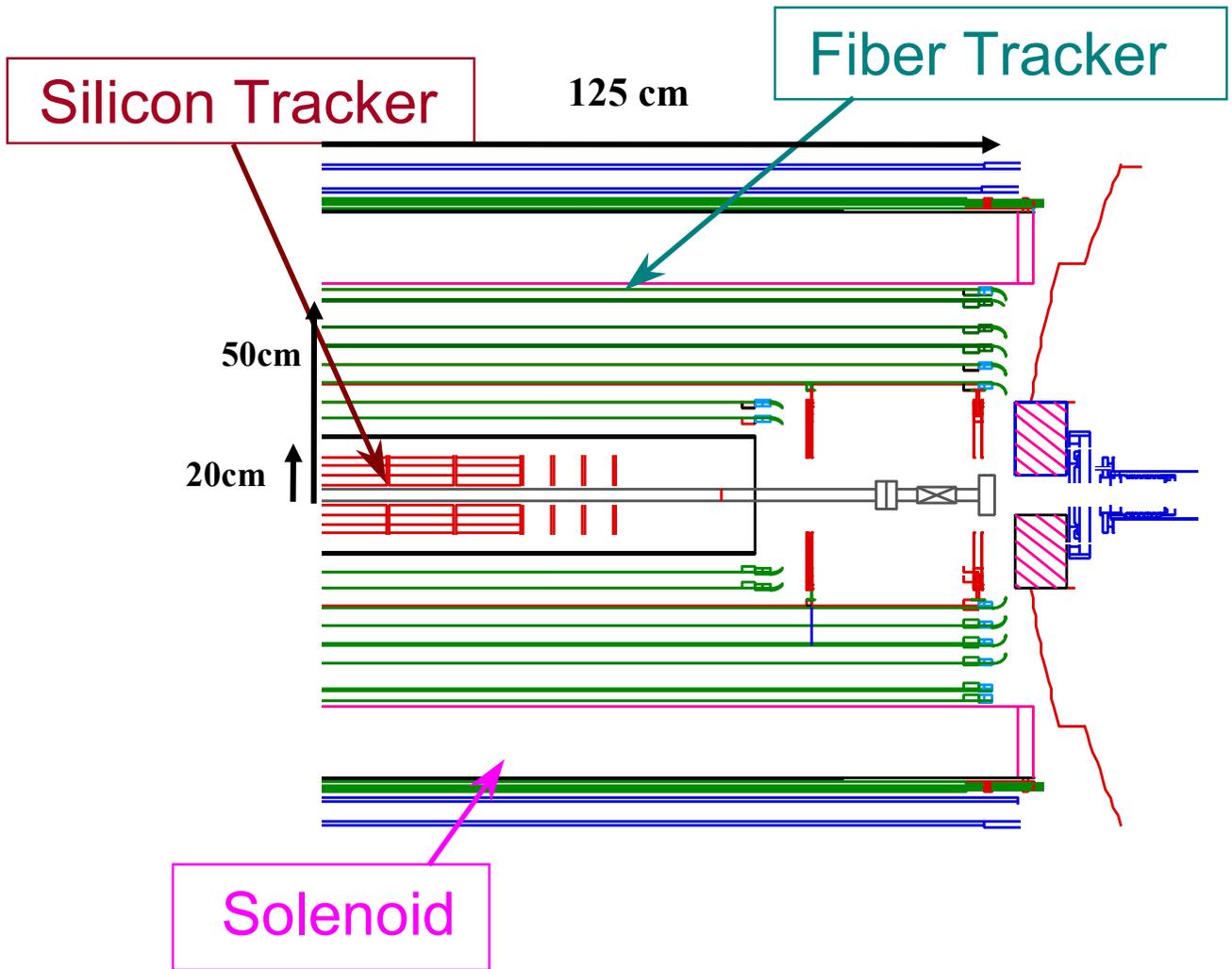
Run II TeVatron

- Fermilab, near Chicago USA
- $\sqrt{s} = 1.96 \text{ TeV}$ pp collider
 - ◆ Bunch crossing time is 396 ns (eventually 132 ns)
 - ◆ Run II starts March 2001
 - ◆ Expect 2 fb^{-1} of integrated luminosity in the first 2 years
- DØ needs a trigger that
 - ◆ offers high reduction of backgrounds
 - ◆ allows efficient selection of rare process signatures
 - ◆ makes its decision fast (e.g., L2 has $100 \mu\text{s}$)

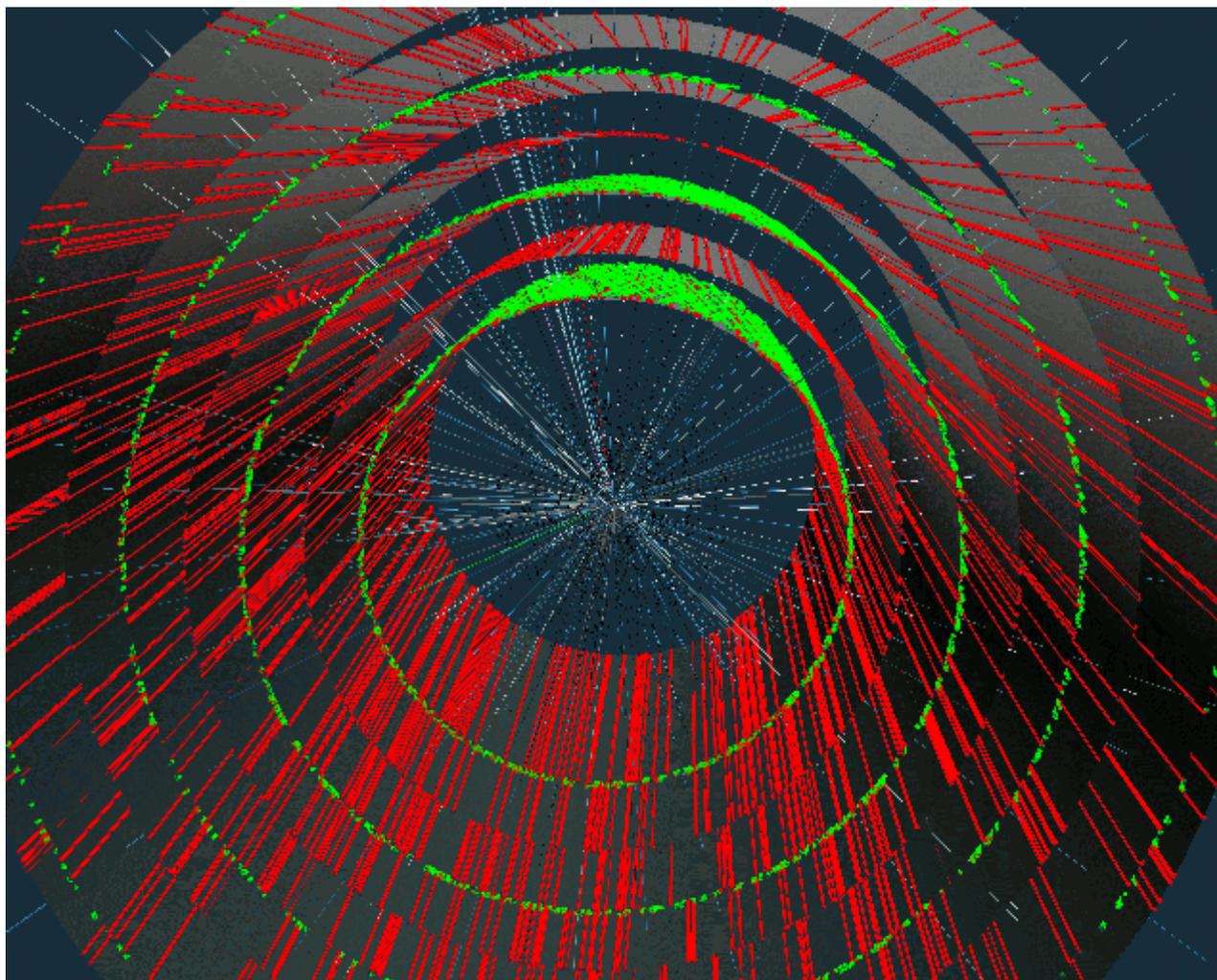
DØ Trigger System



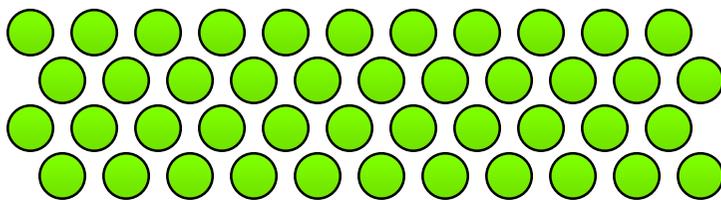
DØ Tracking System



DØ Fiber Tracker

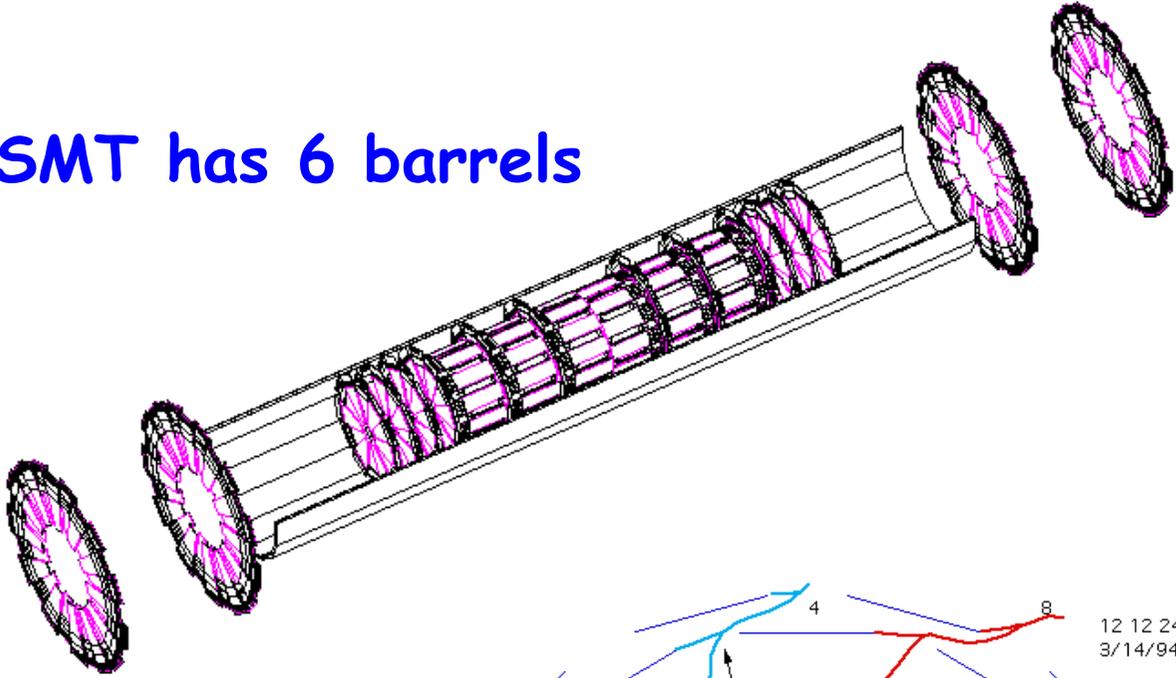


CFT has 8
layers: A-H

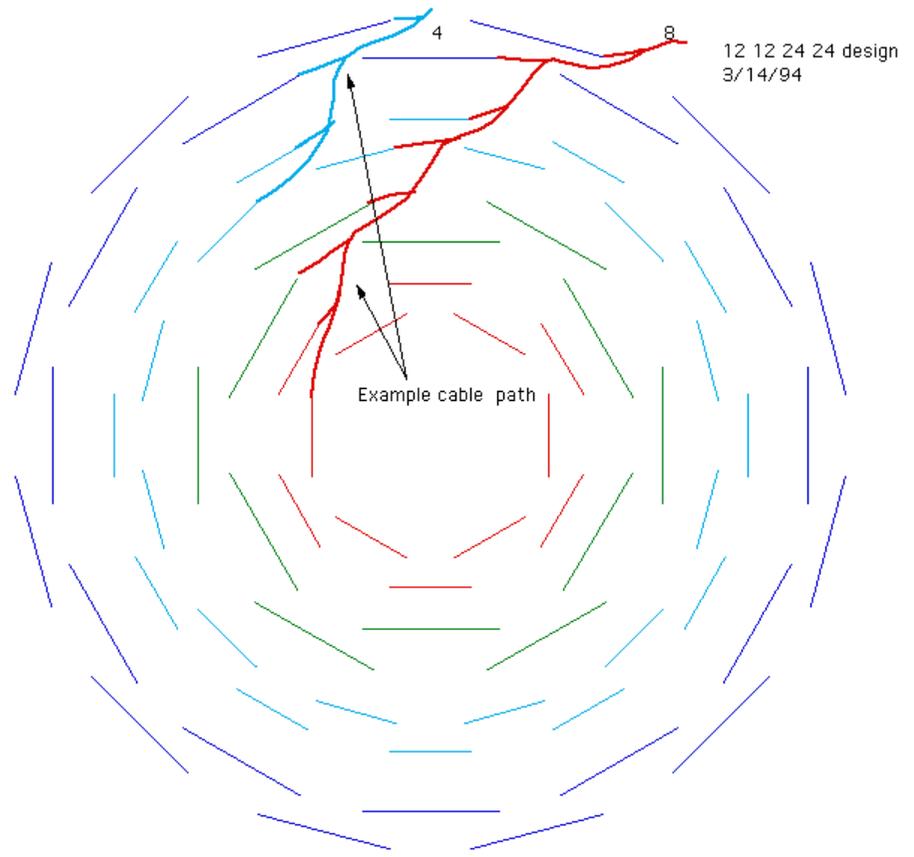


DØ Silicon Detector

SMT has 6 barrels



and 4 layers

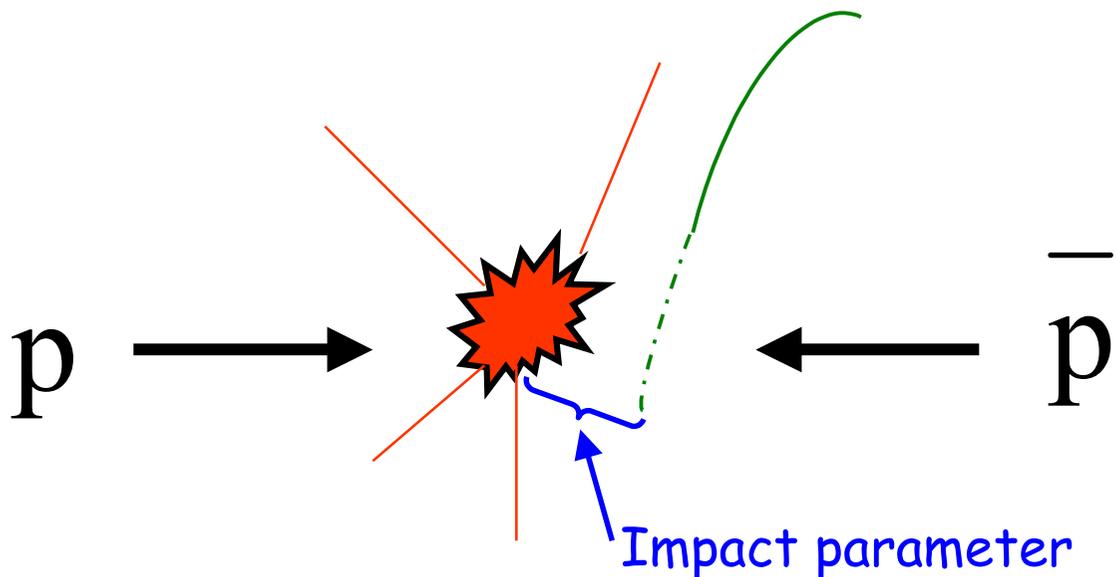


DØ SMT Barrel



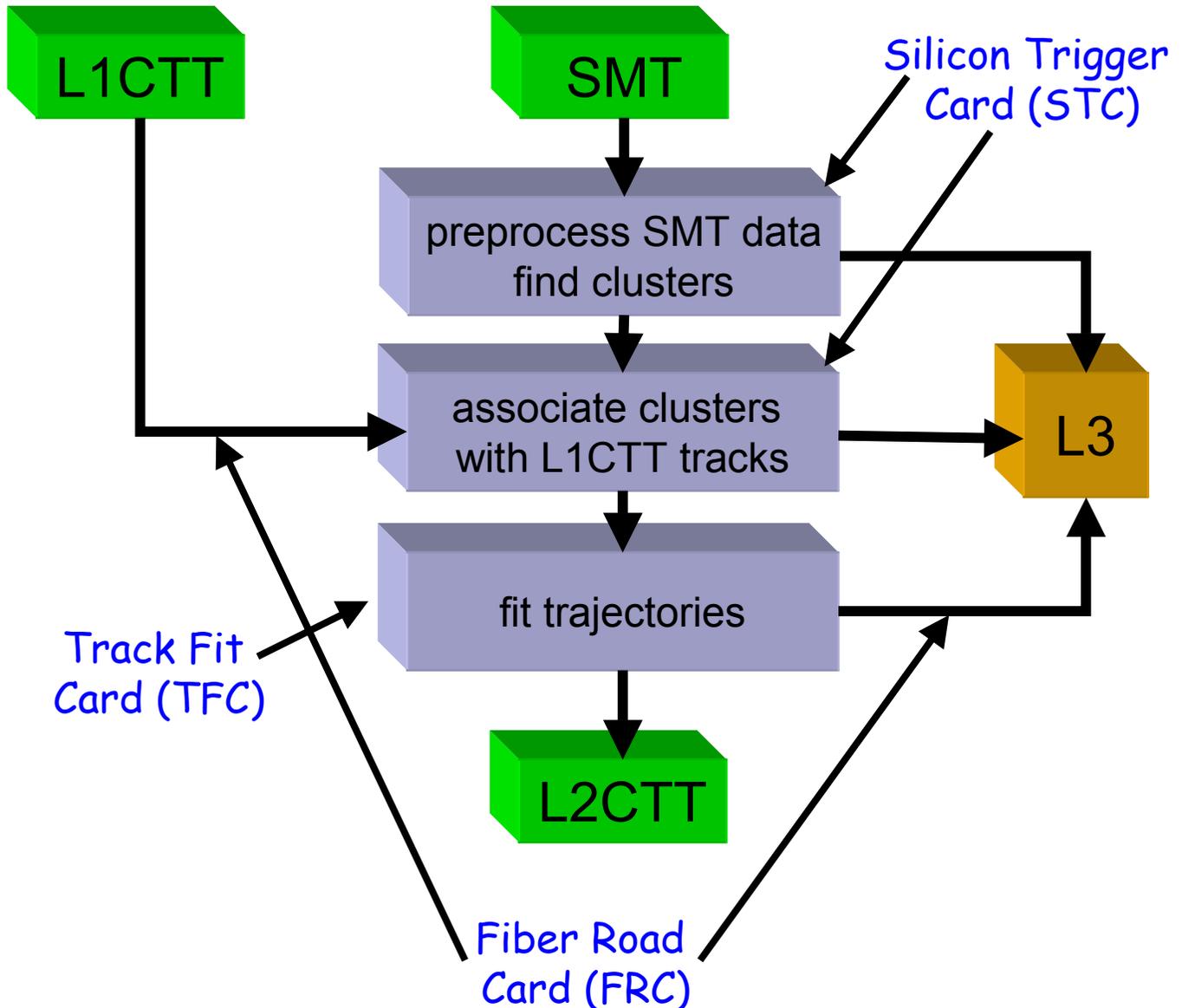
Run II Physics at DØ

- Decay signatures of top quark, Higgs boson, SUSY, and b quark include displaced tracks



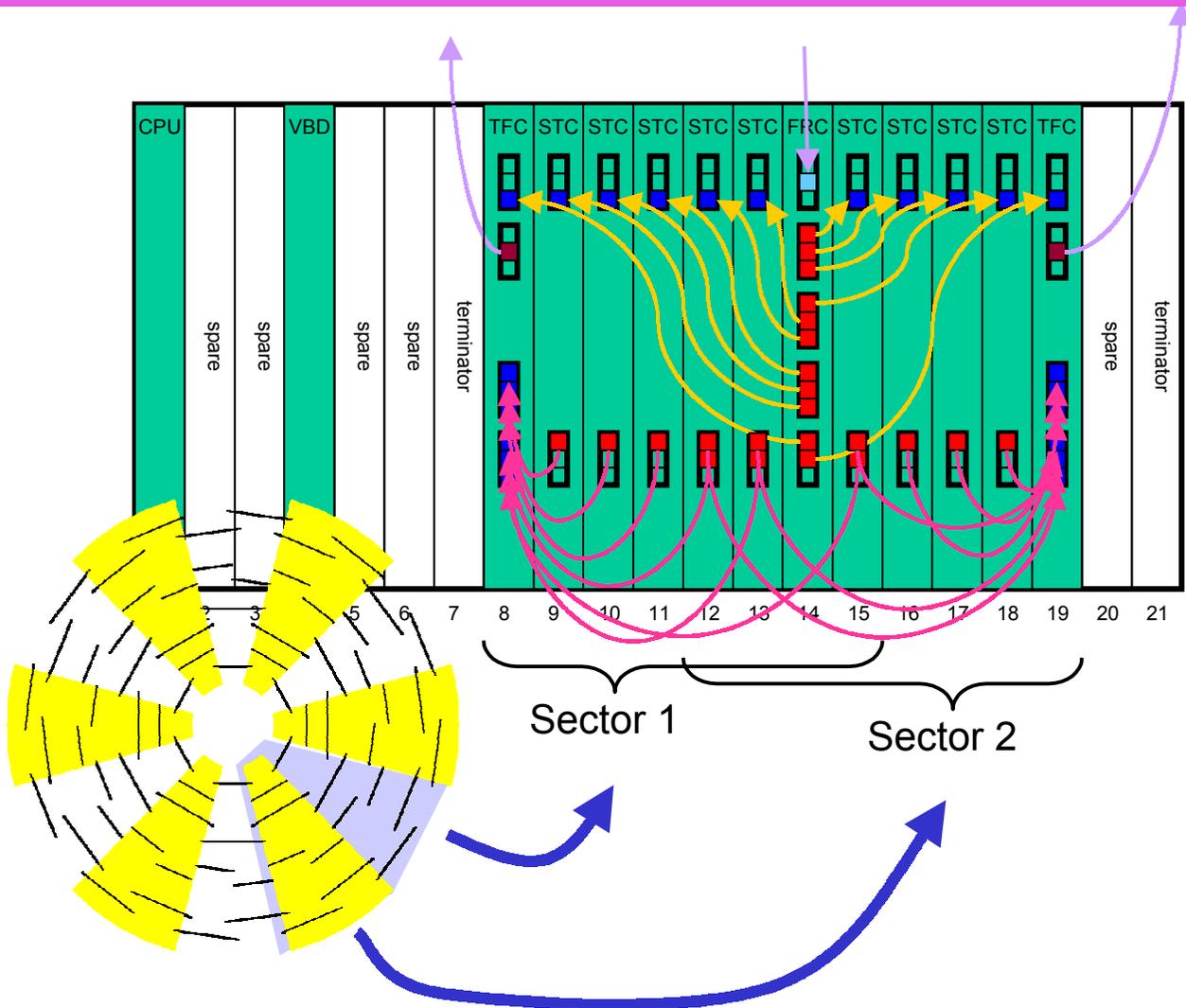
- Silicon Track Trigger identifies displaced tracks with high efficiency and purity in $25 \mu\text{s}$
- STT will be installed one year after the start of Run II

Overview of STT



3 custom VME boards mounted on common custom motherboard

STT Hardware Design



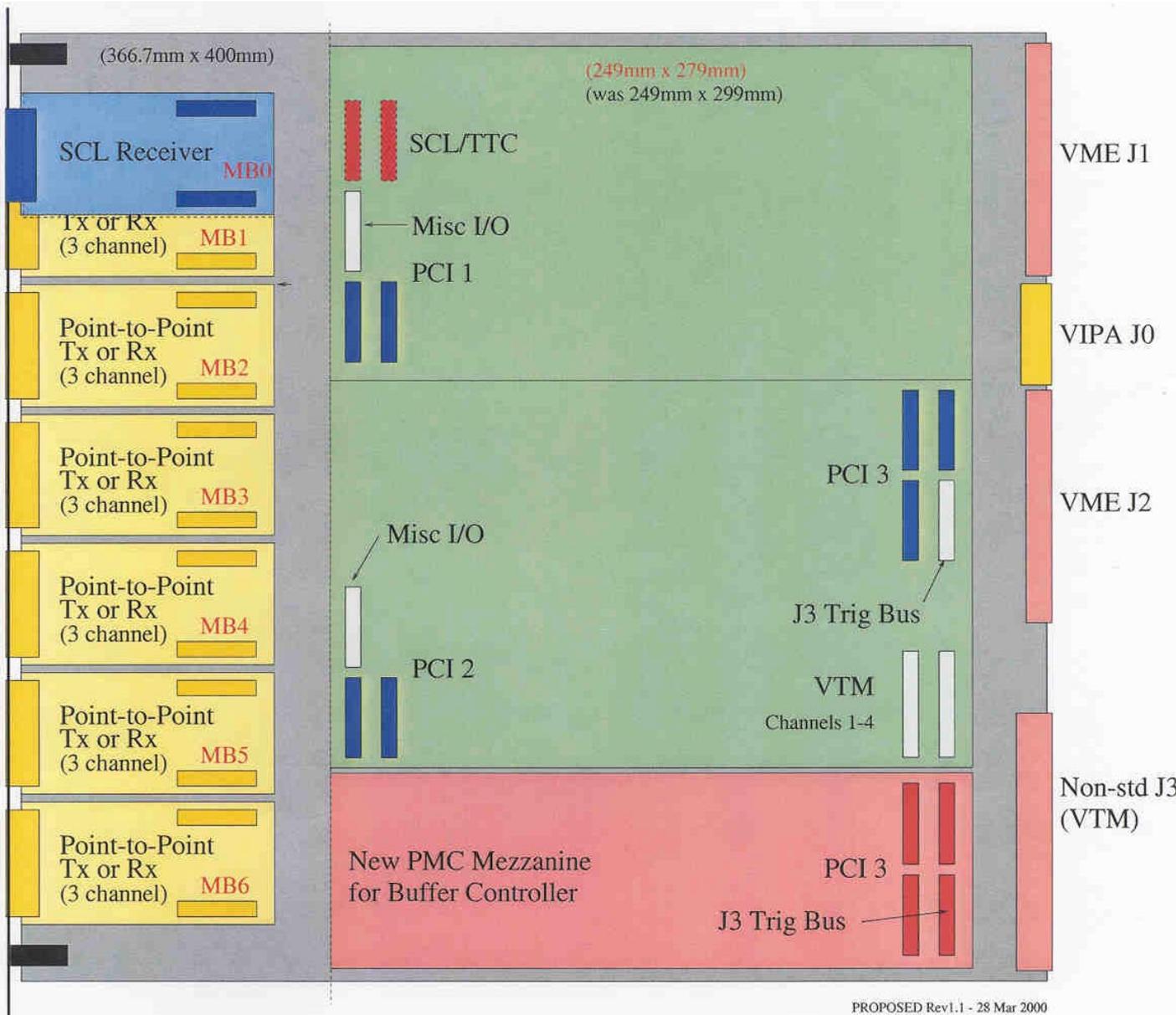
Since most high- p_T tracks stay
in 30° SMT sector, 12
STT sectors are independent

STT Motherboard

- Logic cards share requirements for internal and external interfaces
- Mount logic daughter cards on common motherboard
- 9Ux400 mm VME64x-compatible
- 3 33-MHz PCI busses for on-board communications

- Data communicated between cards via point-to-point links (LVDS)
- Control signals sent over backplane
- VME bus used for Level 3 readout and initialization/monitoring

STT Motherboard



PROPOSED Rev1.1 - 28 Mar 2000

Initialization/Downloading

- **Crate controller**
 - ◆ **Motorola MVME2302 200 MHz CPU**
- **Initializes STT cards at power-up**
- **Downloads lookup tables and FPGA/DSP code to STT cards**
 - ◆ **Notifies destination card of download**
 - ◆ **Information (e.g., DSP code) read from host computer over Ethernet**
 - ◆ **Information passed across VME backplane through motherboard's PCI bus to destination card**
 - ◆ **I/O controller on destination card transfers data to destination**
- **Gathers information from other cards for monitoring purposes**

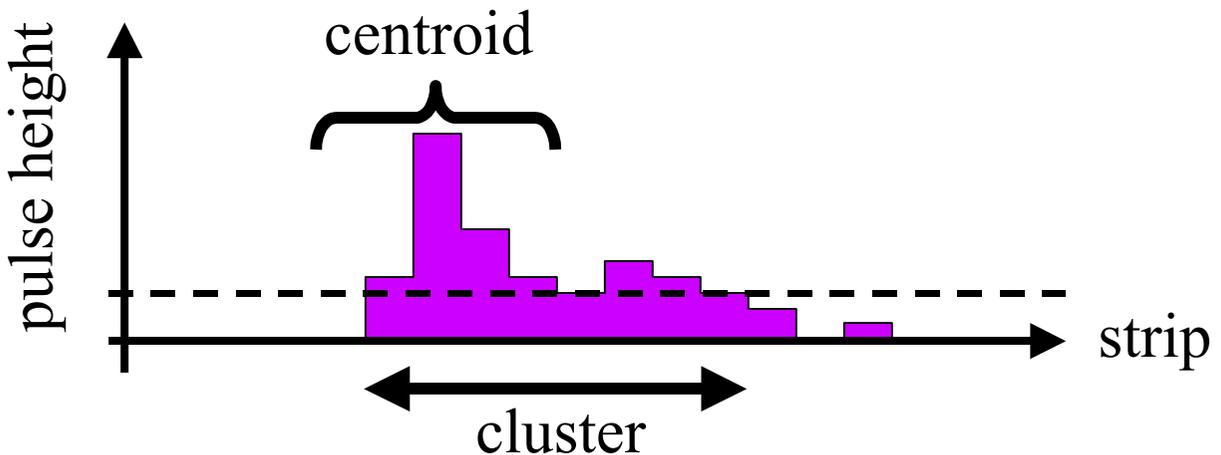
Fiber Road Card

- **Trigger receiver** communicates with the trigger framework (**SCL receiver card** on motherboard) and broadcasts any control signals to the other cards (J3)
- **Road receiver** receives tracks from the Level 1 CFT trigger
- **Trigger/road data formatter** constructs the trigger/road data blocks and transmits this information to the other cards
- **Buffer manager** handles buffering and readout to Level 3

- Implemented in 3 **FPGAs**

Silicon Trigger Card

- Bad strips are masked (LUT)
- Pedestals/gains are calibrated (LUT)
- Neighbouring SMT hits (axial or stereo) are clustered using **FPGAs** programmed in VHDL



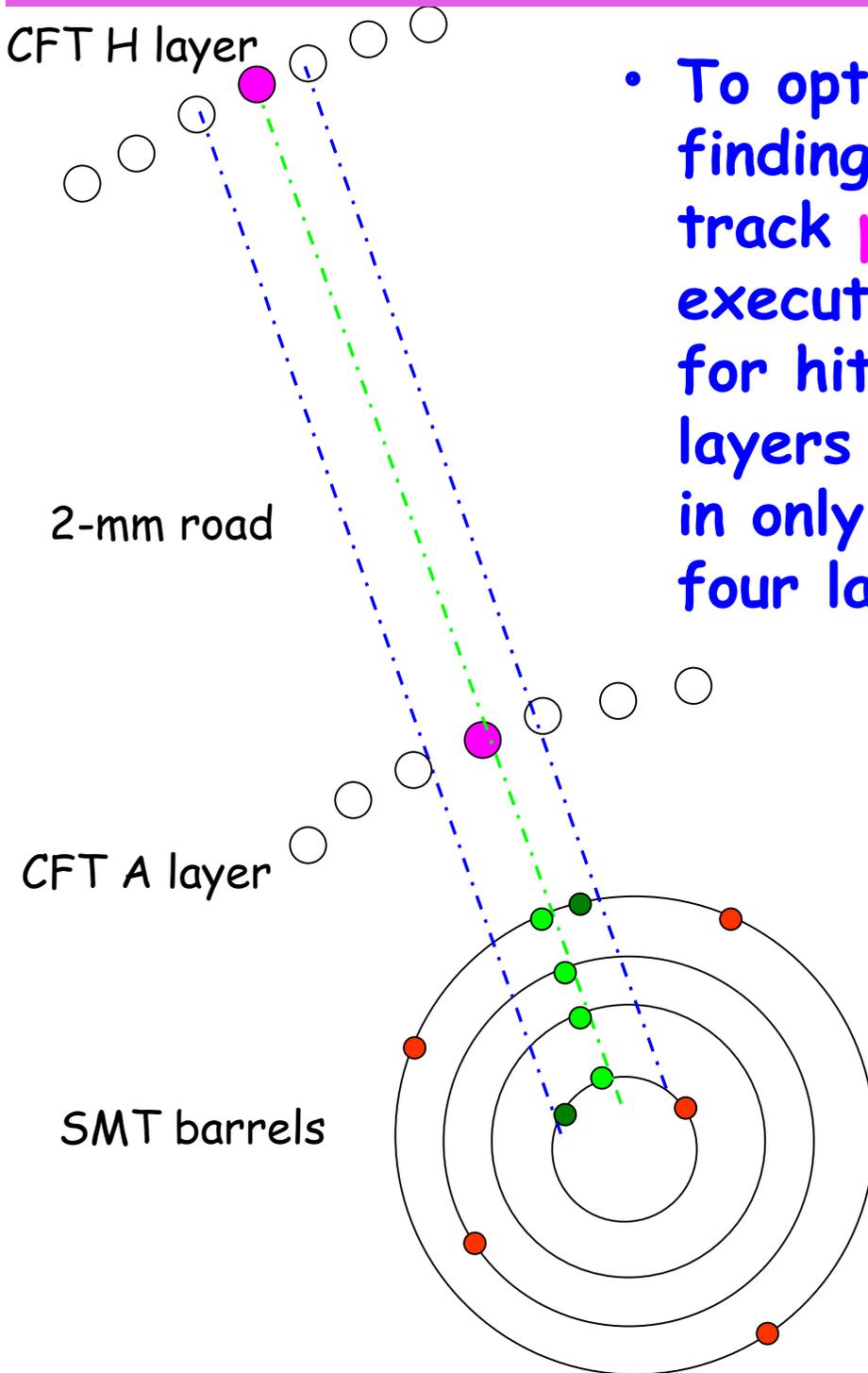
- Axial clusters are matched to **$\pm 1\text{mm}$ -wide roads** around each CFT track via precomputed LUT

Track Fit Card

- Control logic (Altera FPGAs) maps each road to one of **eight** processors and handles I/O buffer management
- Processor (TI DSP) receives **2 CFT hits** and **r - ϕ SMT clusters** in road defined by CFT track
- Lookup table used to convert hardware to physical coordinates
- C program on DSP selects clusters closest to road center at each of **4 layers** and performs a **linearized track fit**:

$$\phi(r) = \frac{b}{r} + \kappa r + \phi_0$$

Hit Filtering Algorithm



- To optimize track-finding **efficiency**, track **purity** and **execution time**, look for hits in all four layers but allow hits in only three out of four layers

Track Reconstruction

- Formulate track equation in terms of **hits** (3 or 4 SMT + 2 CFT hits)
- With ϕ_1 as reference, use ϕ **residuals** in computation

$$\begin{pmatrix} b \\ \kappa \\ \phi_0 \end{pmatrix} = \begin{pmatrix} \text{Inverse Matrix} \\ 3 \times (N_{\text{hits}} - 1) \end{pmatrix} \times \begin{pmatrix} \Delta\phi_2 \\ \Delta\phi_3 \\ \Delta\phi_4 \\ \Delta\phi_A \\ \Delta\phi_H \end{pmatrix}$$

- near-zero ϕ residuals allow use of **integer arithmetic**
- Matrix is precomputed and stored in a lookup table

Beam Spot Correction

- Track parameters computed wrt **detector origin (0,0)**
- Impact parameter relevant to physics measured wrt pp collision (i.e., **beam spot**)
- Beam spot position downloaded to STT on a run-by-run basis
- Impact parameter correction performed in DSP

$$b_{corr} = b + \text{sign}(\kappa) r_B \sin(\phi_B - \phi_0)$$

where (r_B, ϕ_B) is beam position

- Beam spot offset tolerance is **1 mm**, within Tevatron specs

Performance

- Impact parameter resolution of $35\ \mu\text{m}$ includes
 - ♦ beam spot size ($30\ \mu\text{m}$)
 - ♦ SMT resolution ($15\ \mu\text{m}$)
- STT introduces negligible uncertainty to resolution
- Monte Carlo calculation predicts 2 CFT tracks, 14 SMT clusters per sector and 3.7 clusters per track
- Using above, queuing simulation predicts average STT latency is $25\ \mu\text{s}$ with negligible dead-time

Conclusions

- STT represents **custom** solution to DØ's trigger requirements for Run II
- Decision time is **25 μ s** with negligible dead-time
- Design of motherboard as well as logic cards well under way
- Card prototypes ready in **3 months** for testing
- FPGA and DSP programming progressing
- STT will be installed and running by **March 2002**