

Trigger & DAQ

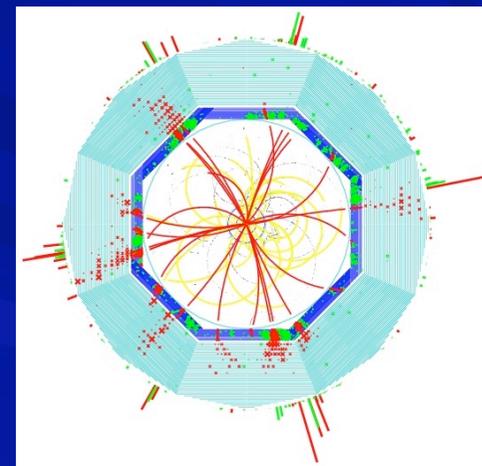
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Evolution of basic parameters

Exp. <i>Year</i>	Collision rate	Channel count	L1A rate	Event building	Processing Power	Sociology
UA's <i>1980</i>	3 μ sec	-	-	-	5-10 MIPS	150-200
LEP <i>1989</i>	10-20 μ sec	250 - 500K	-	10 Mbit/sec	100 MIPS	300-500
BaBar <i>1999</i>	4 ns	150K	2 KHz	400 Mbit/s	1000 MIPS	400
Tevatron <i>2002</i>	396 ns	~ 800 K	10 - 50 KHz	4-10 Gbit/sec	$5 \cdot 10^4$ MIPS	500
LHC <i>2007</i>	25 ns	200 M*	100 KHz	20-500 Gbit/s	$>10^6$ MIPS	2500
ILC <i>2020 ?</i>	330 ns	900 M*	3 KHz	10 Gbit/s	$\sim 10^6$ MIPS ?	$> 3000 ?$



* including pixels



Sub-Detector	LHC	ILC
Pixel	150 M	800 M
Microstrips	~ 10 M	~30 M
Fine grain trackers	~ 400 K	1,5-3 M
Calorimeters	200 K	30-100 M
Muon	~1 M	

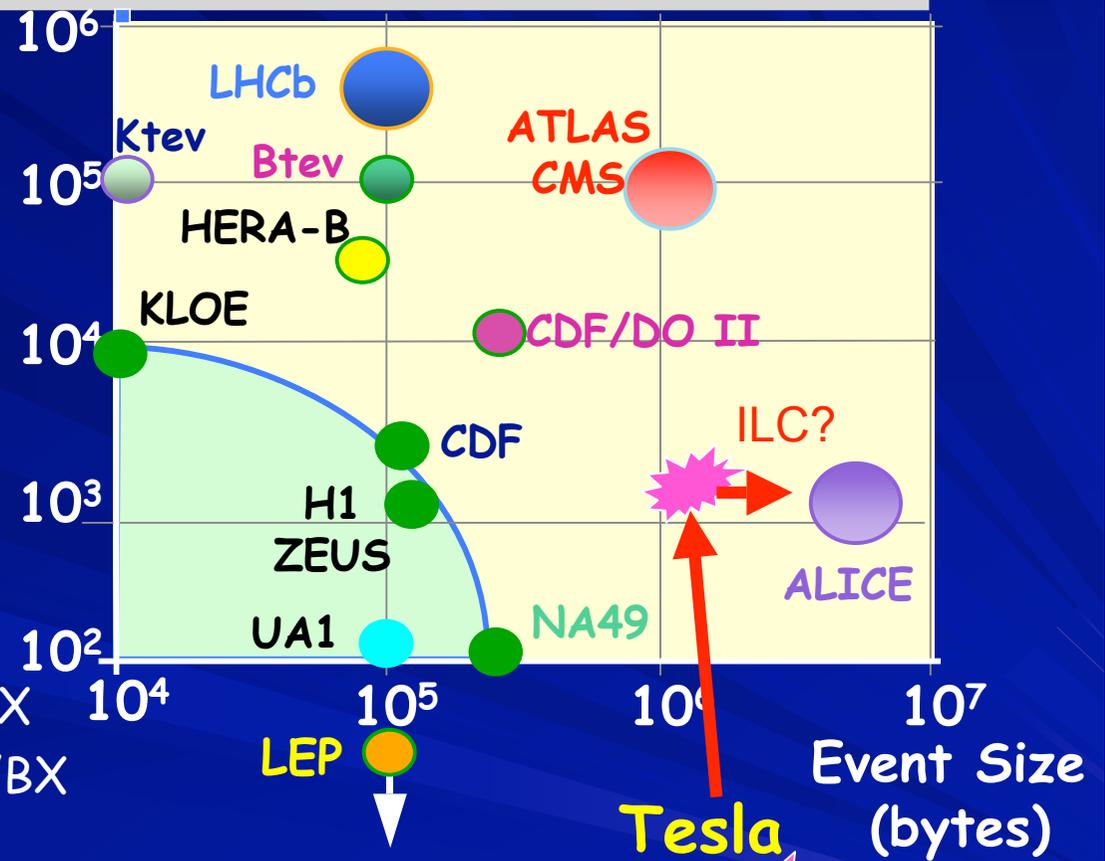
Rates and data volume

High Level-1 Trigger
(1 MHz)

TESLA numbers

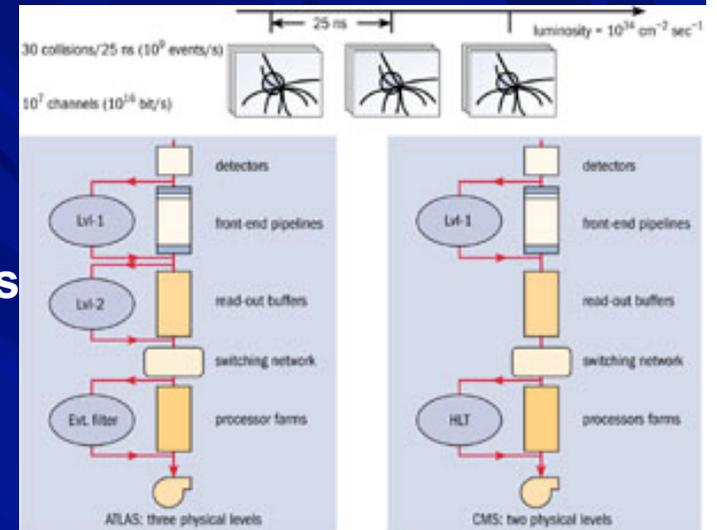
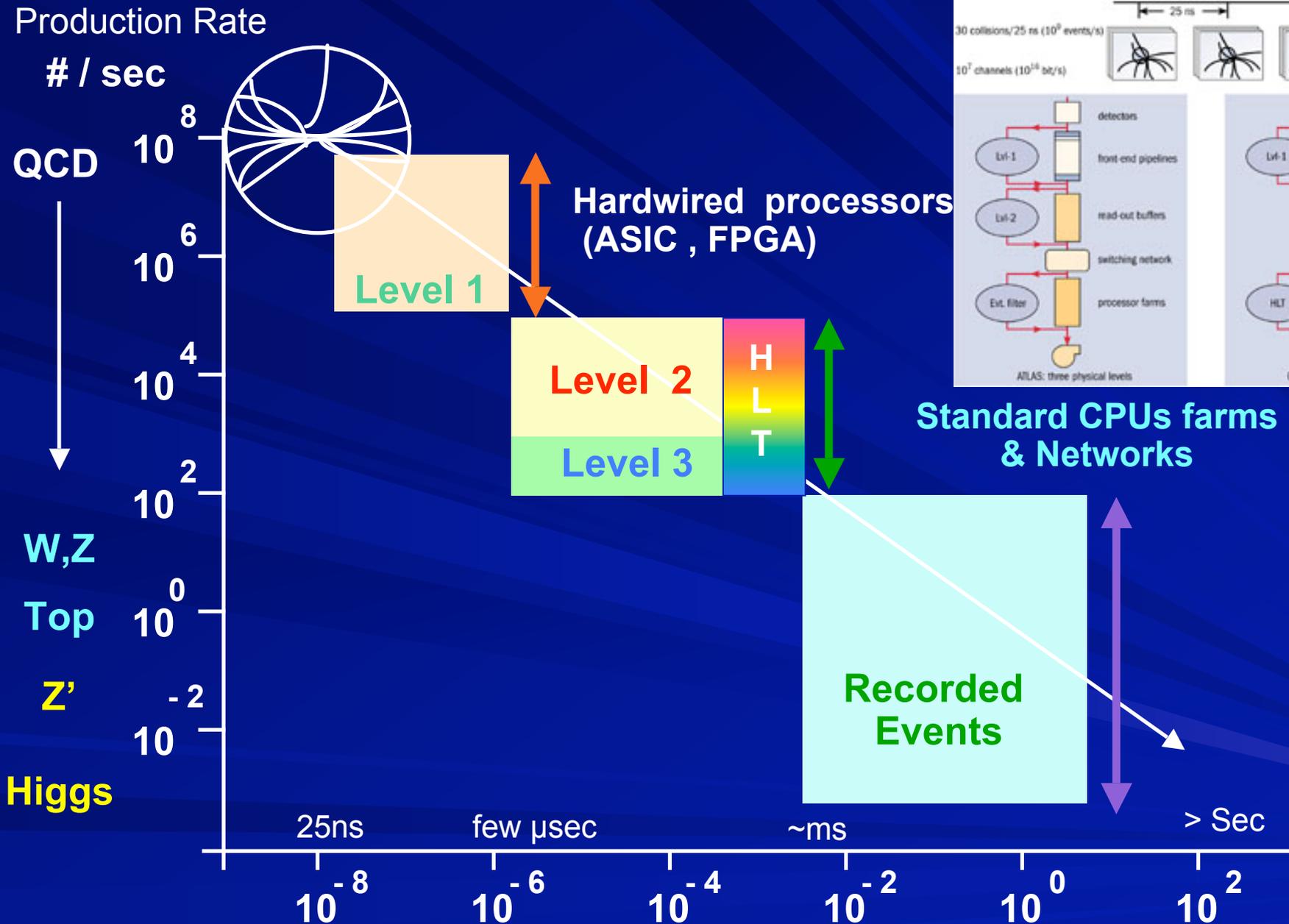
- *Physics Rate :*
 - $e^+ e^- \rightarrow X$ 0.0002/BX 10^4
 - $e^+ e^- \rightarrow e^+ e^- X$ 0.7/BX
- *$e^+ e^-$ pair background :*
 - VXD inner layer 1000 hits/BX
 - TPC 15 tracks/BX

→ *Background is dominating the rates !*

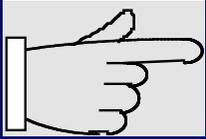


Need a new estimation for ILC

LHC Multilevel Selection scheme



Standard CPUs farms & Networks



Strategy for event selection @ LHC

40 MHz

L1



100 KHz

L2



1 KHz



L3

100 Hz

"Local" identification of high Pt objects → *use coarse dedicated data*

- Electrons /Photons , Hadrons & Jets → Energy clusters
- Muons → Track segments
- Neutrinos → Missing Et

Particle signature (e/g,h,Jet, μ ...) → *use final digitized data*

- Refine Pt cuts → fine granularity & track reconstruction
- Combine detectors → Converted electron , "Punchthrough" , decays
- **Global topology** → multiplicity & thresholds

Identification & classification of physics process → *trigger menu*

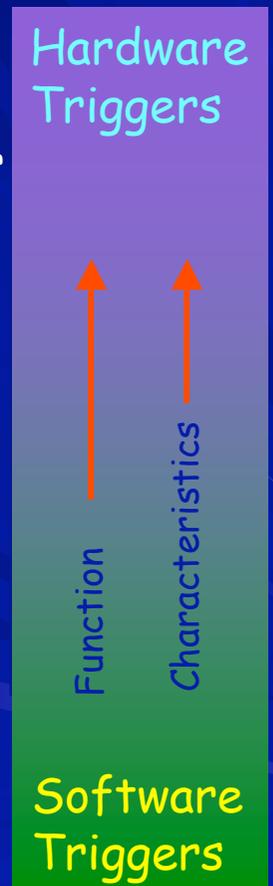
- Partial event reconstruction → Vertices , Masses ,Missing Et....

■ **Physics analysis**

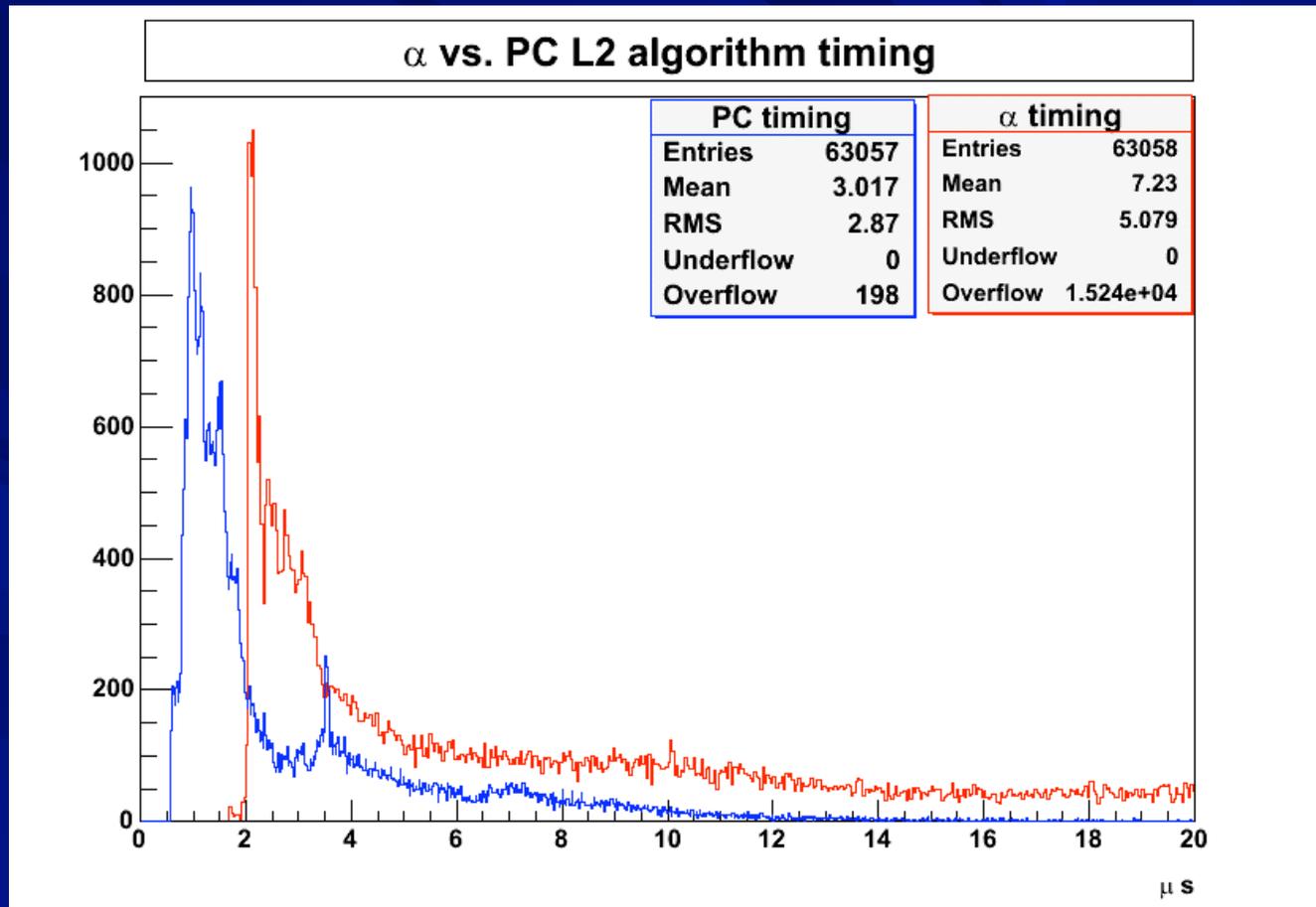
- "Off-line" type analysis of classified events

Present evolution (Tevatron, LHC ...)

- Higher level trigger decisions are migrating to the lower levels → **Software Migration is following functional migration**
 - Correlations that used to be done at Level 2 or Level 3 in are now done at Level 1.
 - More complex trigger (impact parameter!) decisions at earlier times (HLT) → Less bandwidth out of detector?
- **Boundaries**
 - L2 and L3 are merging into High Levels Triggers
 - DAQ and trigger data flow are merging
 - On-line and off-line boundaries are flexible
- **Recent Developments in Electronics**
 - Line between software and hardware is blurring
 - Complex Algorithms in hardware (FPGAs)
 - Possible to have logic designs change after board layout
 - Fully commercial components for high levels.

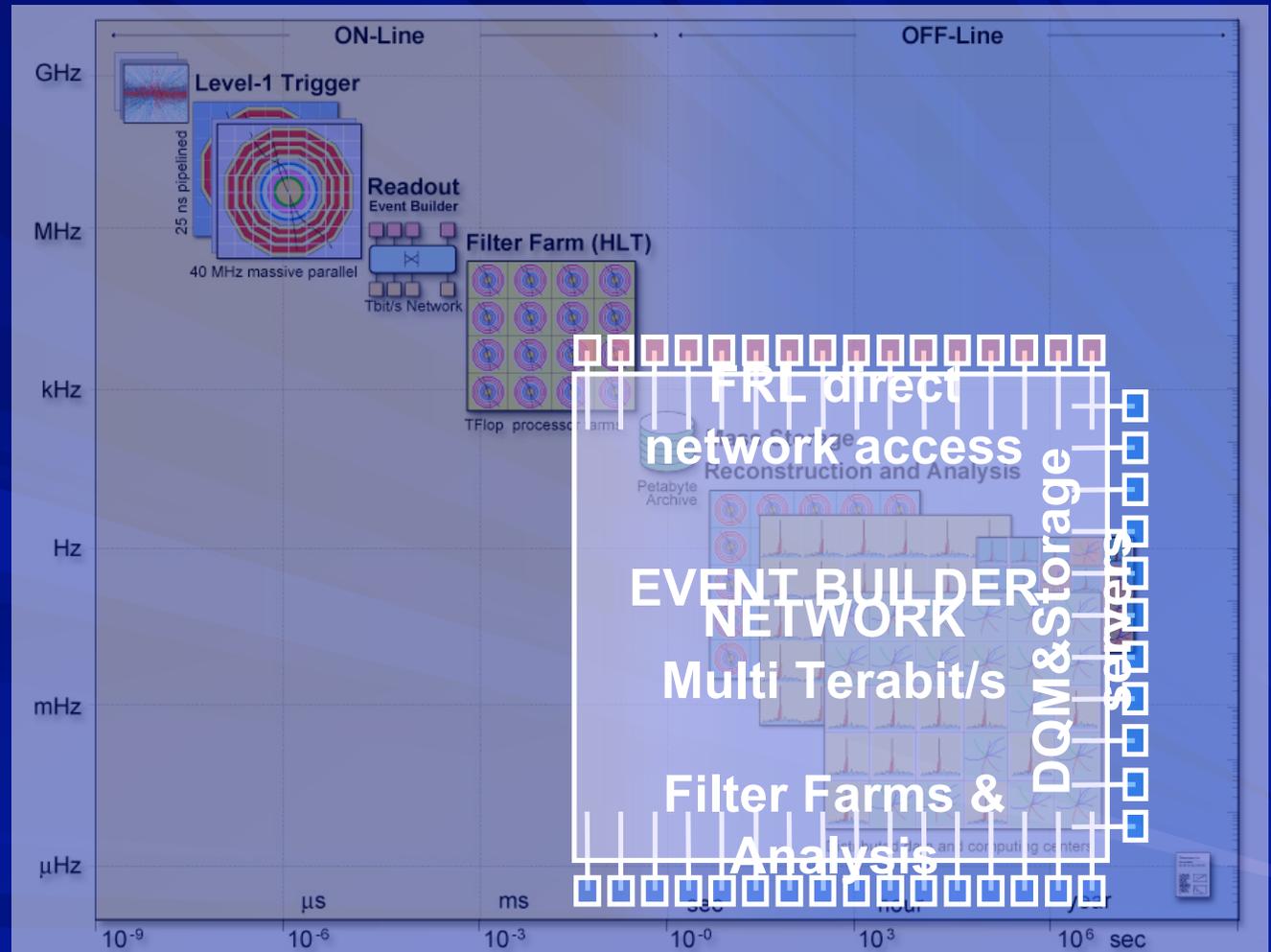
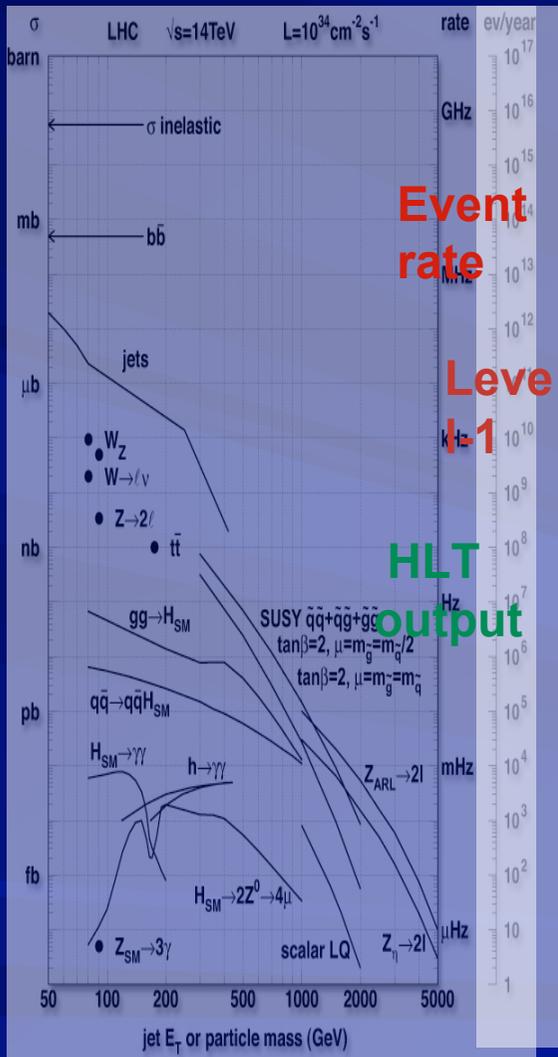


The Tevatron (CDF) L2 lesson



- Alpha = many years of efforts ...hardware and software
- PC (Commercial): few months to implement! No hardware!

DAQ data flow and computing model



Technology forecast



*Summary of the talk given by D. Calvet at the IEEE Real Time Conference ;Stockholm 4-10 June 2005.
"A Review of Techniques and Technologies for the Transport of Digital Data in Physics Experiments"*

■ End of traditional parallel backplane bus paradigm

- Announced every year since ~1989
- VME-PCI still there; watch PCI Express, RapidIO, ATCA

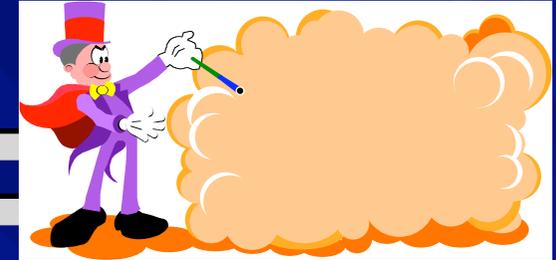
■ Commercial networking products for T/DAQ

- DAQ 94' Conferences: ATM, DS-Link, Fibre Channel, SCI
- Today: Gigabit Ethernet (1 → 10 → 30 GB/s)

■ The ideal processing / memory / IO bandwidth device

- The past: Transputers, DSP's, RISC processors
- Today: FPGA's → Integrates receiver links, PPC, DSP's and memory

Technology forecast (Con't)



■ Point-to-point link technology

- The old style: Parallel Copper - Serial Optical
- The modern style: Serial Copper - Parallel Optics
 - >3Gb/s today, 10Gb/s in demonstration

■ Processors → Moore's law still true until 2010 ...at least !

- Continuous increasing of the computing power
- Today 4GHz clock → 10 to 15 GHz in 2010 !

■ Memory size → quasi illimited !

- Today : 256 MB
- 2010 : > 1 GB ... then ?

■ Modern wisdom (about technology)

- *"People tend to overestimate what can be done in one year, and underestimate what can be done in 10 years."*

On-Off line boundaries

- **Detectors are becoming more stable and less faulty**
 - High efficiency, Low failure rate
 - Powerfull "on-line" diagnostics and error recovery (expert systems)
- **On-line computing is increasing and not doing only "data collection": More complex analysis is moving on-line**
 - » "Off-line" type algorithms early in the selection chain (b tag ..)
 - » Selection of "data streams" --> Important role of the "Filter"
 - » Precise alignment needed for triggering
 - » Detector calibration using Physics process available
 - » On-line calibration and correction of data possible
- **Common aspect →**
 - Algorithms, Processing farms, Databases...
 - use similar hw/sw components (PC farms..)



Boundaries become flexible

ILC



The ILC environment poses new challenges & opportunities which will need new technical advances in Data Collection

→ NOT LEP/SLD, NOT LHC !

■ The FEE integrates everything

→ From signal processing & digitizer to the RO BUFFER ...

■ Very large number of channels to manage (Trakers & ECal)

■ Interface and feedback between detector & machine is fundamental

→ optimize the luminosity → consequence on the DAQ architecture

■ Classical boundaries are moving : Slow control, On/Off line ...

■ Burst mode allows a fully software trigger !

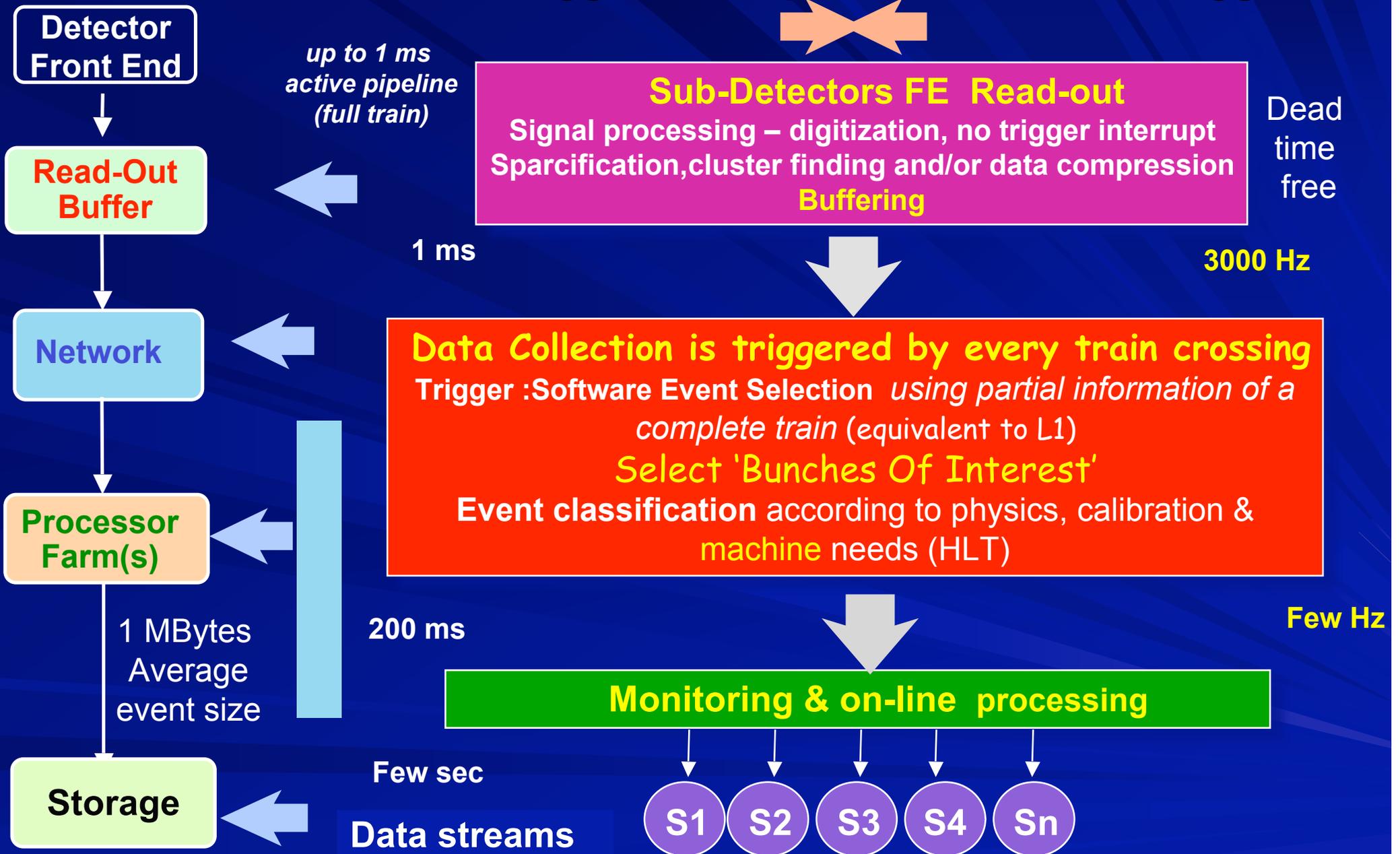
→ Flexible, scalable and cost effective...

→ Looks like the Ultimate Trigger: Take EVERYTHING & sort later !

→ GREAT! A sociological simplification!

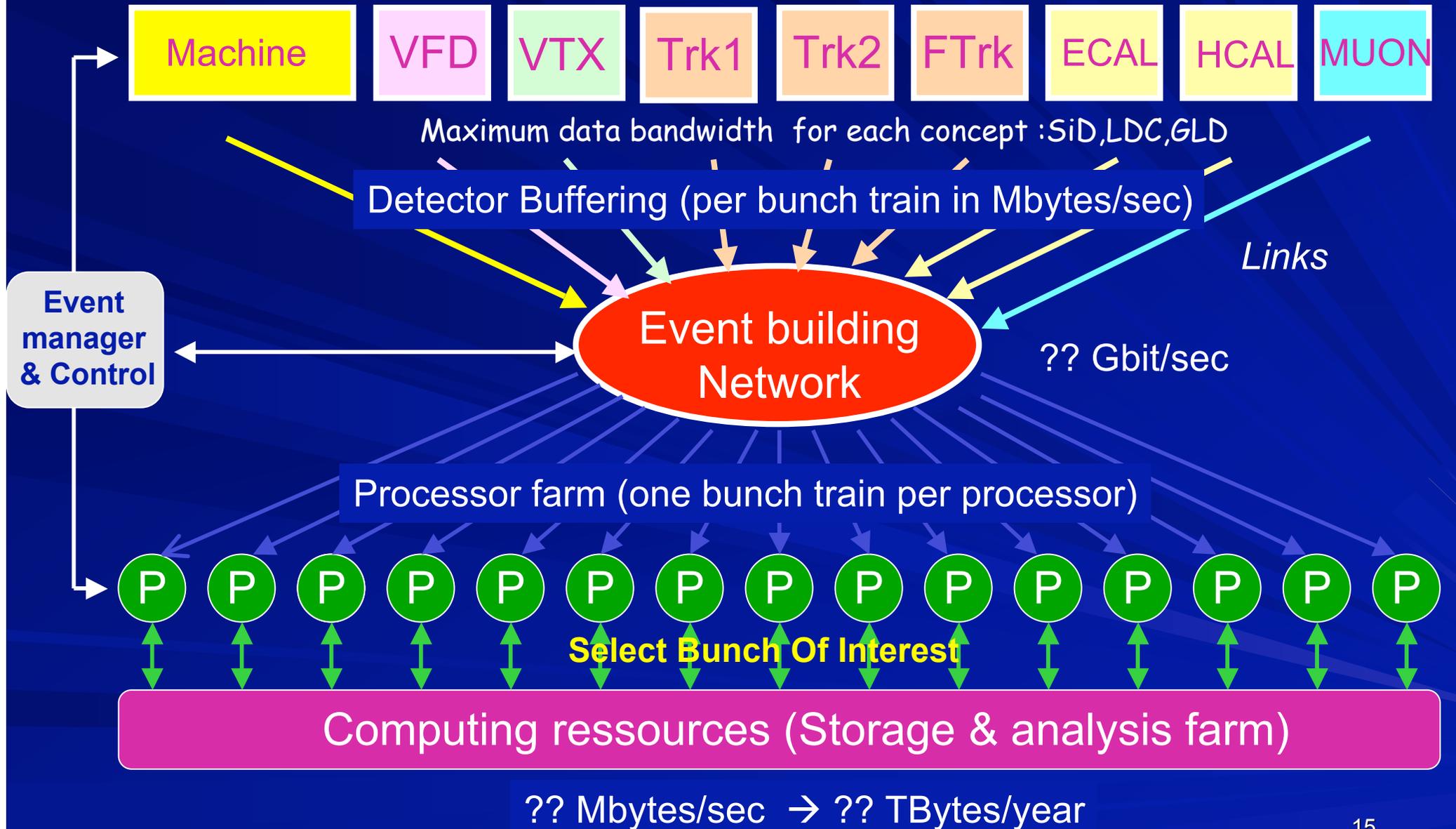
Data Flow

Software Trigger concept → No hardware trigger !



ILC DAQ conceptual (generic) Architecture (2005)

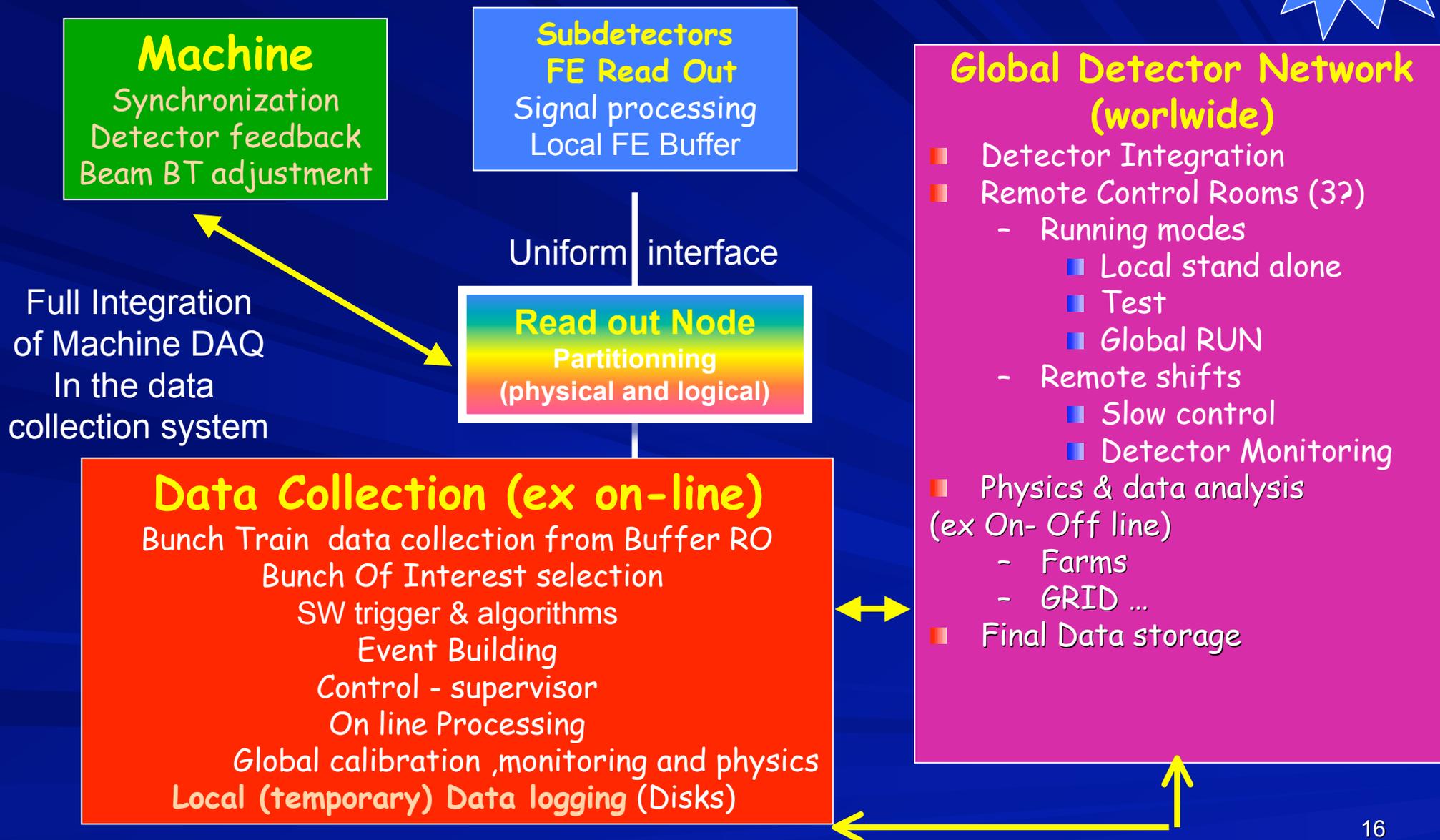
Detector Subsystems Channels count for each concept :SiD,LDC,GLD



About systems boundariesmoving due to !

→ evolution of technologies, sociology

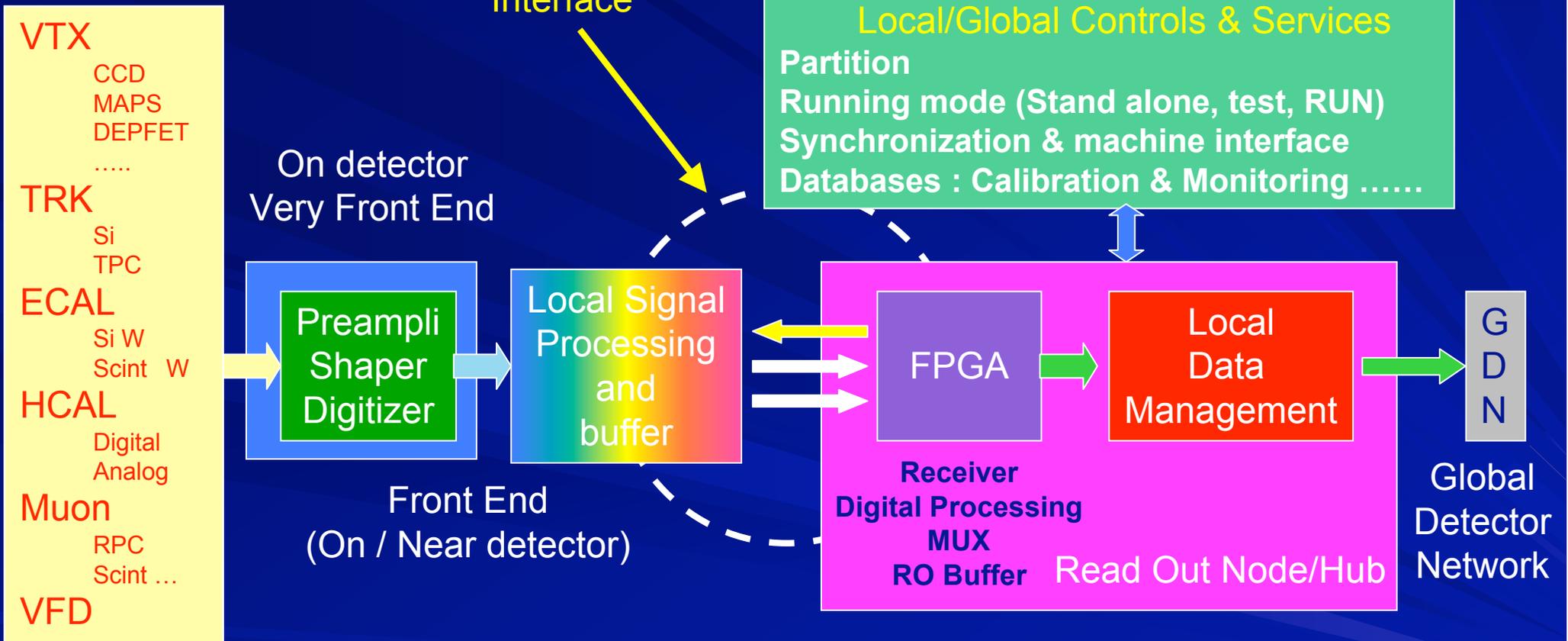
NEW !



Current view of a uniform RO architecture

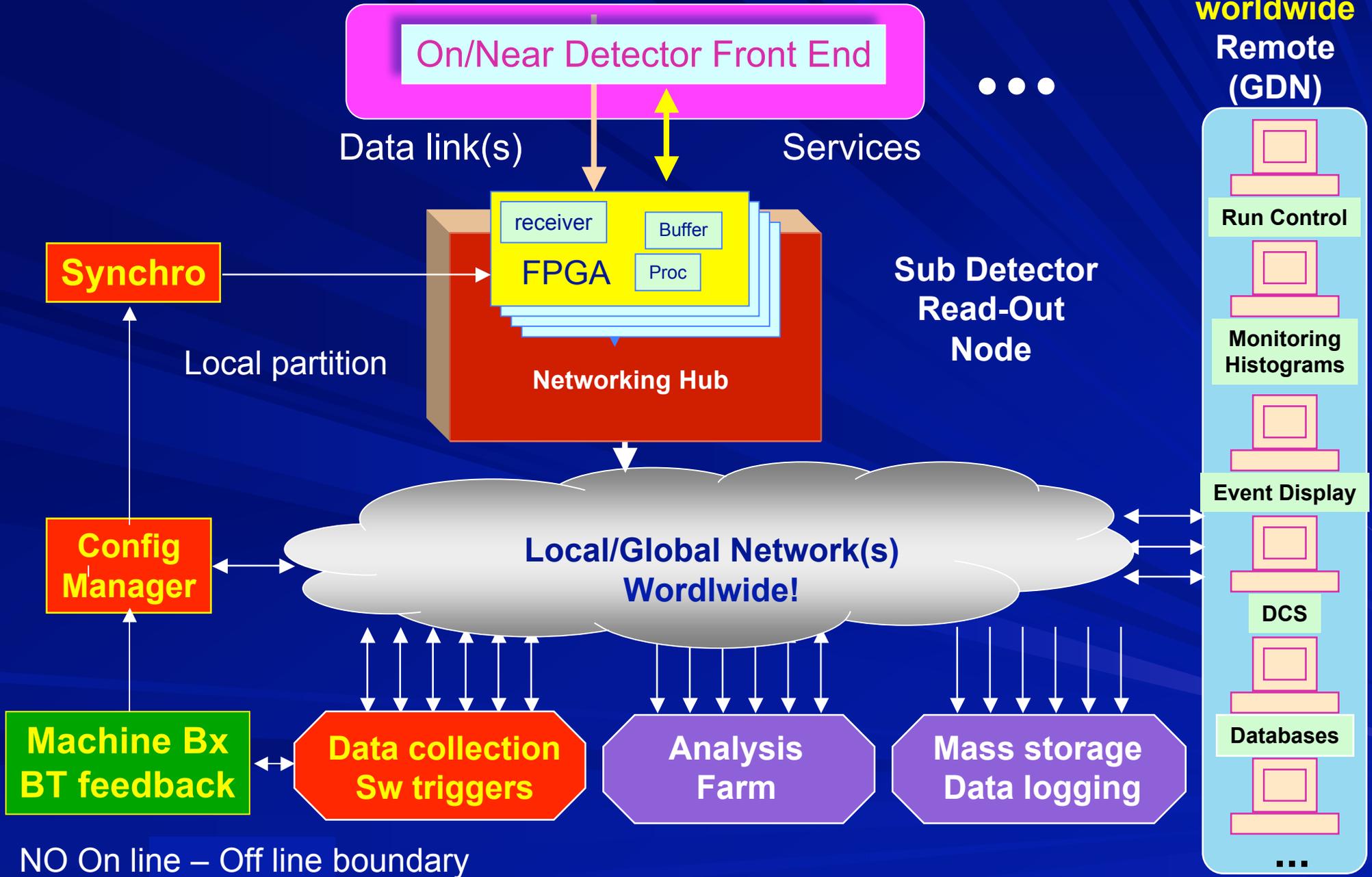
Sensor technology

Integration
To be studied!



*System On Chip

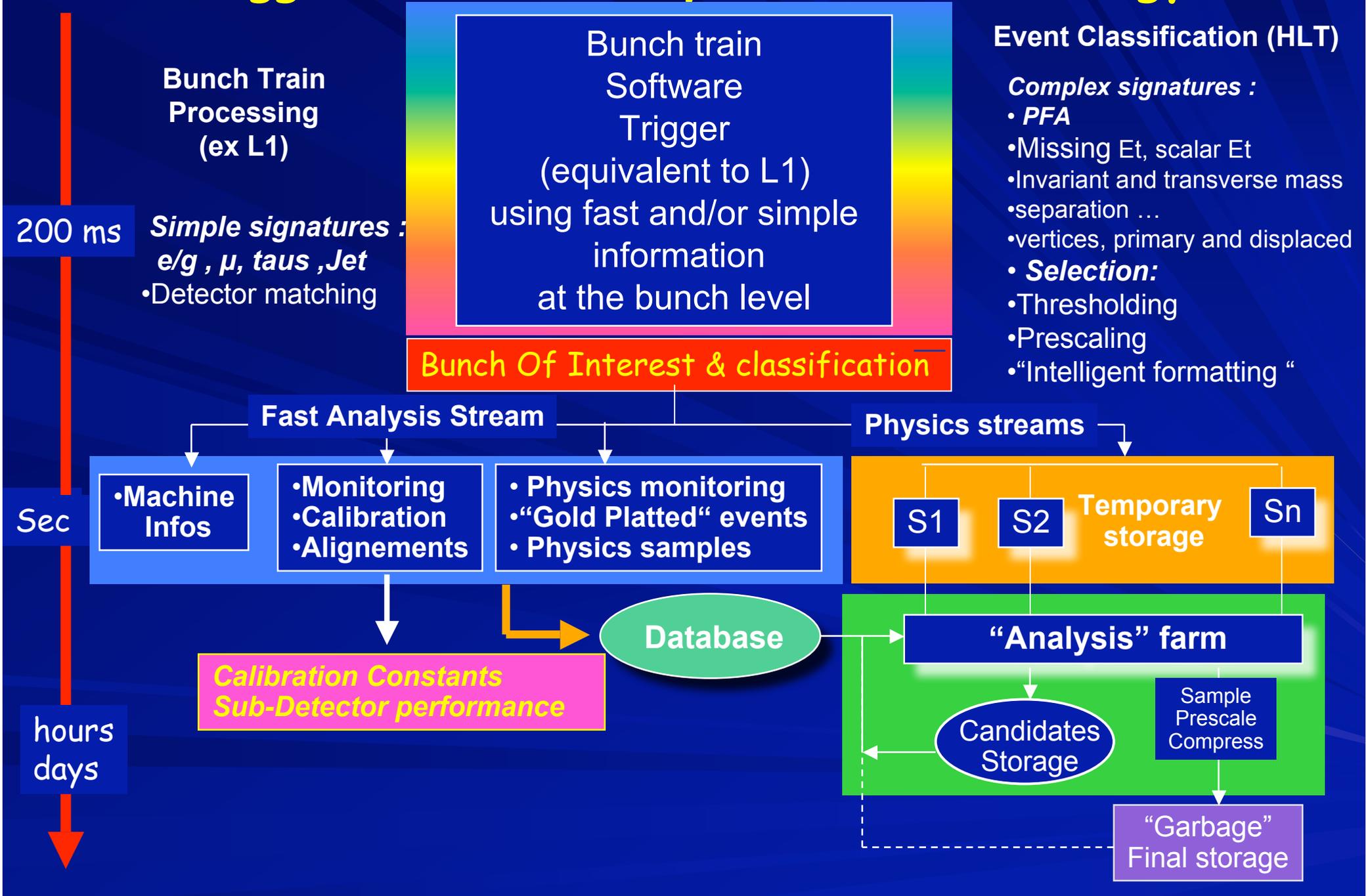
ILC 'today' Data Collection Network model



Tera scale system



Trigger & Event Analysis common strategy



ATCA in one page

(Advanced Telecommunications Computing Architecture)

Courtesy of R.Larsen (SLAC), R.Downing (FNAL), S.Dahwan (Yale), B.Martin (CERN)

ITER, AGATA

■ Coming from Telecom industry

- System throughput to 2 Tb/s
- System Availability 99.999% (~5 min/yr)
- Sponsored by the PIC Industrial Computer Manufacturers Grop (PICMG)

■ Basics elements and features

- Crate & subrack (Shelf) : Backplane, Shelf Manager, Air Cooling, Power, Entry Modules
 - "Shelf Manager" manages all module, crate, system utilities
- Module /Board (Blade) 14 to 16 units 8U !, 2 inch x 280 mm - 200W, vertical/horizontal
- Backplane : redundant dual star and full mesh (point to point)
 - Multiprotocols : Ethernet, Fiber channel, **PCI express**, Infiniband, rapidIO
 - Synchronization and Clock Interfaces buses (6)
- Rear Transition Module for user up 20 W
- Carrier (Daughter Card, Plug-in Module, Advanced Mezzanine Card)
- Software (Linux based)

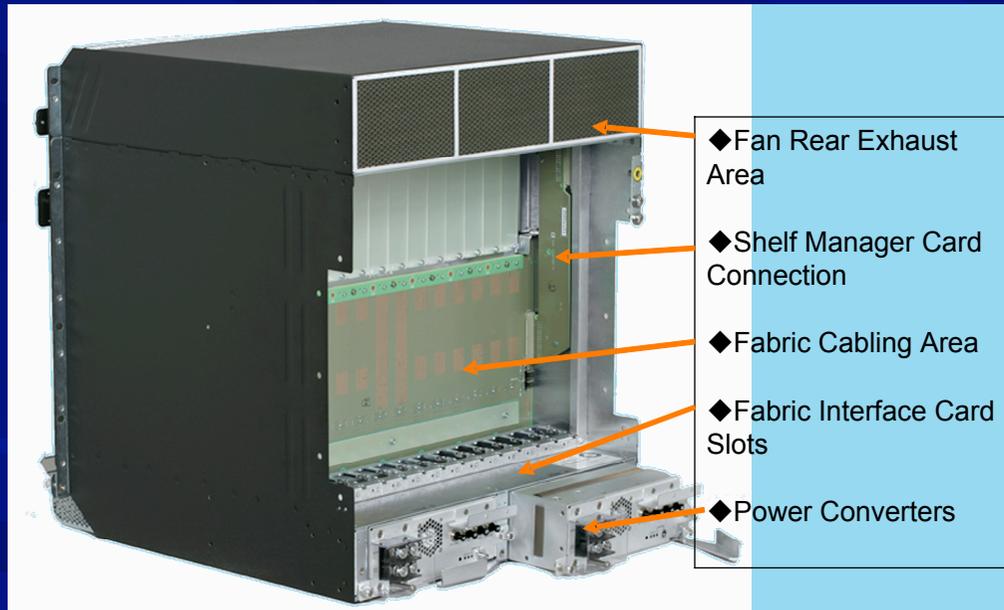
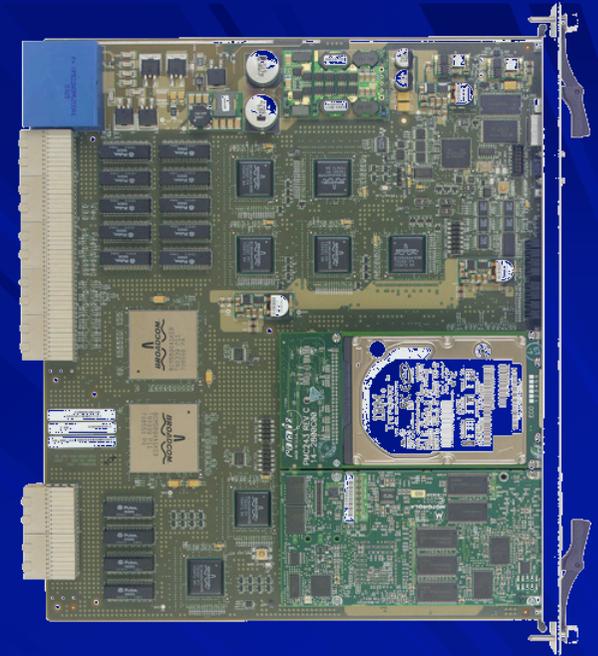
ATCA elements



- ✂ Dual Network Switch Module Locations
- ✂ Dual Star Fabric Connectors
- ✂ 48V DC Power Plugs
- ✂ Redundant Shelf Manager Cards
- ✂ Fan area

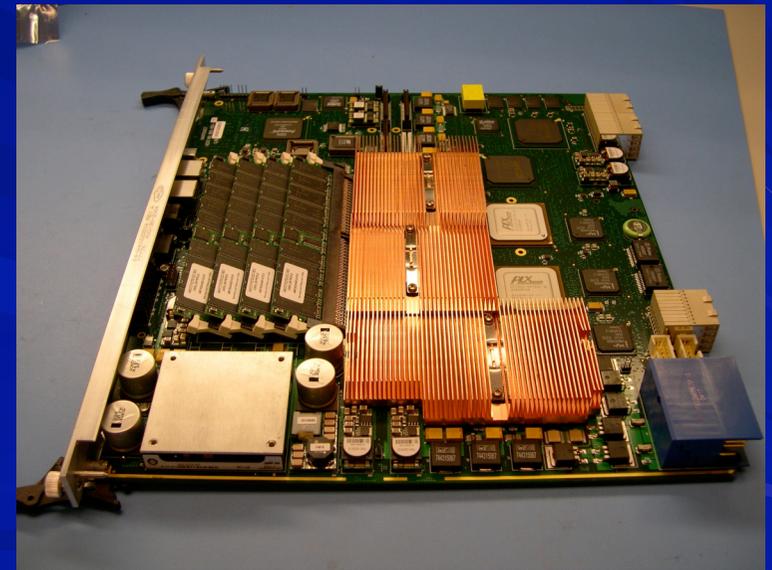
Shelf front

System Controller and Switch Blade



- ◆ Fan Rear Exhaust Area
- ◆ Shelf Manager Card Connection
- ◆ Fabric Cabling Area
- ◆ Fabric Interface Card Slots
- ◆ Power Converters

Shelf rear



System processor