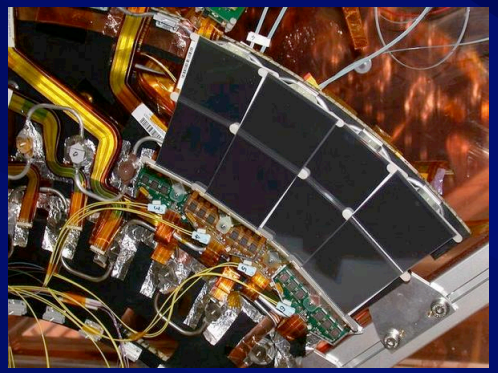
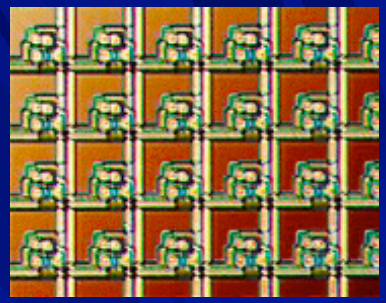
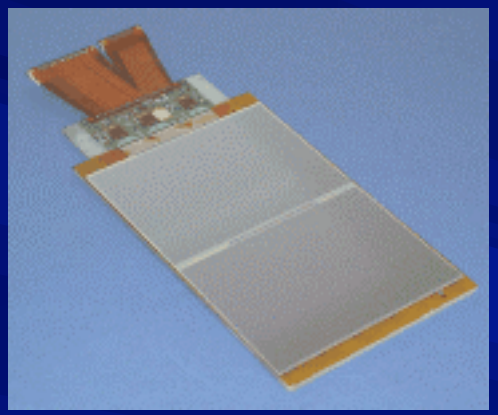
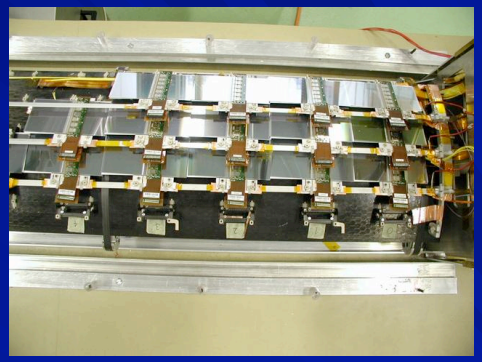




# Solid State Detectors





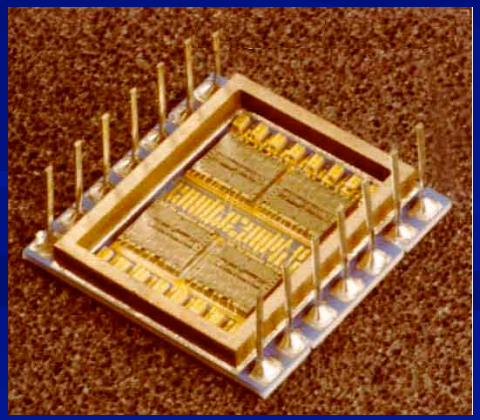

*By P. Le Dû*

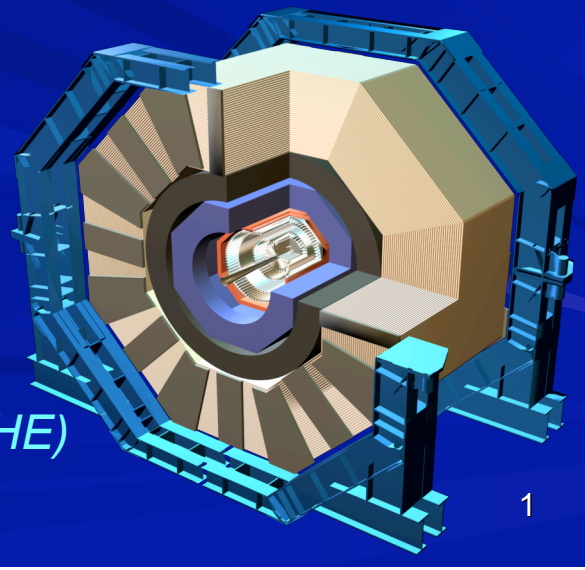
dapnia

cea

saclay

*patrick.le-du@cea.fr*




*Thanks to `*
*E. Hejne (CERN) & J.F. Genat (LPNHE)*

# About Scale ?

MILLI
MICRO
GIGA NANO
TERA PICO
PETA FEMTO
$10^{+18}$ EXA ATTO $10^{-18}$
$10^{+21}$ ZETTA ZEPTO
$10^{+24}$ YOTTA YOCTO

- We are going to ATTO

# LARGE INSTRUMENT NEEDED TO STUDY SMALLEST OBJECTS

$\gamma$ photon with $\lambda = 10^{-18}$ m has energy ~1 TeV

HIGH FREQUENCY IMAGING NEEDED (40 MHz FRAME RATE)

HIGH RESOLUTION IMAGING NEEDED (< 10 $\mu$m precision)

DIMENSIONS IMPOSED BY CONTAINMENT of HIGH ENERGY (TeV)

- From the Microsope ($10^{-6}$ m)
- to the ATTO scope ($10^{-18}$ m)

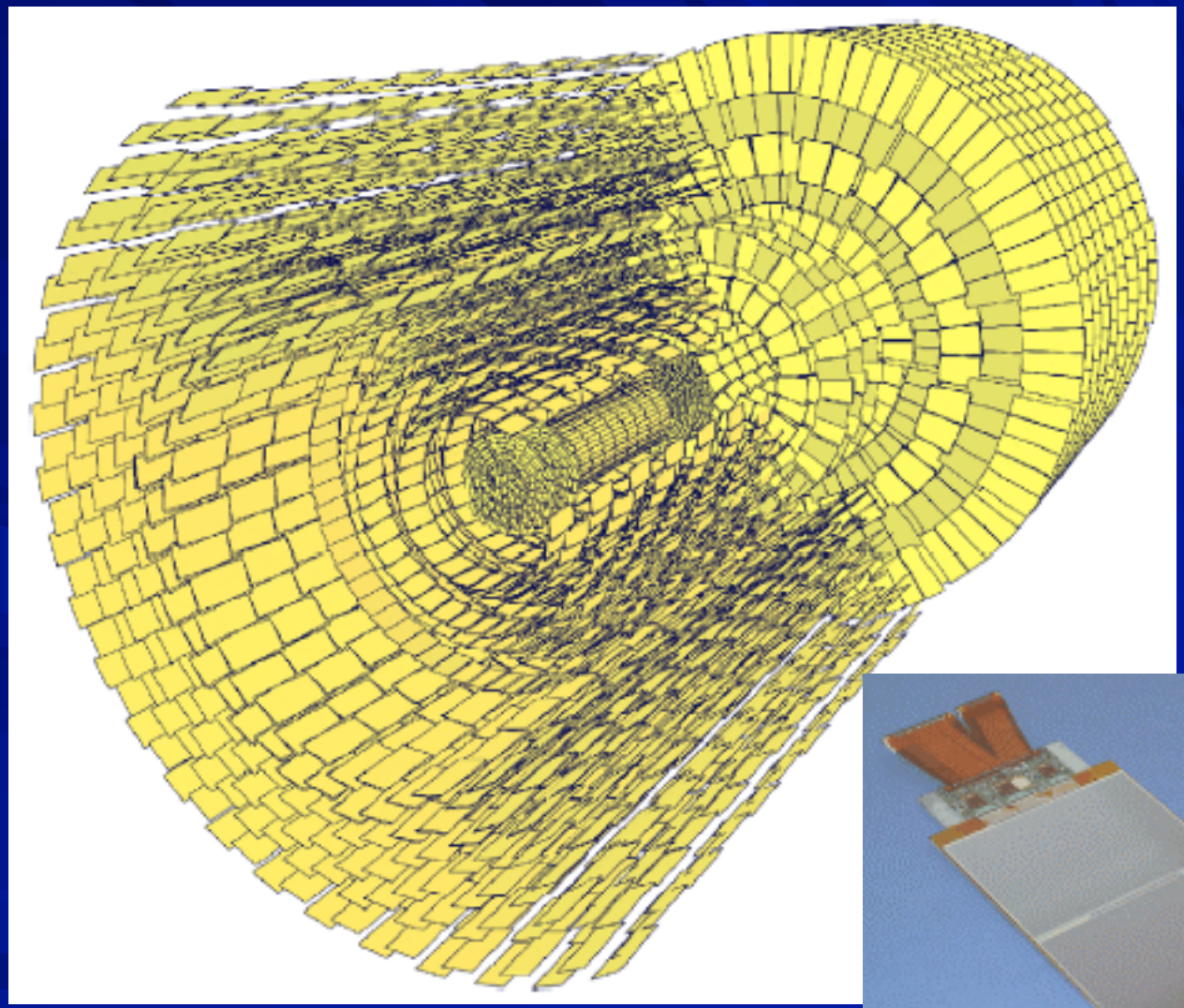
# COMPARISON ATLAS - CMS

*COURTESY W. van DONINCK*

# Principle & Performances

- Ionisation material: Si, Ge,GaAs, CdTe, CdZ …
- Charge collection by electric field
  - Drift, electrodes (CCD's)
  - Inverse polarized pn junctions
- Geometry :
    - Strips : localization, trackers
    - Pads : EM Calorimeters
    - Pixels : Vertex, Astrophysics, medical imaging
- Sensitivity MIP: 8000e- / 100 μm.
- Energy Resolution
  - 5-100eV @ 6 keV
  - 50 keV @ 5.5 MeV
  - 2 keV @ 1 MeV
- Transparency 0.1% $X_0$ / 100 μ
- Radiation hardness
  - O(100) kRad (CCD) - 50 Mrad (Hybrides)

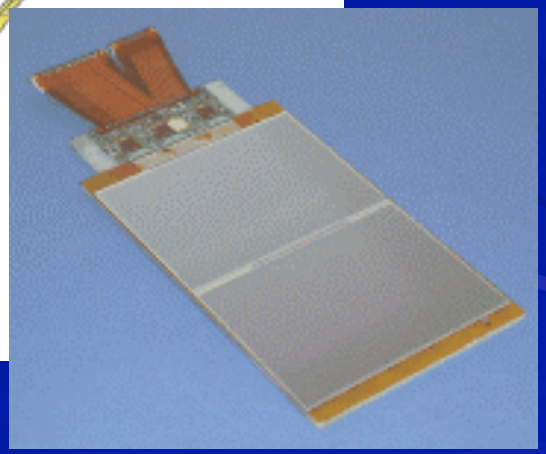
# CMS SILICON TRACKERS



16540 (15148stripd)

STRIP MODULES

(4-6 CHIPS x 128) ~$10^7$



PIXELS ~ $4 \times 10^7$

M.S. MENNEA et al.
NIM A 548 (2005) 391

# Example: ILC Strip detectors

Detector: High resistivity Silicium O(kΩ/cm)

Electronics: Deep Sub Micron Silicium (DSM)

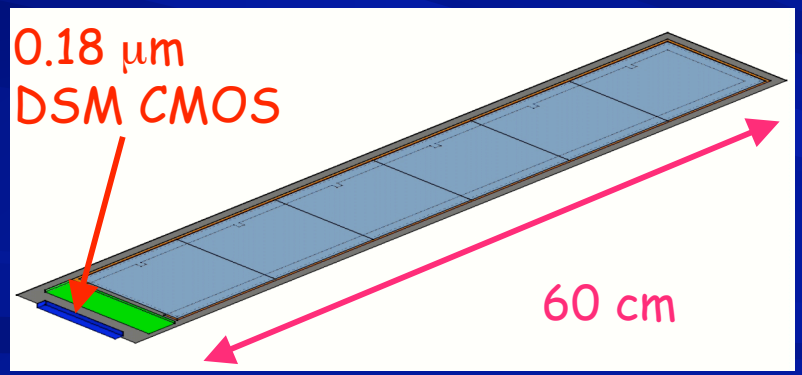
*Resolution:* *~O(10)μm (pitch > 100 μm)*

*Read Out:* *Long Shaping O(μs) -> charge*

*Short Schaping O(20 ns) -> time*

*Transparency:* *0.1 $X_0$ / 100 μm*

*Alice, CMS, ILC*

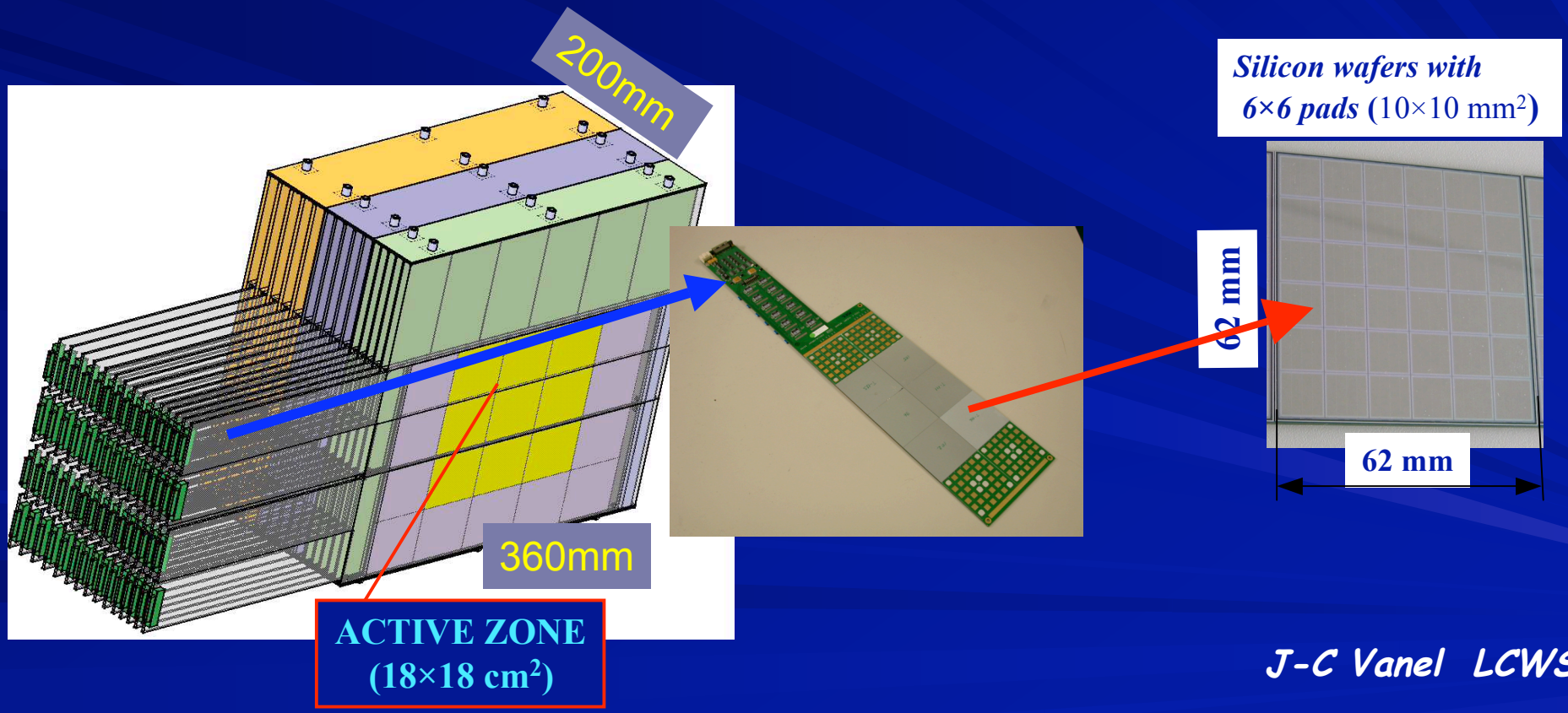



ILC:
SiLC Detector Ladder
with FE Electronics

*Perspectives: Wafers 12", amincissement (100-200 μm)*
*Electronique basse puissance DSM/SiGe, timing.*

# Electromagnetic Calorimetry @ ILC

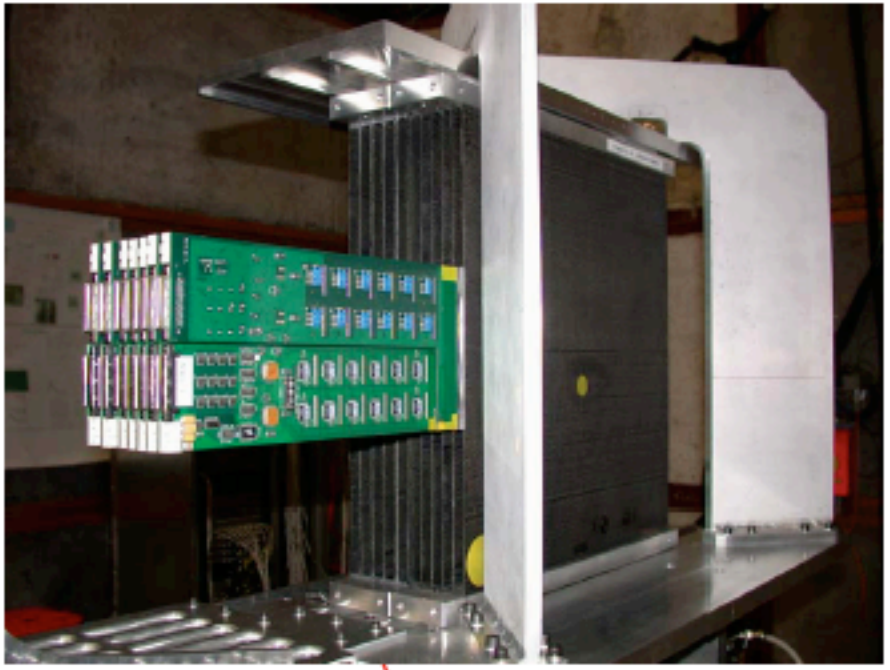
Absorber: W
Read-Out: Silicium pads 1cm² **(diodes PIN)**
Électronics AMS 0.35 μm, R: amorphous Si, C: $Si_3N_4$
32 $10^6$ channels
Optimazed for separation photons/charged tracks
$\Delta E/E$ = 11 to 14% / sqrt(E)

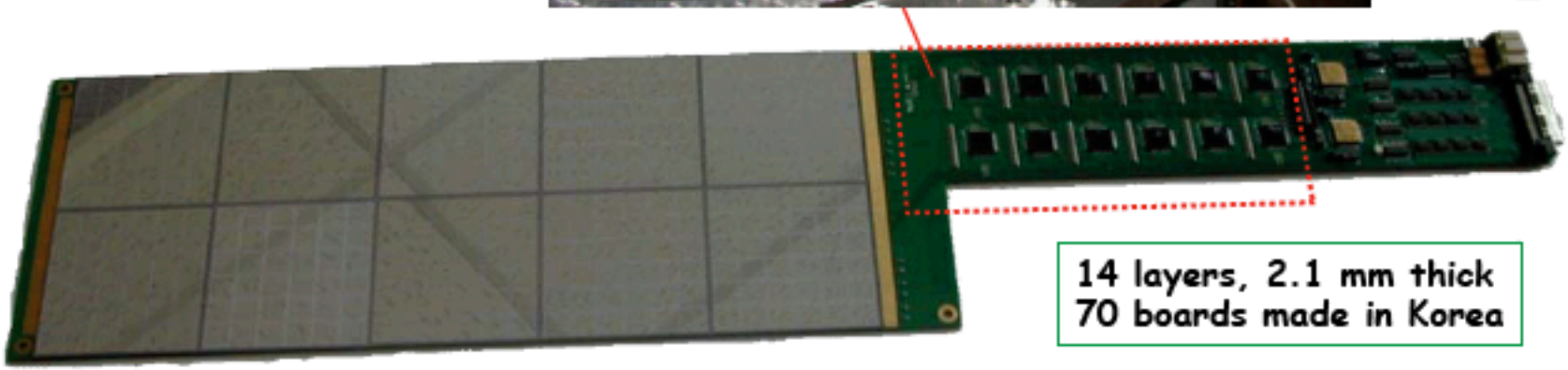


# Prototype 2007

## CALICE W-Si calorimeter

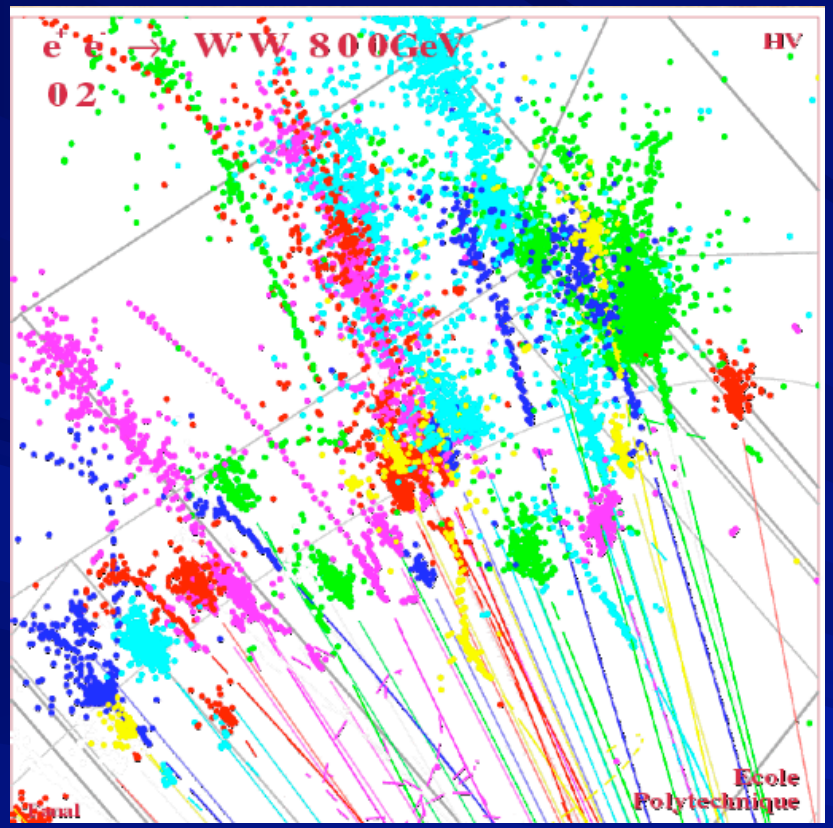
- "Imaging calorimeter"
  - 30 layers W-Si
  - 1 cm² Si PADS

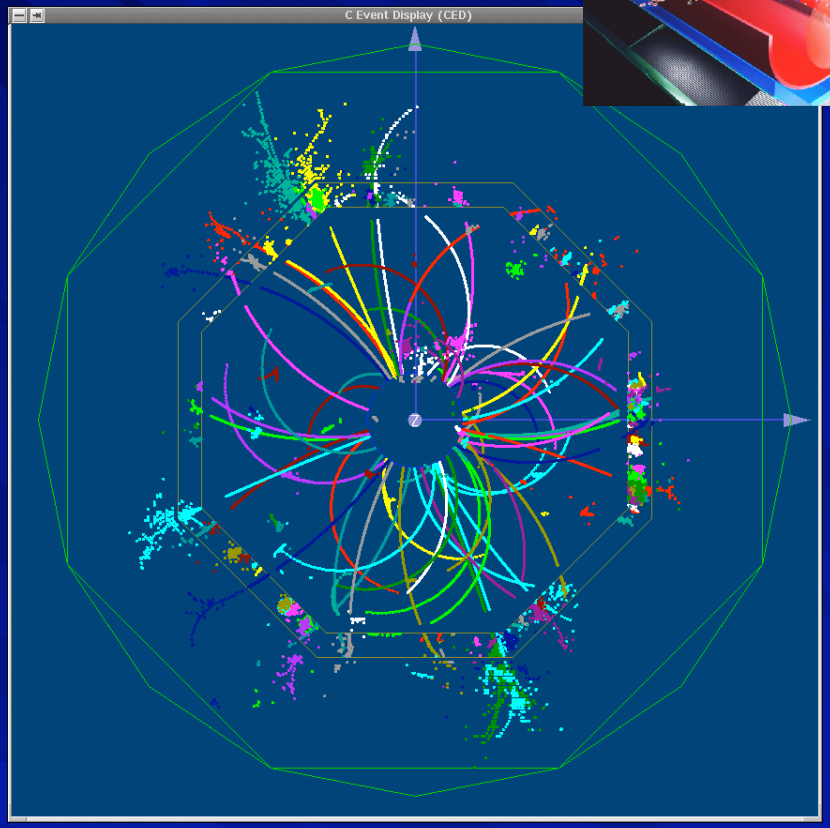


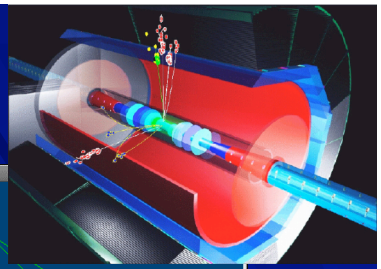


14 layers, 2.1 mm thick
70 boards made in Korea

# ILC Particle Flow Algorithm (PFA)



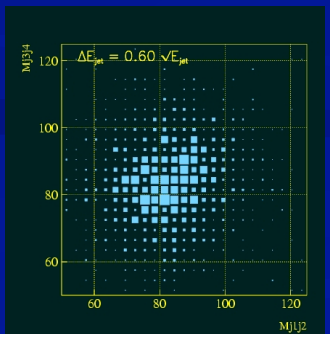



PFA simulation

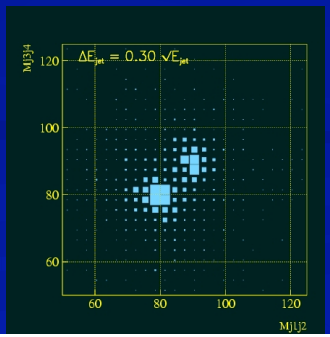
e.g. tt event in LDC

*LEP-like resolution*

$60\%\sqrt{E}$




***2 Jets separation***

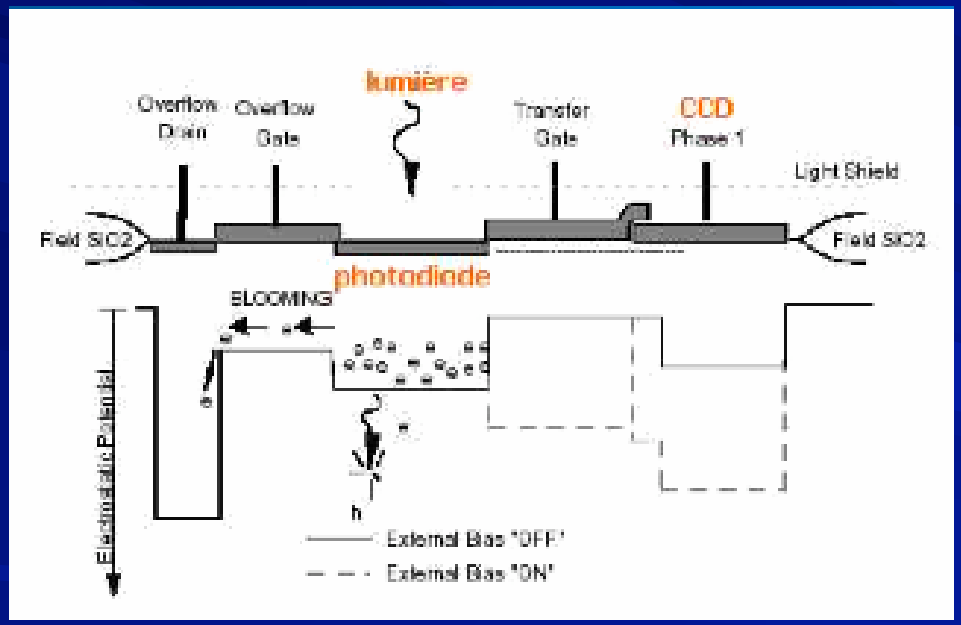



*ILC goal*

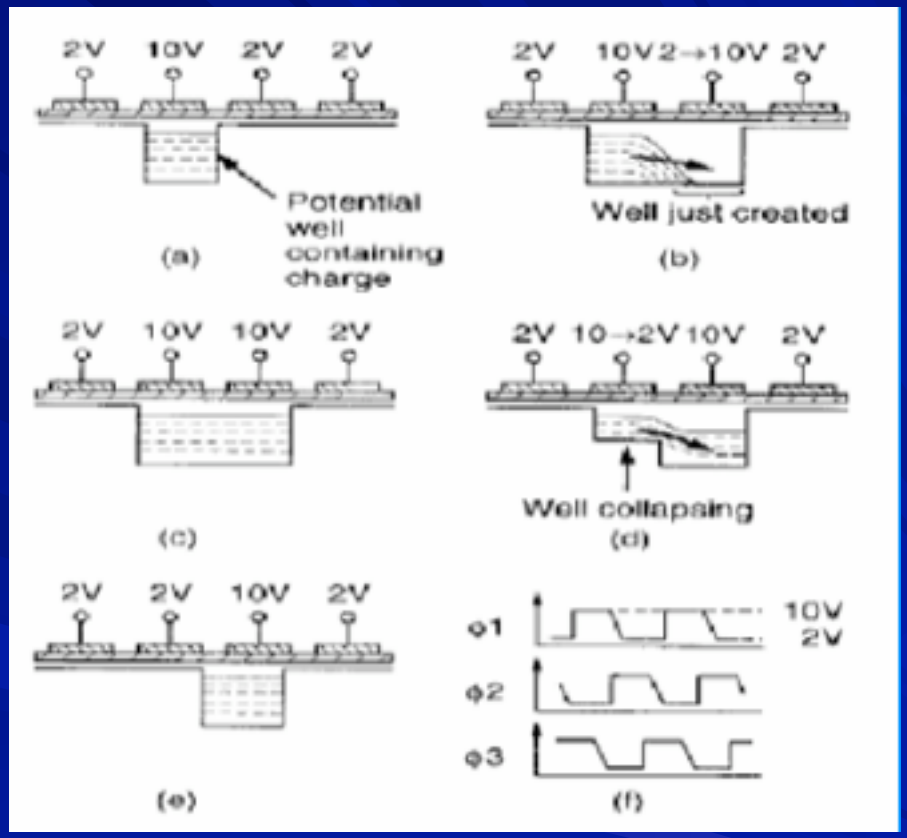
$30\%\sqrt{E}$

# Solid state Arrays: CCD

- Principle
  - Array of small Photodiodes
  - Light integration
  - Transfer thru the matrix

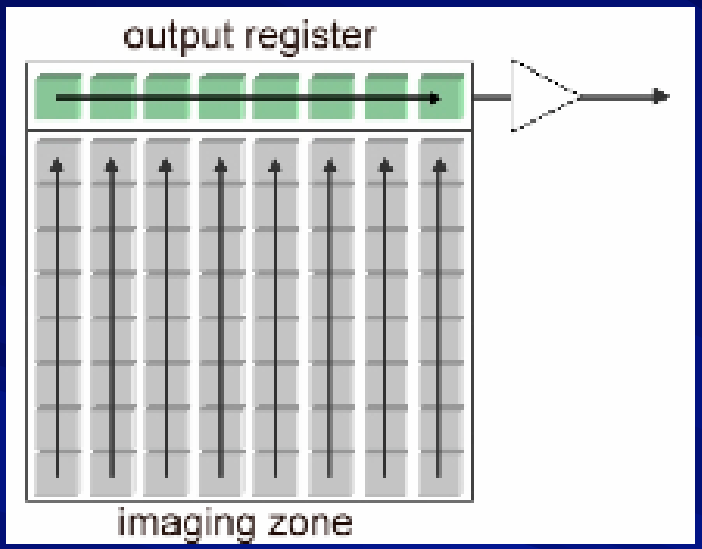


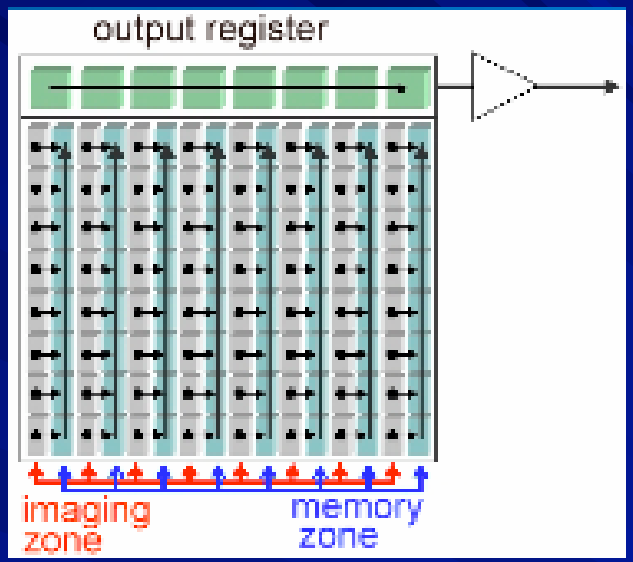

Detail of a pixel and operation principle

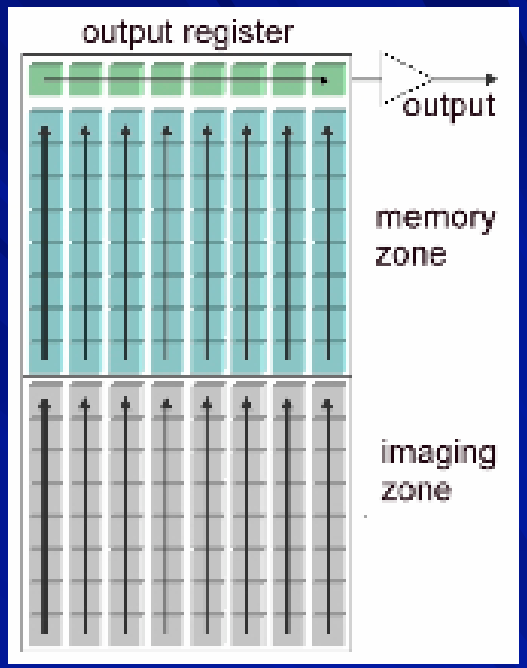



Transfer from well to well (pixel)
2 phases clocked gates

# CCD Readout architecture




Full frame transfer
*Smearing :*
*needs a shutter*
*but*
*simpler chip*

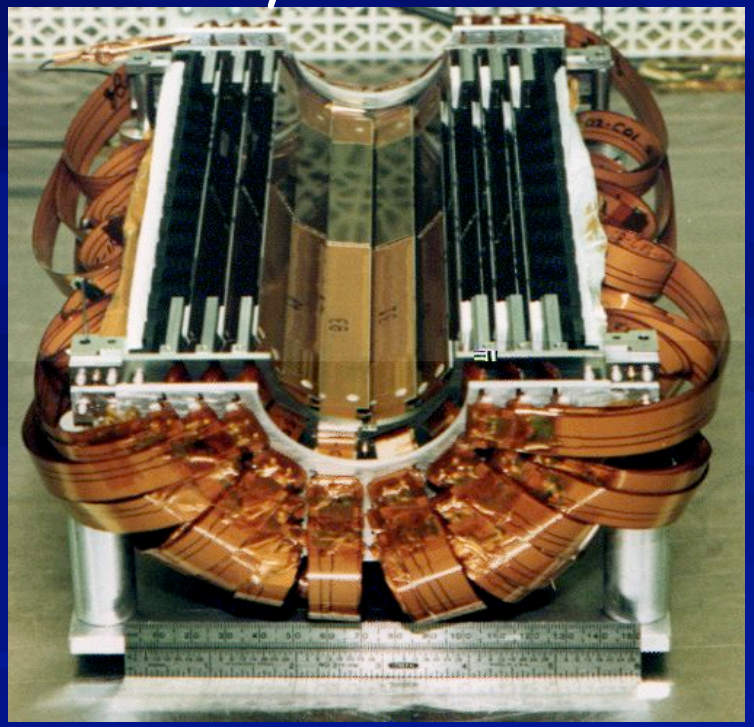
interline transfer
*Fast frame transfer*

Frame transfer
*Long exposures*

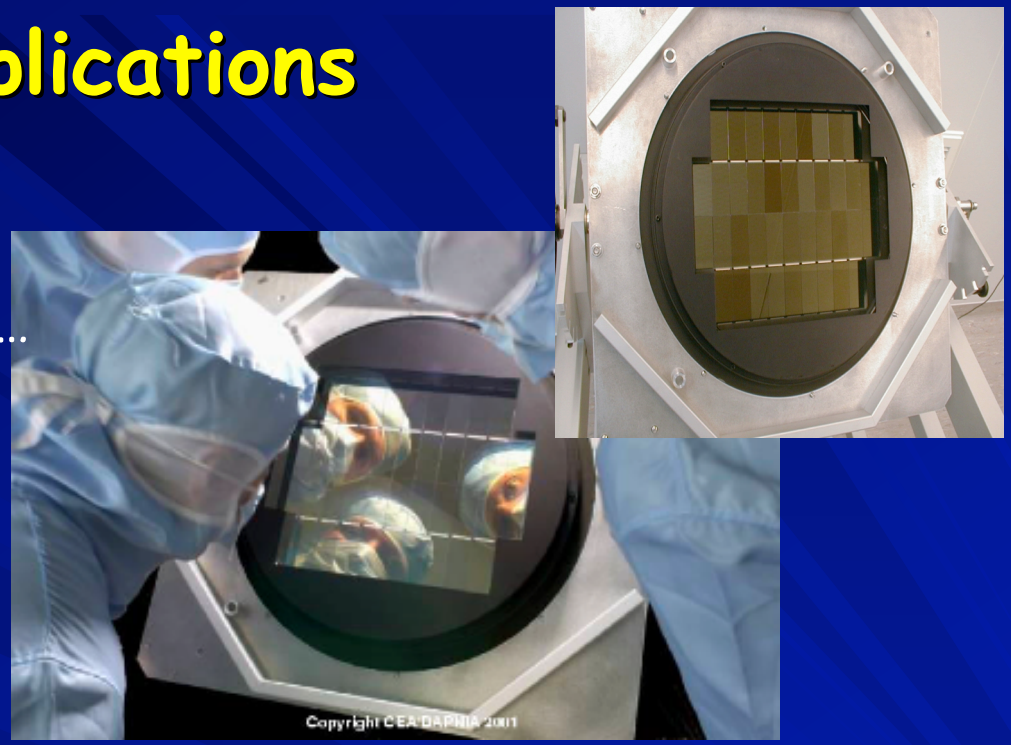
Typical R/O speed = 5 MHz
⇒ FFT at 5 frames /s
for a1024x1024 pixel CCD

# CCD Applications

- Consumer media equipment
- Scientific :
  - spectrometry, biomedical imaging…
- Astronomy



CCDs du SLAC Linear Collider Detector (SLD) 1998



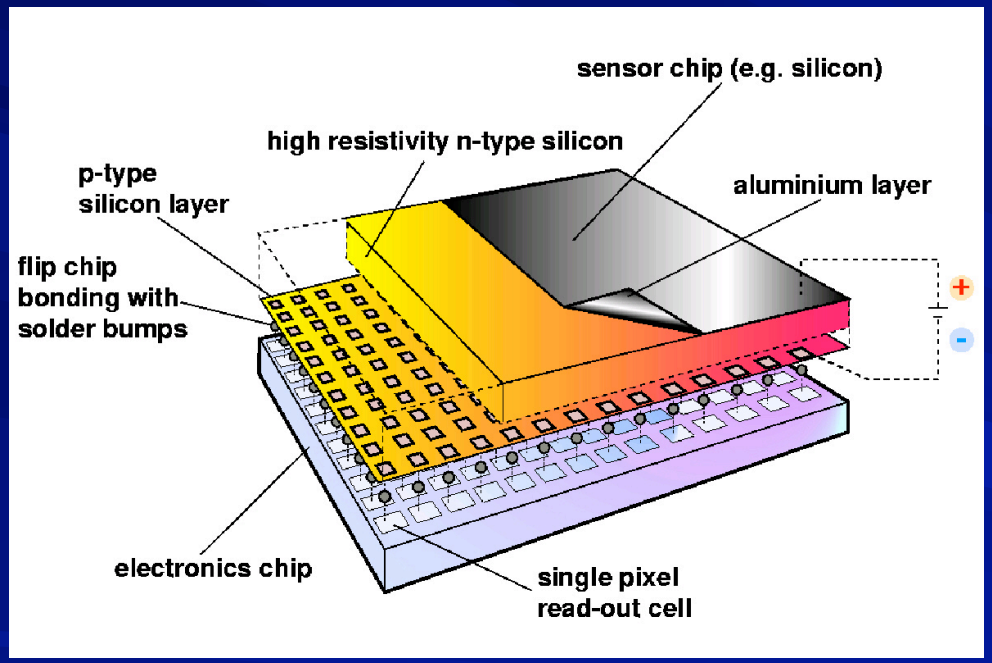

The focal plane of MEGACAM (2001)
Telescope CFH (Hawaii)

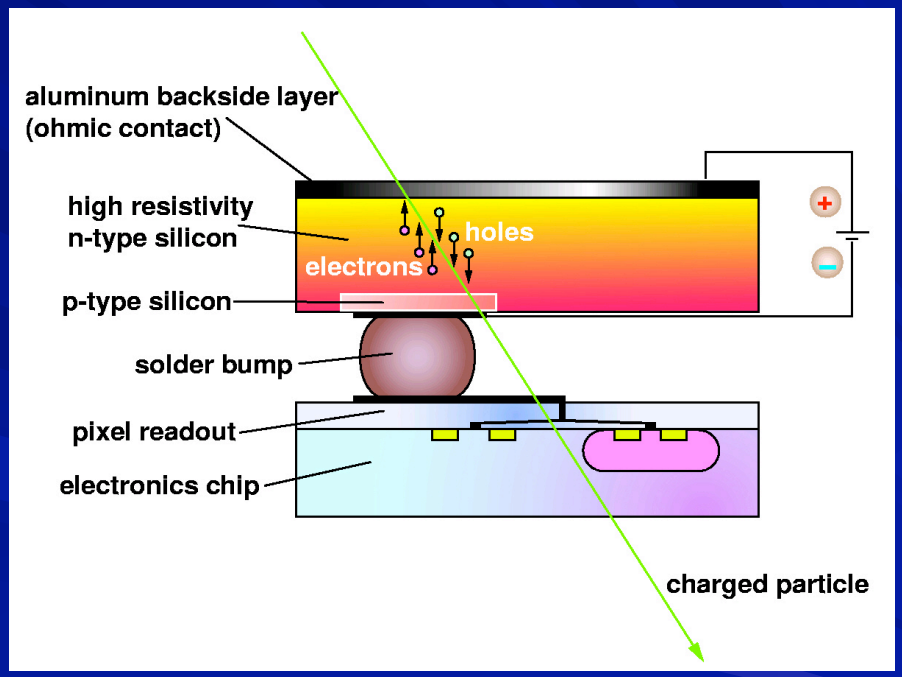
- 40 CCD's
- e2v Technologies model CCD42-90
- 2048 x 4612 pixels (13.5 x 13.5 µm)
- Back iluminated (λ350 to 1000 nm)
- Cooling at -120°C
- 400 Mpixel, 30 sec readout
- 80 Go of data / night

# HYBRID PIXEL DETECTORS

PERFECT APPROACH for HIGH RATE PARTICLE PHYSICS (LHC)
FULLY PARALLEL SIGNAL & INFORMATION PROCESSING

MANY OTHER APPLICATIONS: SINGLE PHOTON IMAGING

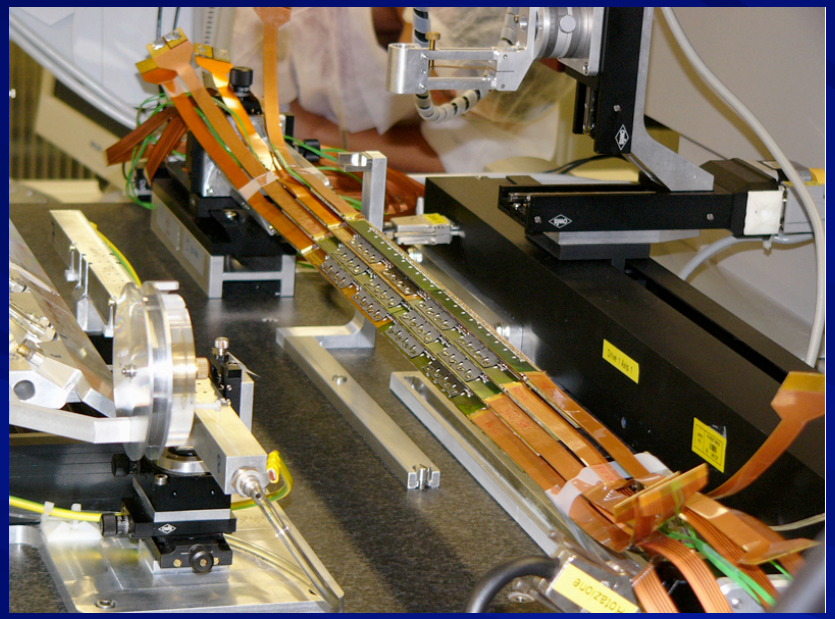



SYNCHROTRON LIGHT IMAGING
MEDICAL X-RAY IMAGING

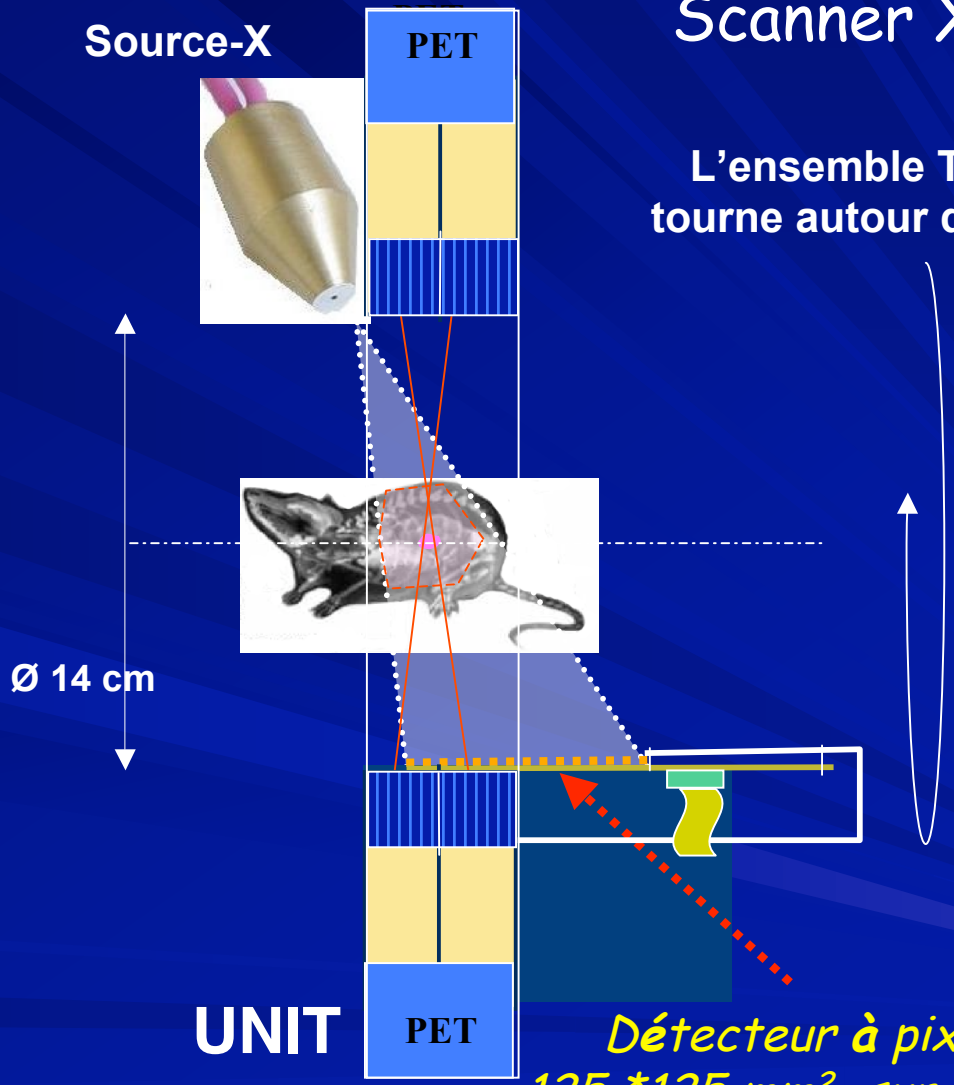
# Applications

PE Tomography
+
Scanner X



LHC ALICE

Pixel detector



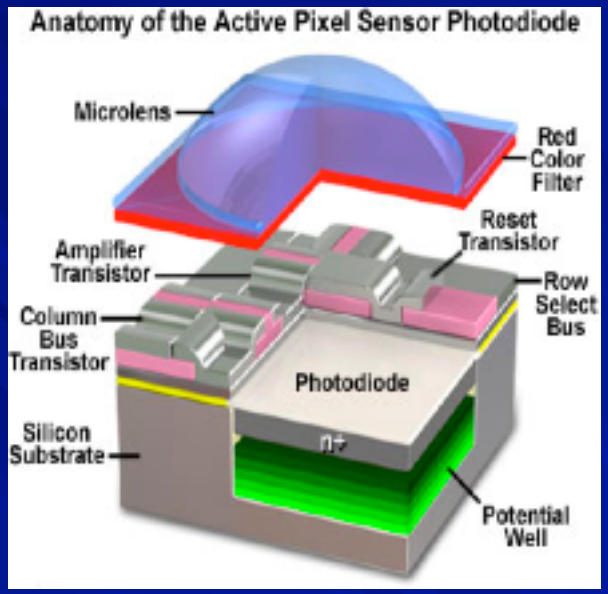

**L'ensemble TEP et CT tourne autour de la souris**

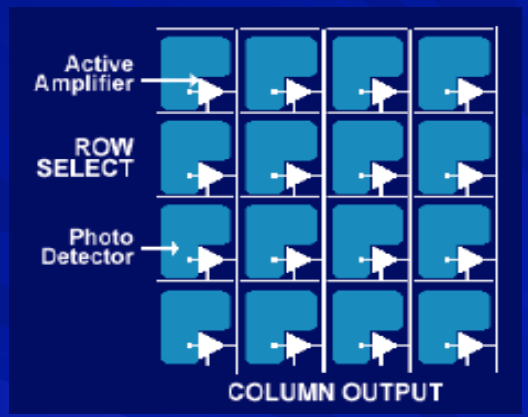
**UNIT**

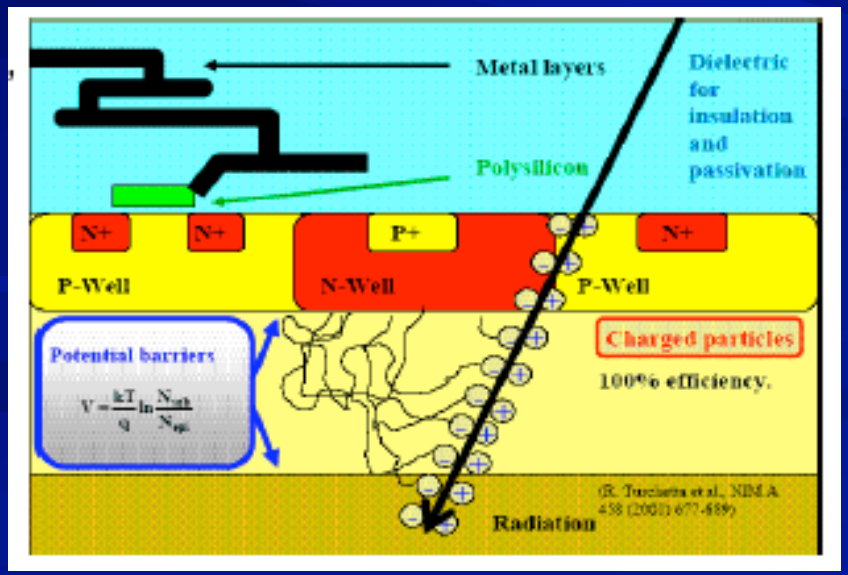
*Détecteur à pixels CdTe*
*125 *125 mm² sur 6,4 x 6.4cm*
*(2006)*

# Monolithic Active Pixel Sensor (MAPS)

- CMOS Imager
- Classical CMOS processing
  - Circuit similar to webcam (low cost)
- Matrix of Pixels = photodiodes + preamp and gates
- Rapid read-out by individual random addressing
- Electronics associated to each pixel




10 µm

**Avantages :**

-System-on-chip : monolithic device

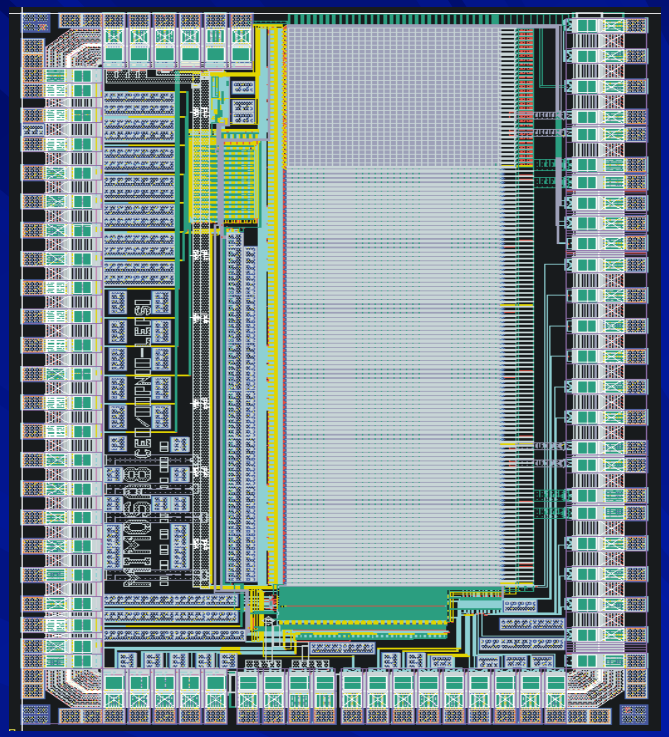
-Sensitive Volume = epitaxial layer

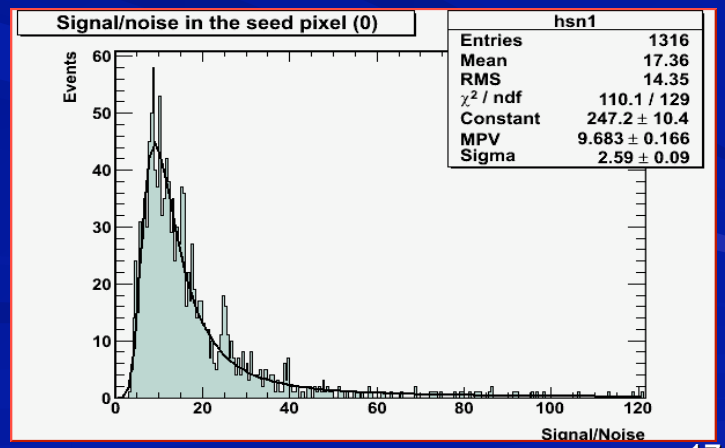
-Standard Techno -> « Low cost»

-Radiation tolerant aux radiations > CCD

# MAPS : system-on-chip

- Development of series of « Mimosa »
  - Collaboration between IN2P3/IRES (Strasbourg)
- Mimosa 8 (DAPNIA)
  - TSMC 0.25µm digital
  - ~6µm epitaxial layer
  - 32*128 pixels (25µm pitch)
  - on-pixel CDS plus column discriminator.





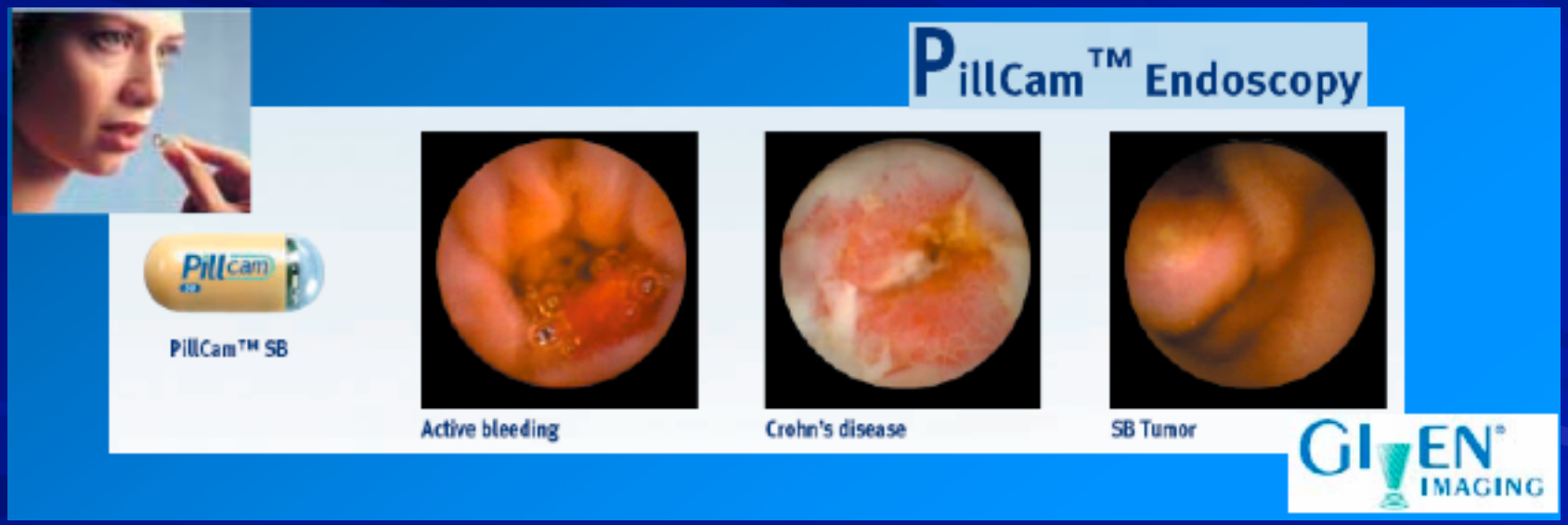

S/N pour MIPs: ~10
Detection efficiency > 98%
Résolution spatiale attendue: < 1.5 µm

# APS Main parameters and performances

- Sensitivity : 1 to 2 V/lux-sec
- Dark noise : 10 mV/s @ 60°C
- Dynamic : 40 to 60dB (depends from ADC on chip)
- Speed : up to 200 frames/s in VGA format (640x480 pix)
- Size : up to •”4000 x 4000 pix (3 x 3 µm•)
- Low cost, standard IC processing, high yield
- But :Low efficiency : poor fill factor (microlensesimprove)

# APS applications

- Camera "on chip"
- Low cost still camera, web cam, process and shape control
- Quality and performances steadily improve
- Medical applications : dental X ray , endoscopy

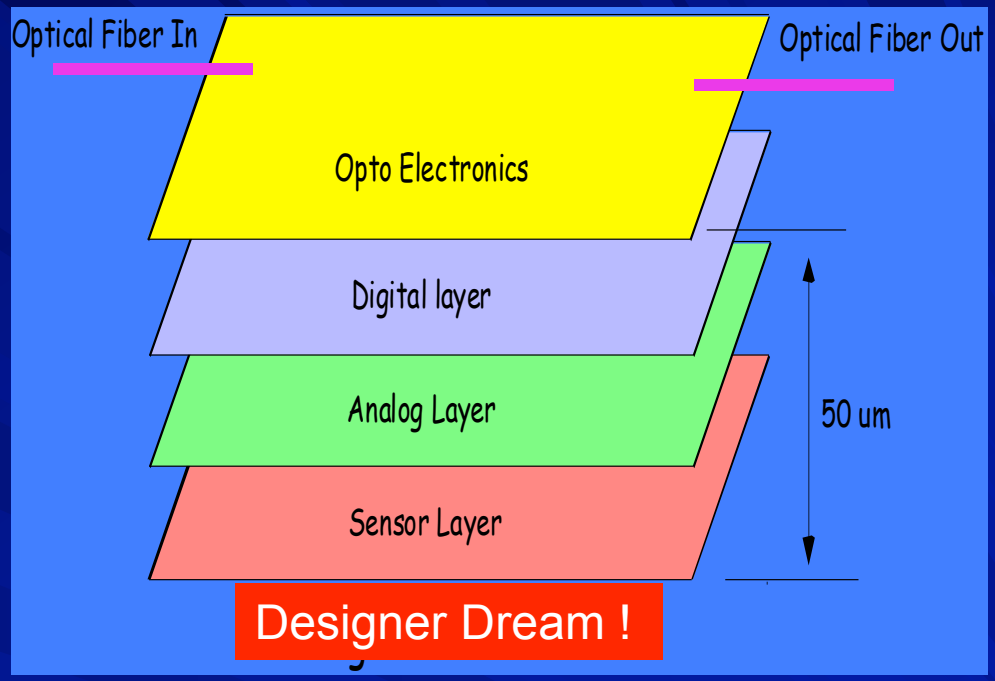


# The Future

3D chip

# What is 3D Circuit Integration ?

- A 3D chip is comprised of 2 or more layers of semiconductor devices which have been thinned, bonded together, and interconnected to form a "monolithic" circuit.
- Frequently, the layers (also called tiers) are comprised of devices made in different technologies.
- The move to 3D is being driven by industry.
  - Going 3D reduces trace length, Reduces R, L, C
  - Improves speed
  - Reduces interconnect power, crosstalk
  - Reduces chip size
  - Processing for each layer can be optimized




Key Enabling Technologies

- Wafer thinning (to <25μm)
  - Grinding, lapping, etching, and chemical polishing
- Precision alignment
  - Better than 1 micron
- Bonding of thinned wafers
- Through wafer via formation and metallization

# Application : ILC Vertex detector

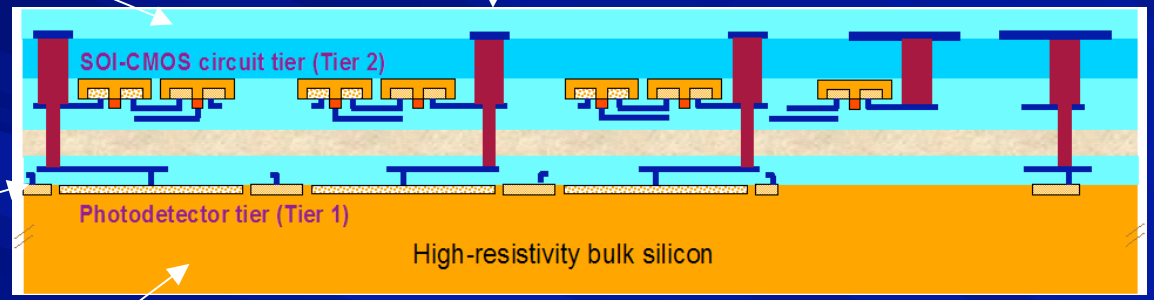
REQUIREMENTS

- Very low mass - 0.1% rl per layer
- Resolution < 5 microns in x,y
- Time resolution < 50 microseconds
- Very low power < 20 W (with 1/200 duty factor)
- Inner layer at ~ 1.5 cm radius

CMOS circuitry

Interlayer vias

Wafer bond oxide, intermetallic or epoxy




(MIT-LL)

high resistivity silicon wafer, Thinned to 50-100 microns

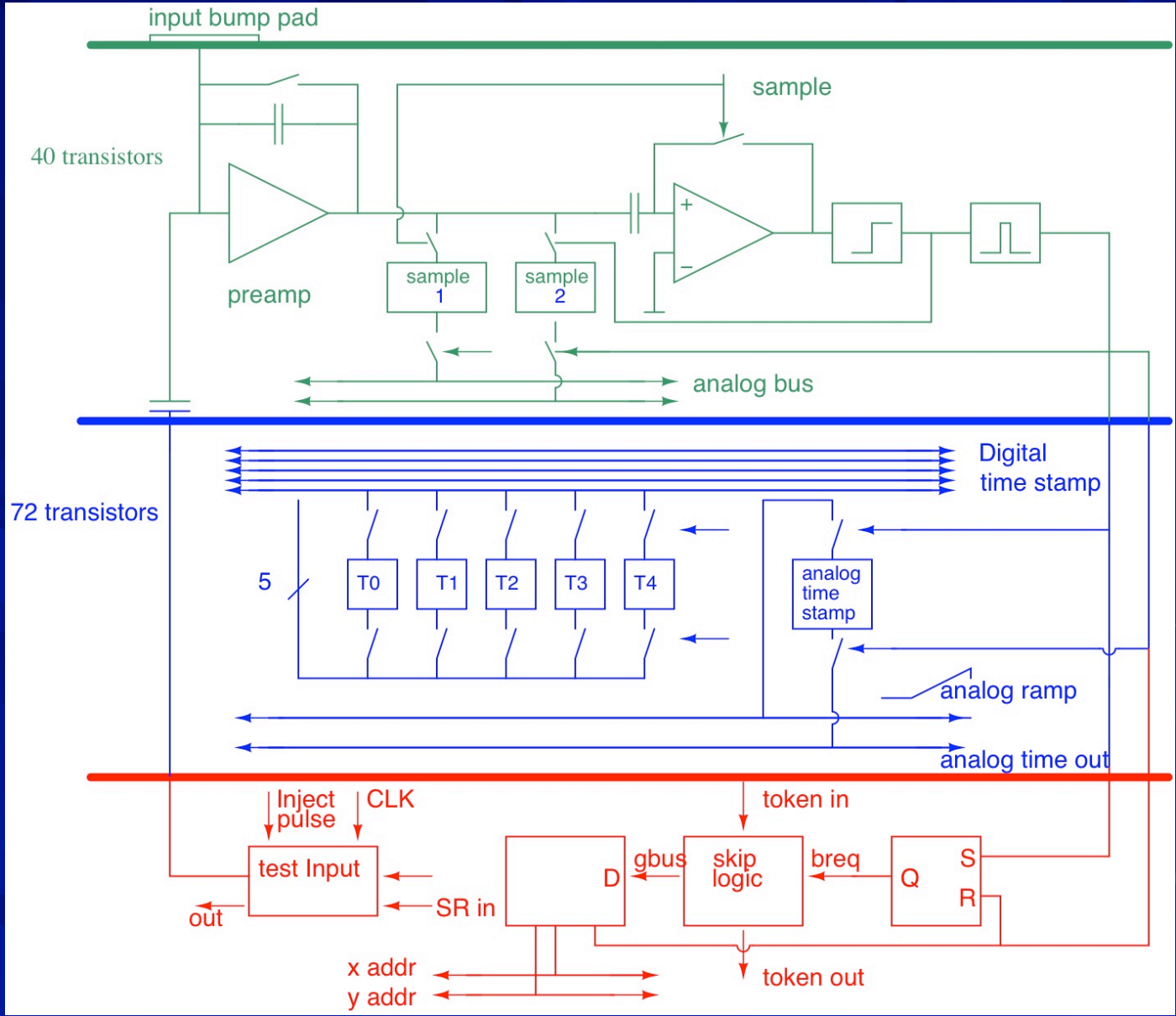
Active edge processing

Backside implanted after thinning, before frontside wafer processing

# ILC pixel Chip design (MIT-FNAL)

Correlated double sample
Noise ~ 35 e- (??)
Adjustable disc. threshold
Few hundred nA/pixel
Most bias currents (times) adjustable

Analog and digital time stamps
Analog resolution (?)

Sparse readout
Individual kill/inject

3 vias / pixel