Performance Measurement of the Upgraded DØ Central Track Trigger

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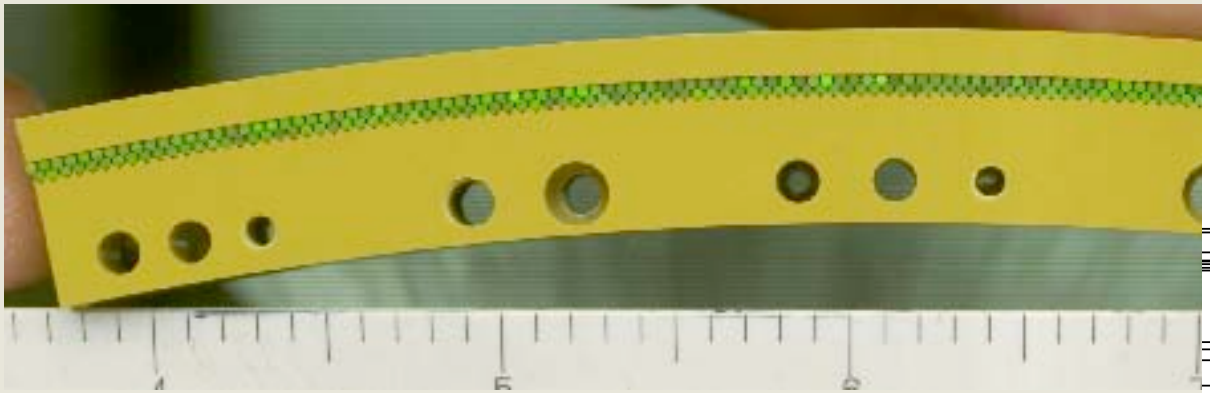
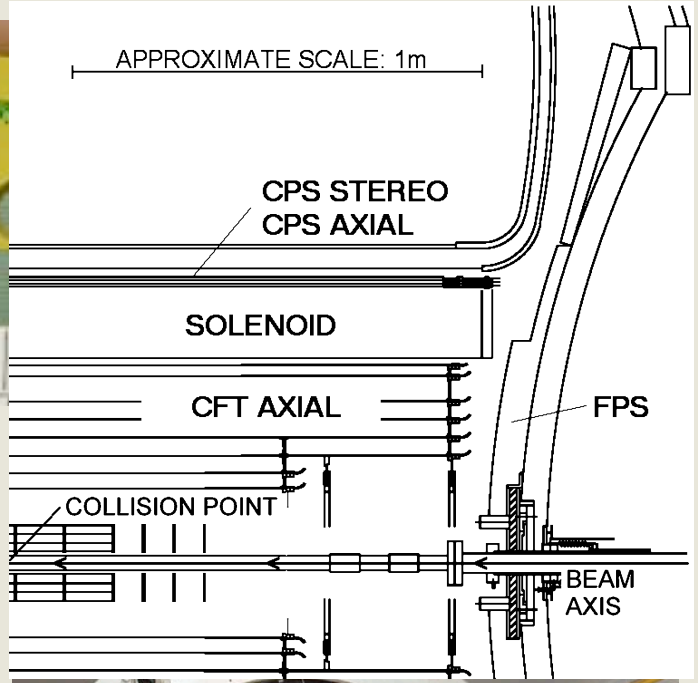
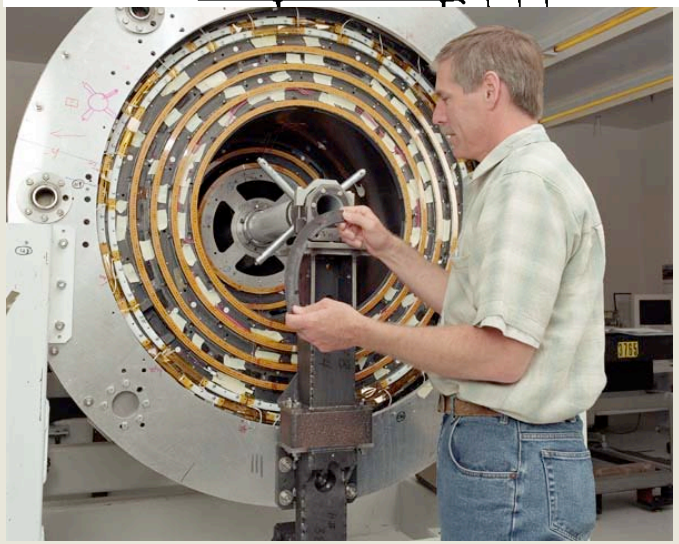
Central Fiber Tracker (CFT)



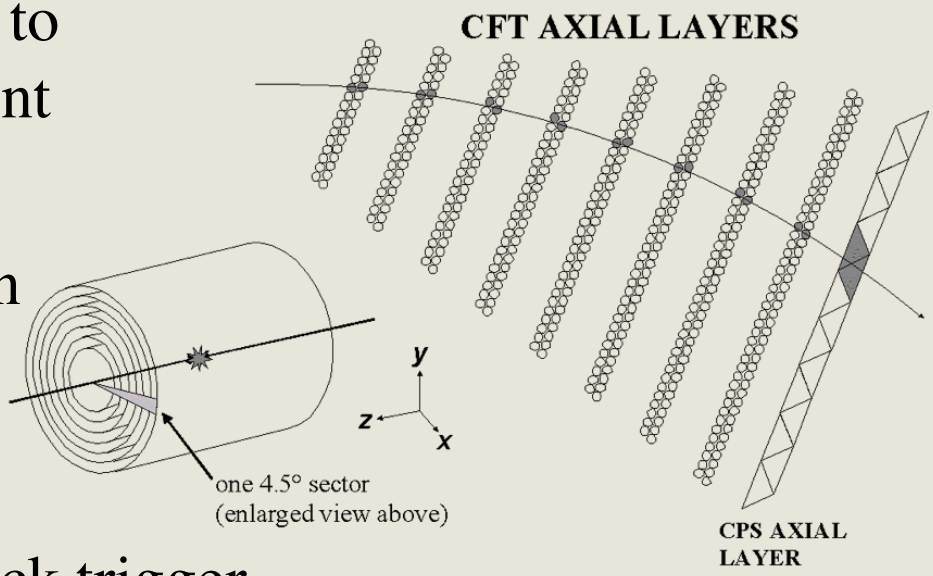


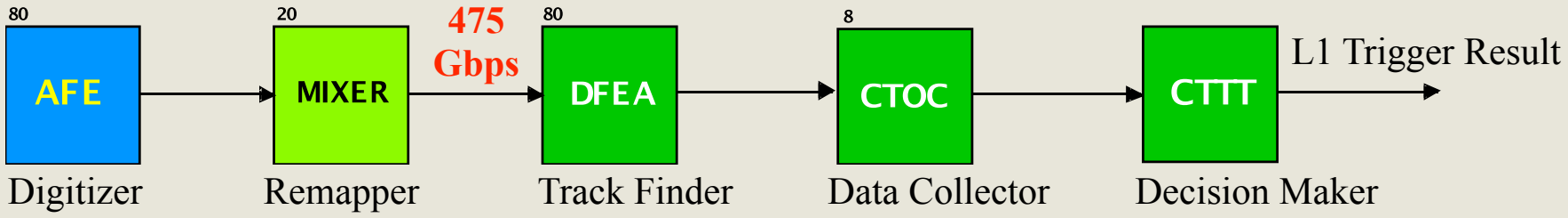
- Btw silicon tracker and 2 Tesla solenoid
- Covering $|\eta| < 1.7$ (22° to beam axis)
- Scintillating fibers read out by Visible Light Proportional Counters (VLPCs)
- 71'680 fibers in 8 axial and 8 stereo doublet layers with radii from 20 to 52 cm
- Segmented into 80 4.5°-wide sectors
- Surrounded by pre-shower detectors



Central Track Trigger (CTT)

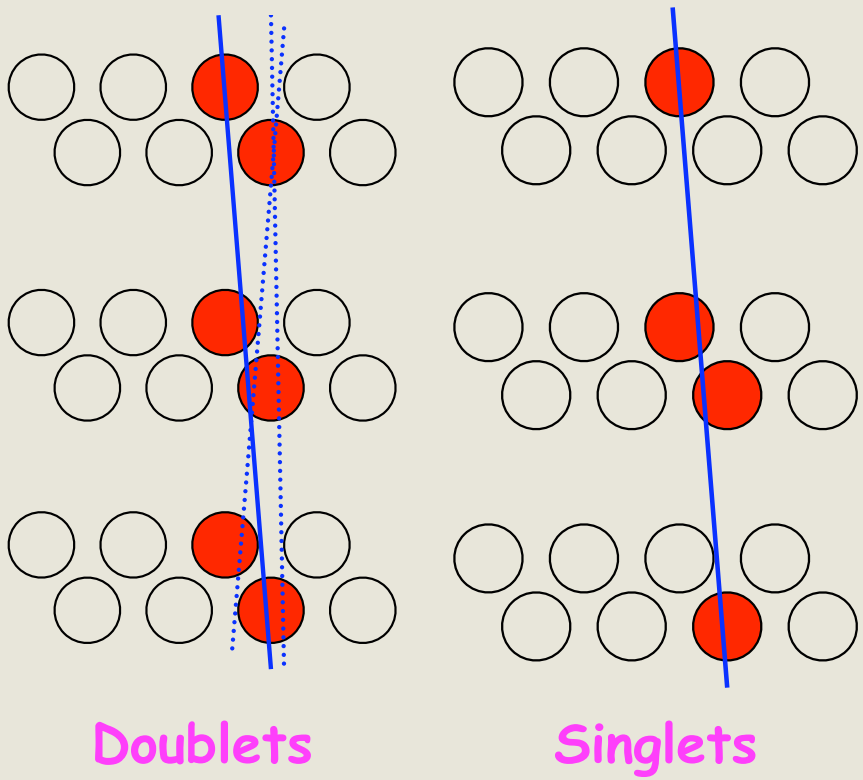
- Hardware trigger on level 1 running at 7.6 MHz (132 ns / decision)
- Uses hit pattern from CFT axial layers to find tracks in r-phi plane with 4 different p_T thresholds: 1.5, 3, 5, 10 GeV
- Tracks constrained to beam-spot region
- Provides additional information on isolation & pre-shower match
- Delivers tracks for L1 Muon & CalTrack trigger
- Generates seed tracks for the level 2 silicon track trigger





Upgrade of the Track-Finding Hardware

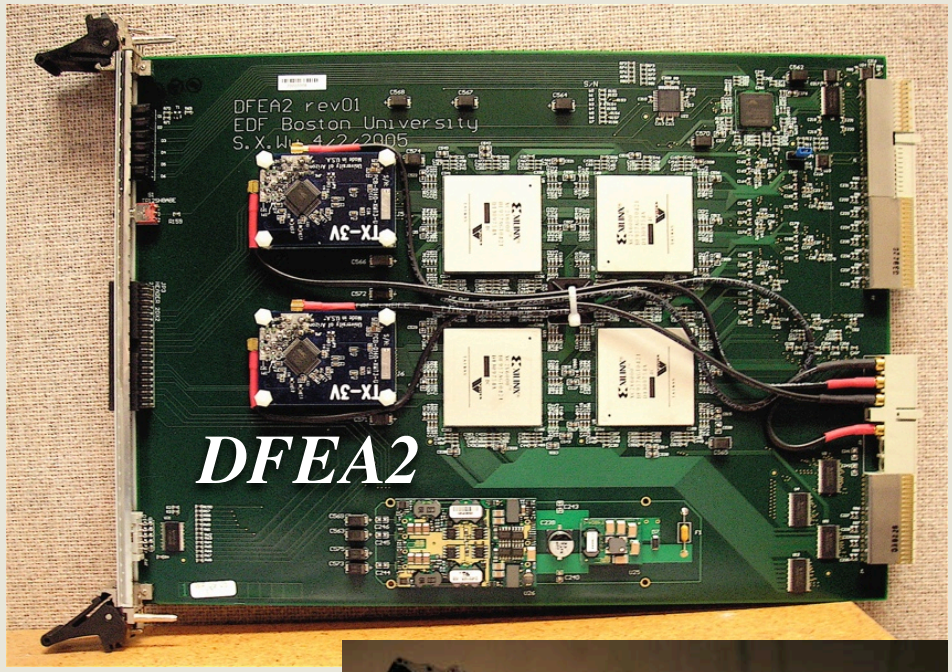
- Run IIa hardware limited the number of fiber hit combinations (equations)
  - Combine 2 fibers into one doublet space-point
  - With increasing occupancy, the fake track rate dominates due to combinatorics
- Solution is to use the full granularity of the CFT using single fiber hits
  - Increases number of track equations from 16k to 50k per sector
  - Needs larger FPGAs with faster download for track equations
- Equations and trigger algorithms continue to be optimized to keep trigger rate under control

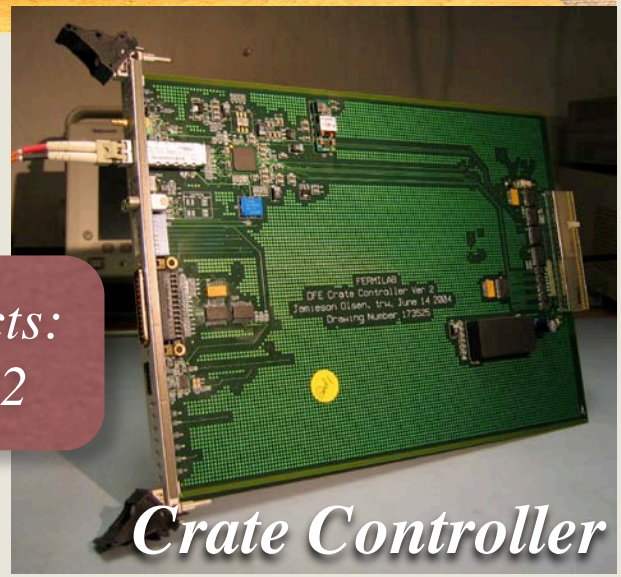


Performance optimization & simulation: Poster N30-256

New Hardware Components

- Track finding hardware (DFEA2):
  - Four large Xilinx Virtex II FPGAs
  - 6U x 320mm format
  - Custom backplane
  - Two trigger sectors per board
  - 8 (4) x 1.5Mbps bus LVDS inputs (outputs)
  - Two 1-Gigabit coaxial copper outputs
  - Designed at Boston University
- New crate controller
  - Gigabit optical Ethernet connection
- Improved infrastructure
  - New redundant power distribution
  - New crate design to improve cable routing

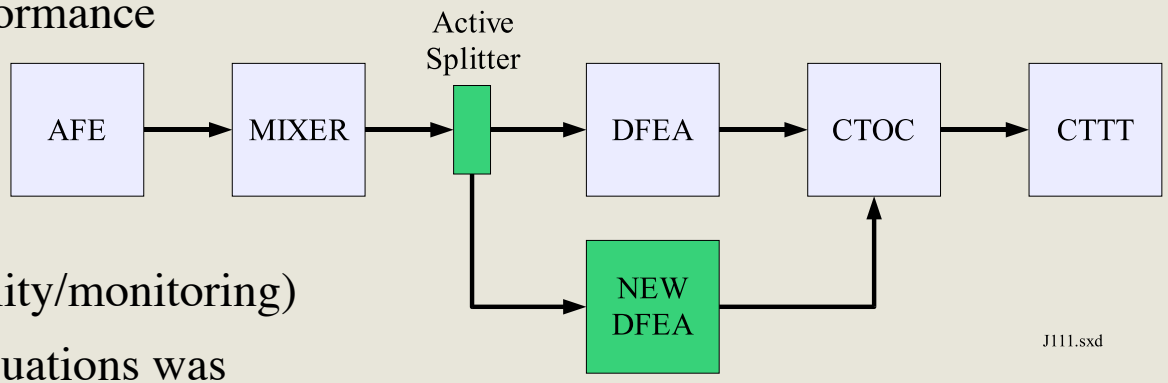




Hardware aspects: Poster N30-242

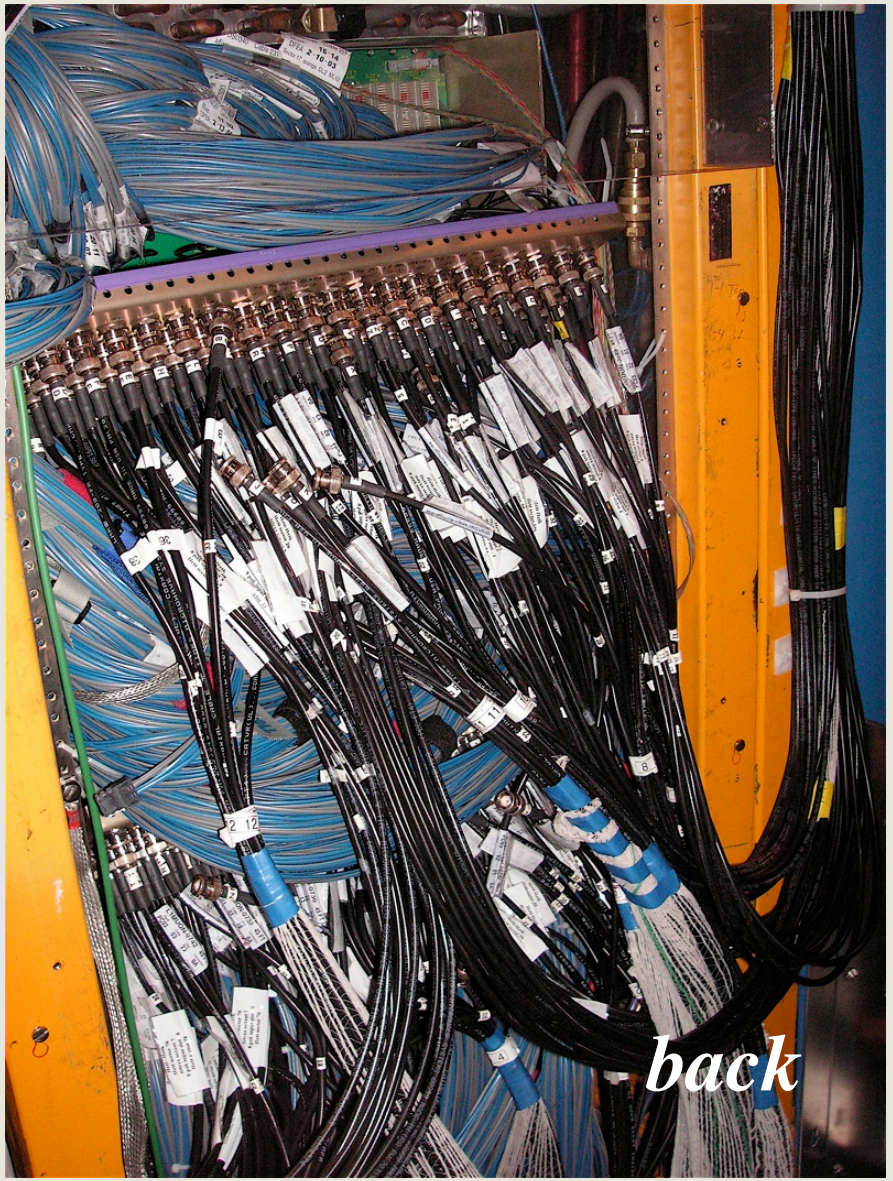
Preparation & Commissioning

- Before the upgrade, the new hardware and trigger algorithms were tested in the real environment
  - 2 new track-finding boards (4 trigger sectors) were running in parallel to the old system
    - 1-to-1 comparison of the performance using the same algorithms
    - Excellent setup to test new algorithms
    - Operational experience (stability/monitoring)
  - A partial version of the singlet equations was deployed in the old hardware 2 months before the upgrade
    - Full assessment of the expected trigger rate reduction for high p_T tracks



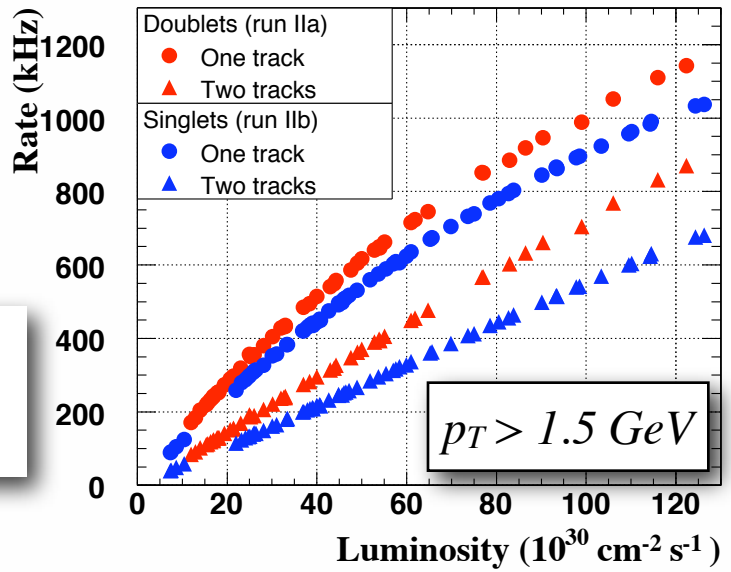
- For the commissioning, the same algorithms as before the upgrade were deployed on the new hardware
  - Unchanged physics performance allowed for a quick check-out of the system
  - The system performs excellently since the beginning

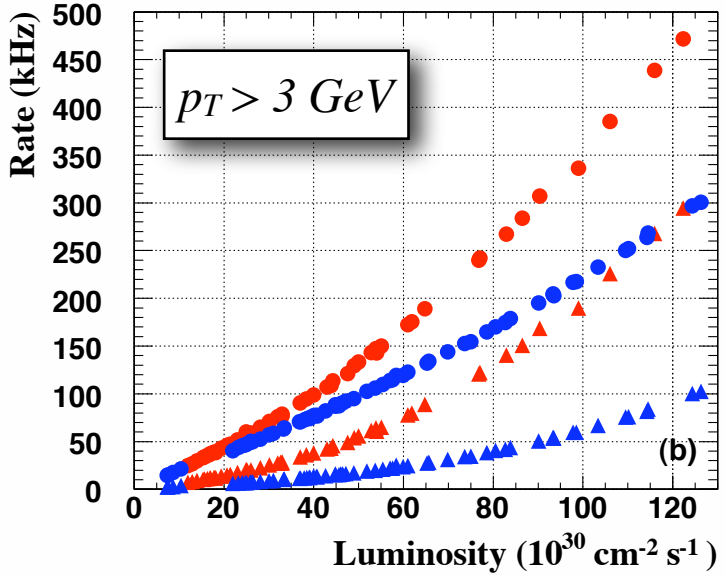
New Hardware Installed

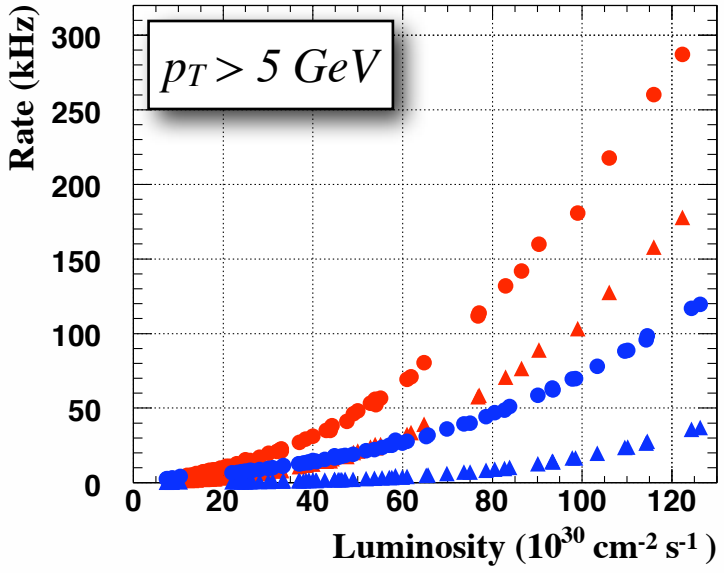


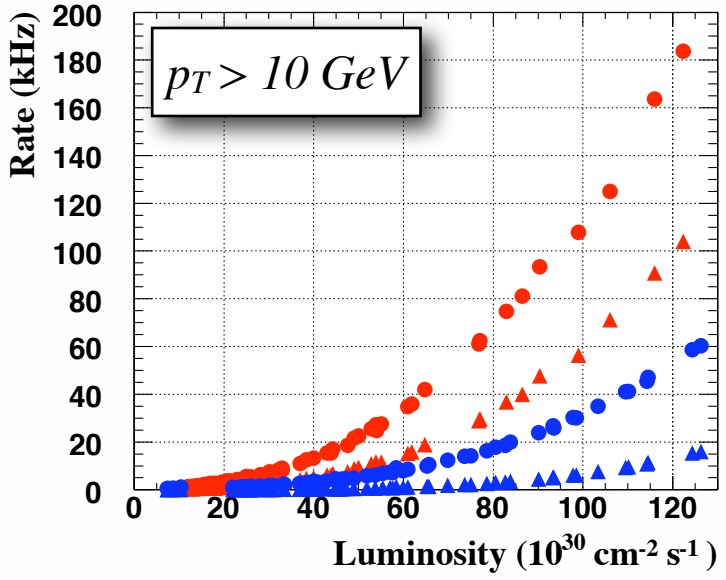
One- and Two-Track Trigger Rates

doublets
singlets

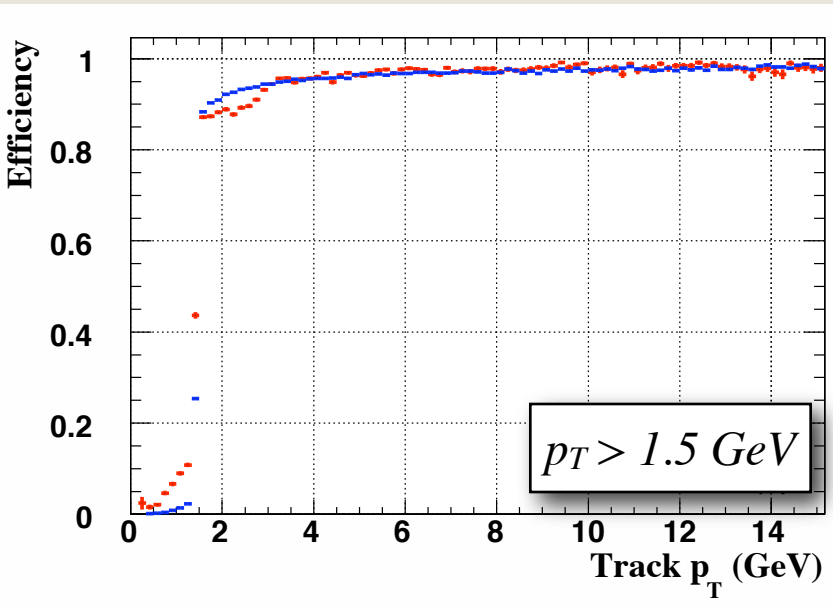


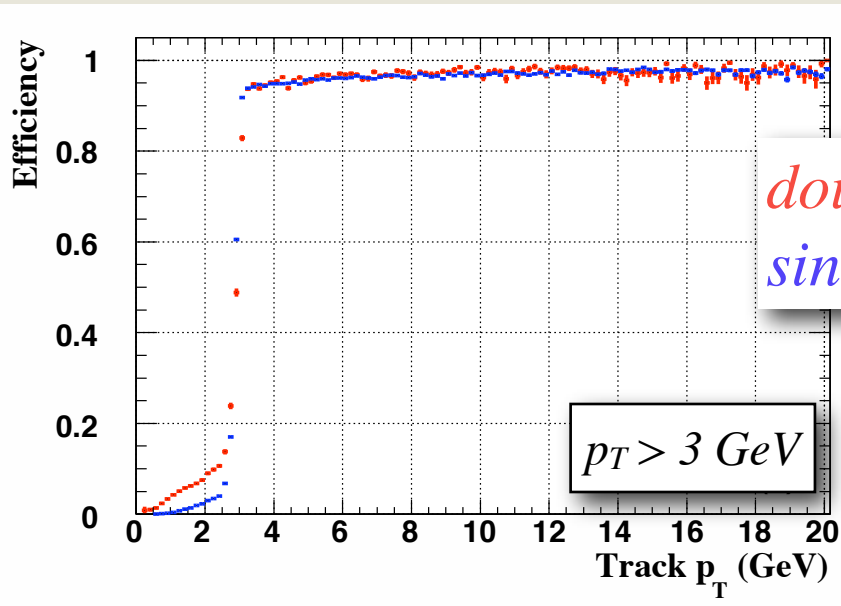




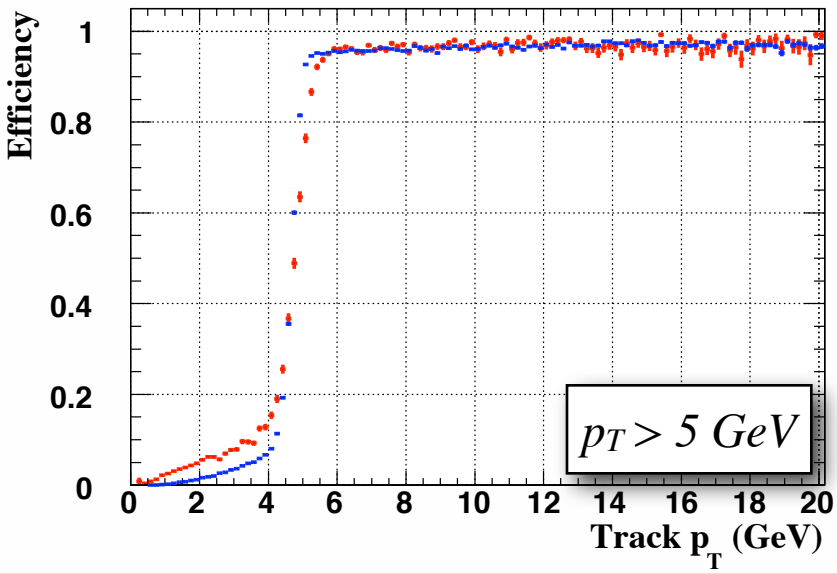


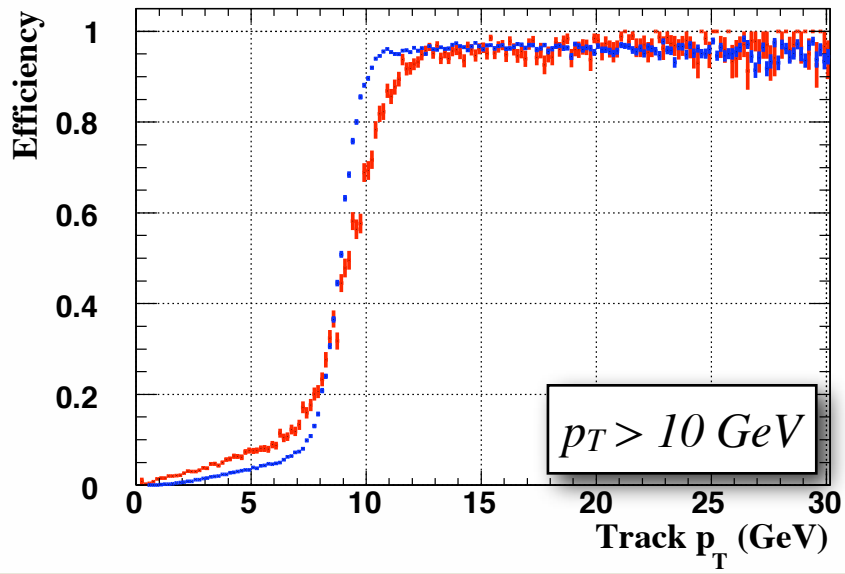
Track Trigger Turn-on Curves





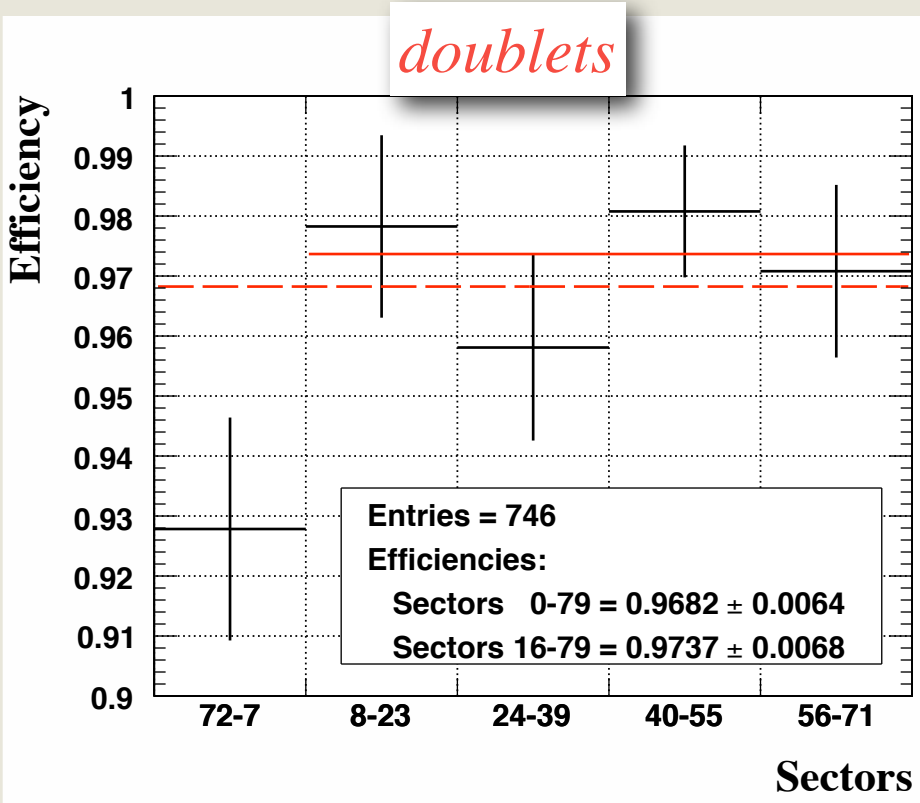
doublets
singlets

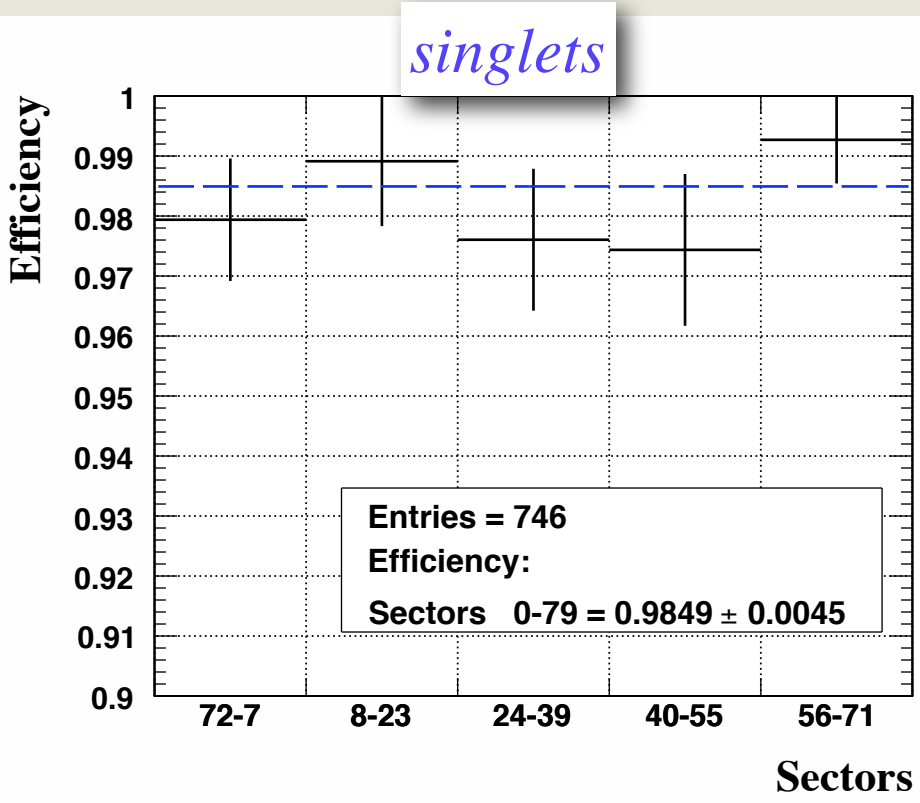




Performance using Z→μμ Events

- Efficiency of the single track trigger for $p_T > 10$ GeV is measured using unbiased muons from Z decays (tag & probe method)
- Using the same events as input to simulation of CTT hardware
- Singlet equations yield a higher efficiency

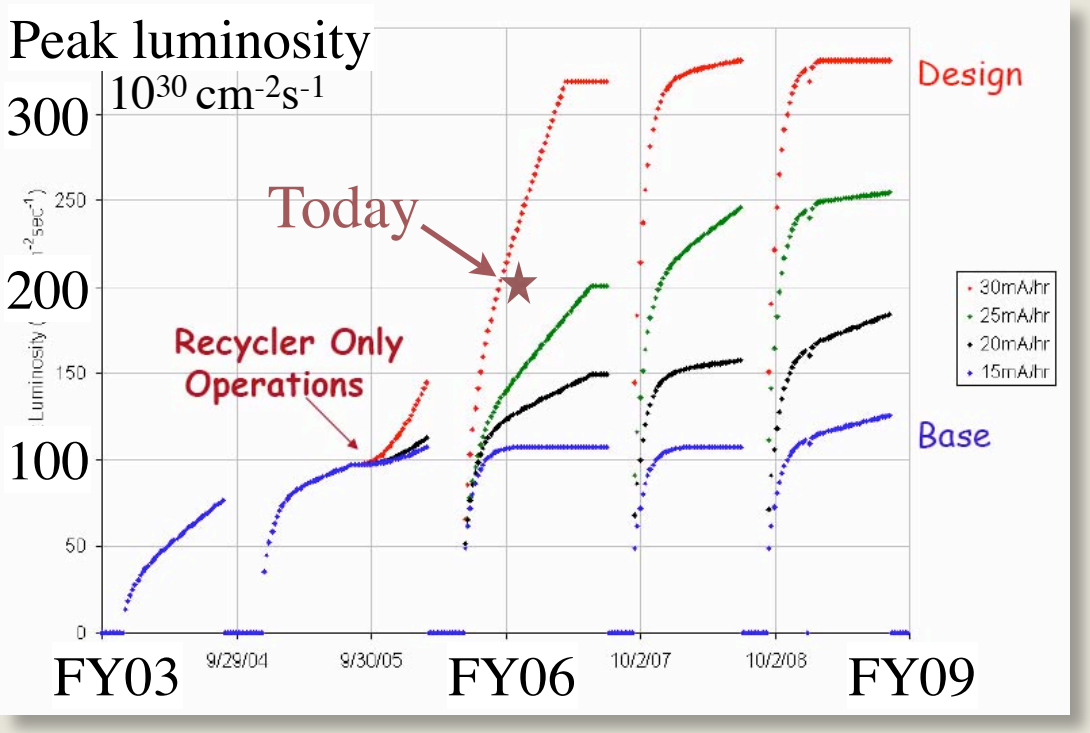




Summary

- The upgraded Central Track Trigger was ready for first beam
- The new track-finding hardware exploits the full CFT granularity
- Trigger rates are reduced by up to a factor of 10
- The track finding efficiency is similar or better
- Trigger turn-on is sharper
- Further improvements in trigger algorithms are needed to cope with increasing peak luminosity

For more information:
Posters N30-242 & N30-256



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