Upgrade and Operation of the DØ Central Track Trigger

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Abstract

The DØ experiment at the Fermilab $p\overline{p}$ Tevatron collider (Batavia, IL, USA) has undergone significant upgrades in anticipation of high luminosity running conditions. As part of the upgrade, the capabilities of the Central Track Trigger (CTT) to make trigger decisions based on hit patterns in the Central Fiber Tracker (CFT) have been much improved. We report on the implementation, commissioning and operation of the upgraded CTT system.

1 Introduction

The Tevatron collides protons and antiprotons with a bunch-spacing of 396 ns at a center of mass energy of $\sqrt{s} = 1.96$ TeV. High luminosity data taking (Run IIb) is well underway, with initial luminosities reaching over 2×10^{32} cm^{-2} s^{-1}. In order to select interesting physics events containing tracks in the central region of the DØ detector ([1], [2]), the CTT identifies trajectories of charged particles based on discriminator signals provided by scintillator-based detectors (see Fig. 1, [3]). CTT trigger logic is implemented in field programmable gate arrays (FPGAs) which compare fiber hit inputs to a predefined list of track equations.

2 CTT Upgrade

For Run IIa, equations combined discriminated inputs from pairs of neighboring fibers (doublets) to reduce the number of track equations. However, as luminosity increases, CTT track-finding was dominated by fake tracks due to combinatorics. For Run IIb the solution was to take advantage of the full CFT granularity by using singlet fiber hits (see Fig. 2). This resulted in an increase in the number of track equations from 16,000 to 50,000 per trigger sector. Larger FPGAs with faster access were needed to accommodate the new track-finding scheme.

The upgraded CTT track-finding FPGAs reside on 40 Digital Front End Axial boards (DFEA2, [4]) which represent the core of the CTT system (see Fig. 3). Each DFEA2 board contains four Xilinx Virtex II FPGAs, and is able to process two trigger sectors. The DFEA2 front panel was designed to accommodate a multitude of options for testing and diagnostics via a multipurpose LED display, and interfaces for a logic analyzer, oscilloscope, and laptop. The boards reside in two 6U crates with a custom designed backplane. I/O is mostly handled via Low Voltage Differential Signal (LVDS) cables at speeds ranging from six to twelve Mbps. All I/O cabling is routed through the backside of each crate to facilitate easy DFEA2 maintenance access.

In addition to the DFEA2 boards, redesigned crate controllers (DFEC) were also installed during the upgrade. The upgraded DFECs provide a high bandwidth Gigabit Ethernet communication path which allows firmware to be downloaded much faster than with the previously used 1553 bus.

The new hardware was installed on the detector platform during the Run IIb upgrade shutdown in Spring 2006.

In order to quantify the performance of the upgraded CTT, trigger rates, turn-on curves, and efficiencies were examined. Figure 4 compares trigger rates using singlet and doublet equations, demonstrating clear improvement with singlet equations. At the same time, the efficiency to detect a track of a given p_T is similar or better with singlet equations.

3 Summary

The new CTT track-finding hardware which was installed during the Run IIb upgrade shutdown exploits the full granularity of the CFT. With reduced trigger rates, sharper turn-ons, and improved efficiencies, the upgraded CTT has been well able to cope with the increased luminosity delivered by the Tevatron during Run IIb. However, further luminosity increases beyond 3×10^{32} cm^{-2} s^{-1} will require additional efforts.

4 Figure captions

Fig. 1: Schematic view of the axial part of the Central Fiber Tracker (CFT). It consists of 8 concentrical doublet layers of scintillating fibers and a pre-shower

detector (CPS) surrounding the interaction point. One of the 80 4.5° trigger sectors used by the CTT is shown with a hypothetical track overlaid.

Fig. 2: Schematic view of 3 doublet layers. On the left, the doublet scheme is depicted, showing that beside from the correct track (solid blue line) other tracks (dashed blue lines) can trigger the same equation. With the singlet equation shown on the right, only the correct track fires the trigger.

Fig. 3: DFEA2 board with 4 Xilinx Virtex 2 FPGAs in the center.

Fig. 4: Trigger rates for single (circle) and double (triangle) track triggers as a function of luminosity for doublet equations (red) and singlet equations (blue) for tracks with $p_T > 3$ GeV.

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