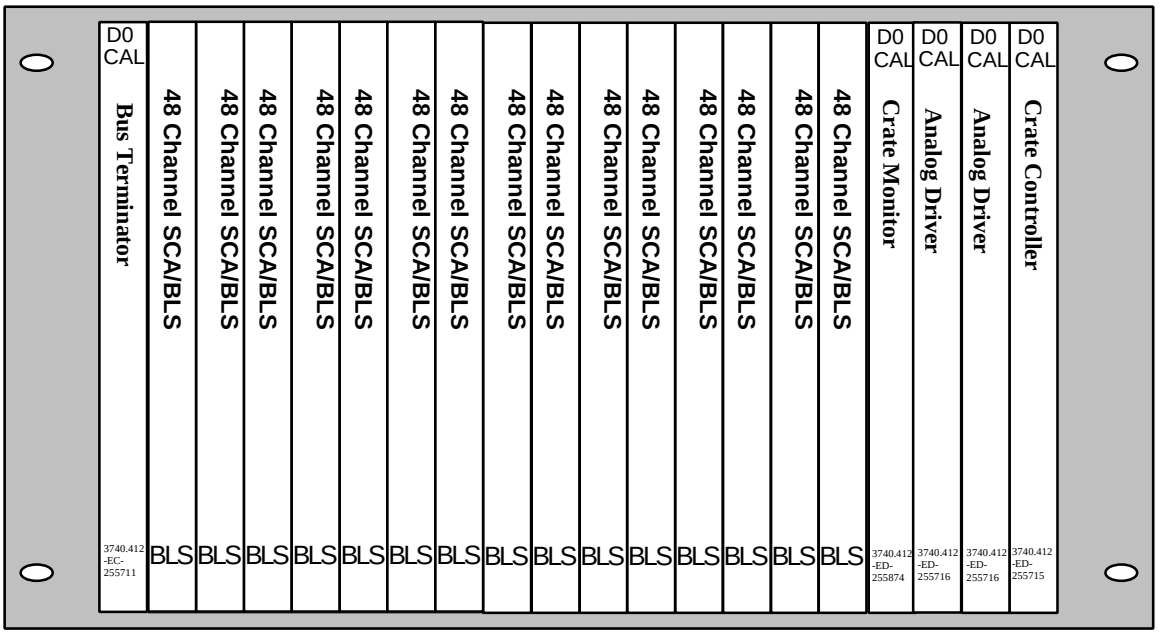
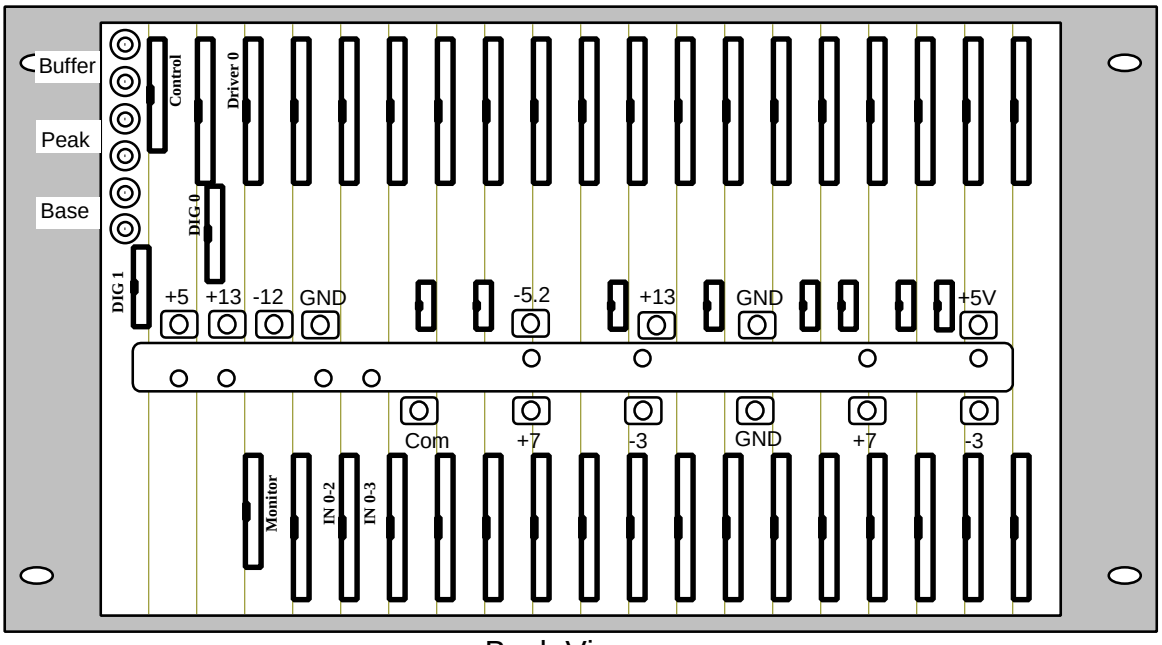
David L. Huffman
6/5/00 11:34 AM

BLS Crate

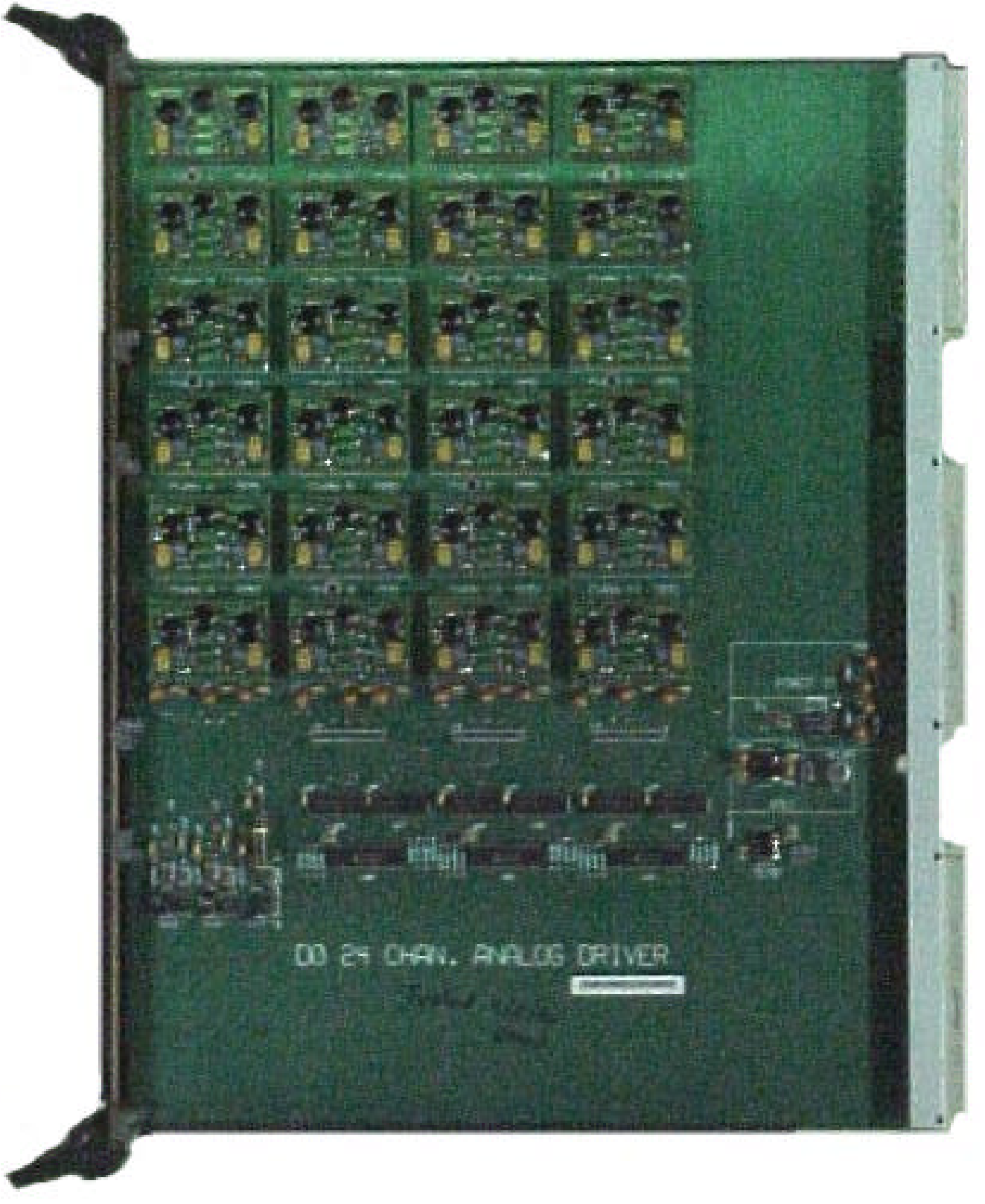


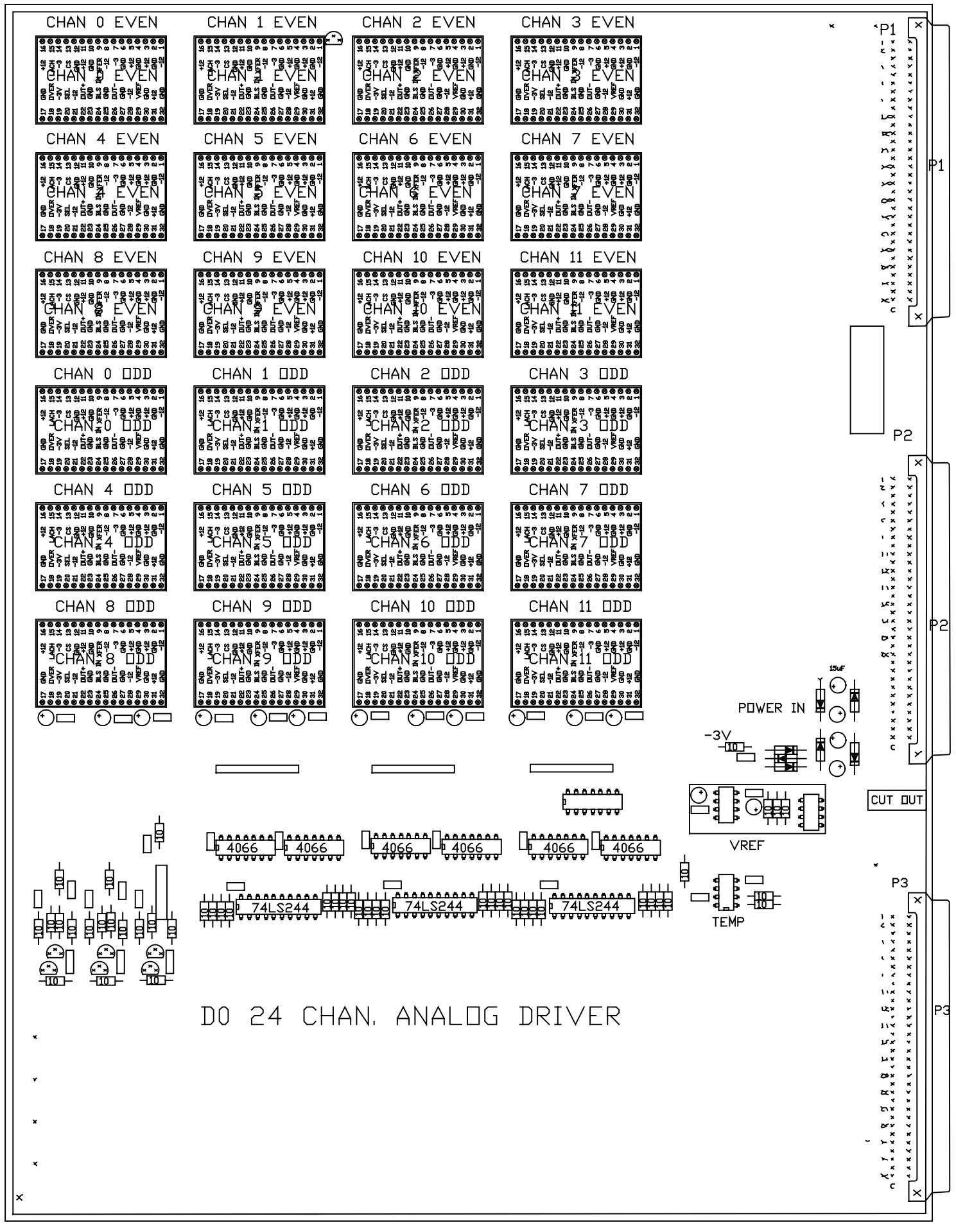
Front View

BLS Crate



Back View


DD 24 CHAN. ANALOG DRIVER



14.437 IN.

D0 ANALOG DRIVER
CDMBA510.DBF
CUSB 2/90 DMW

LAYER ORDER
1
2
3
4
5
6
7
8
9

NEXT PAGE

MISC. FILES
DRILL TARGETS
ASSY DRAWING

FINISHED HOLE SIZES:
A=0.027″
B=0.035″
D=0.110″

SPECIFICATIONS
.062″ FR4
SOLDER PLATE FINISH
MUTI LAYER PCB [6]
1X ARTWORK
QUANTITY
SHORT/OPEN TEST

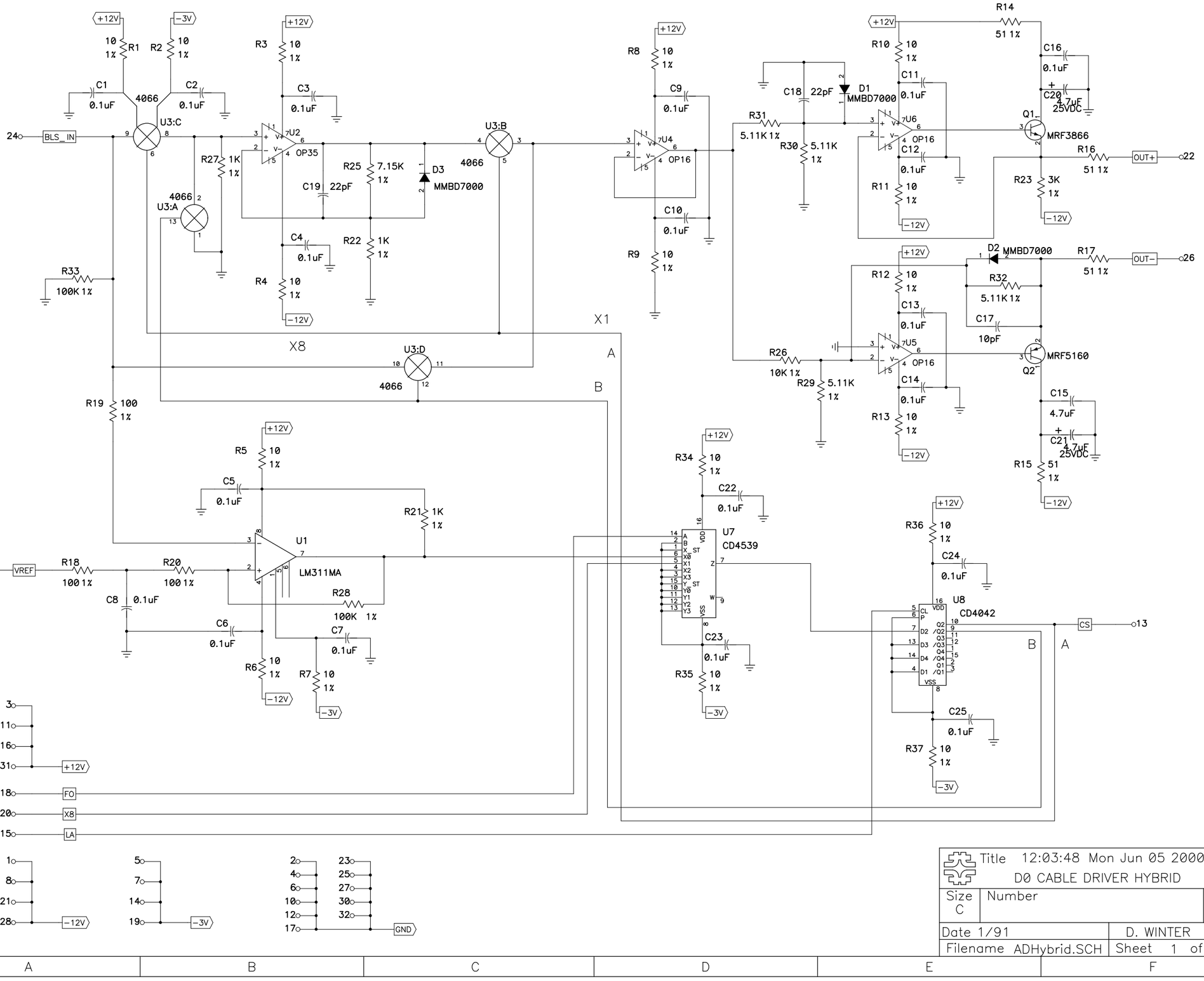
LAYOUT
D.M.WINTER 8-89
CUSB COLLABORATION
CDMBA402.DBF .5MILL RES
CDMBL400.LIB

SHIP TO:
P.M. TUTS
WILSON LAB
DRYDEN ROAD
CORNELL UNIVERSITY
ITHACA, NEW YORK 14853
1-607-255-0937

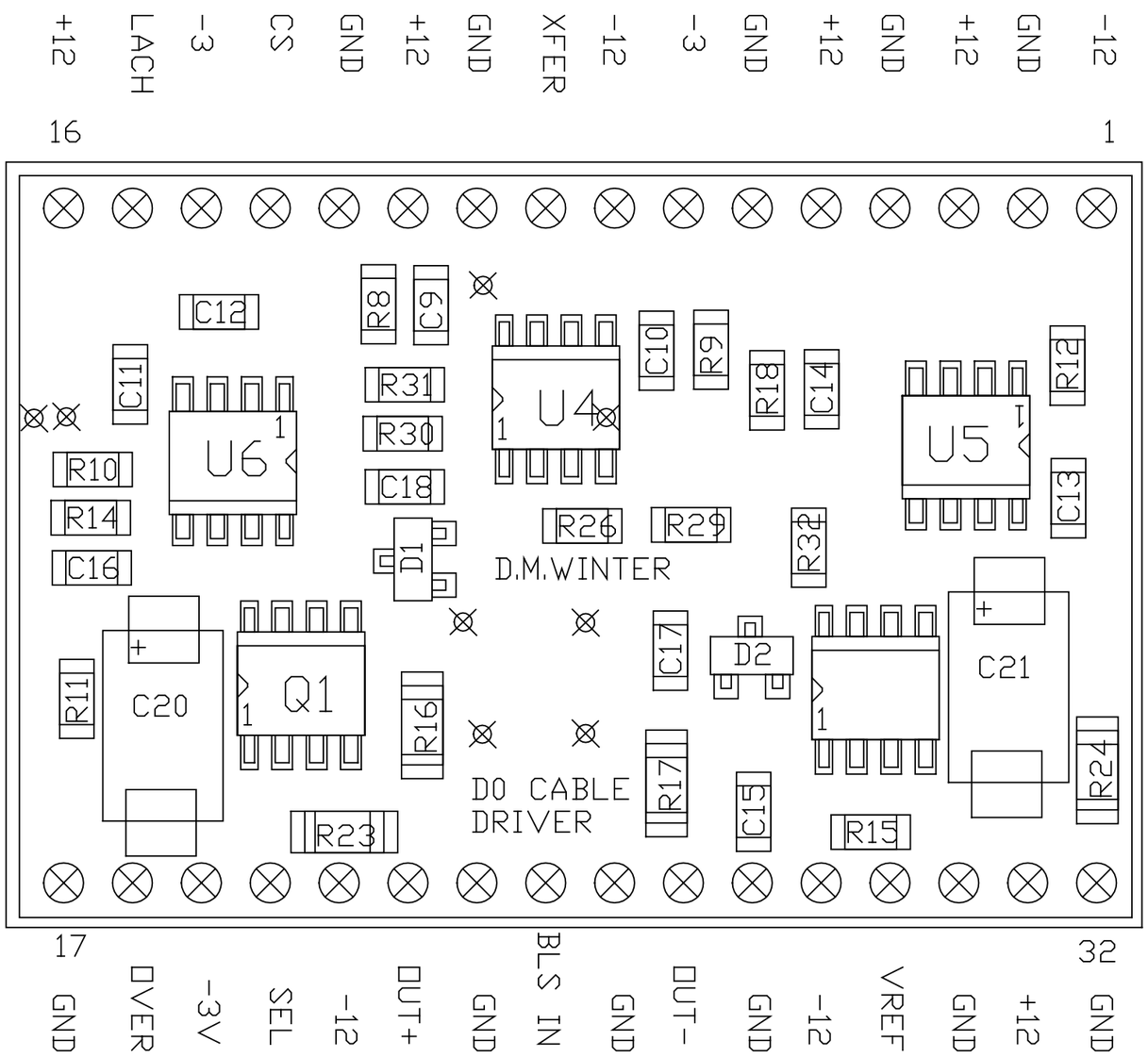
BILL TO:
RESEARCH FOUNDATION
SUNY AT STONY BROOK
STONY BROOK, N.Y. 11794
ATTN. JOAN NAPOLITANO
1-516-632-8095

ROUTE TO INSIDE

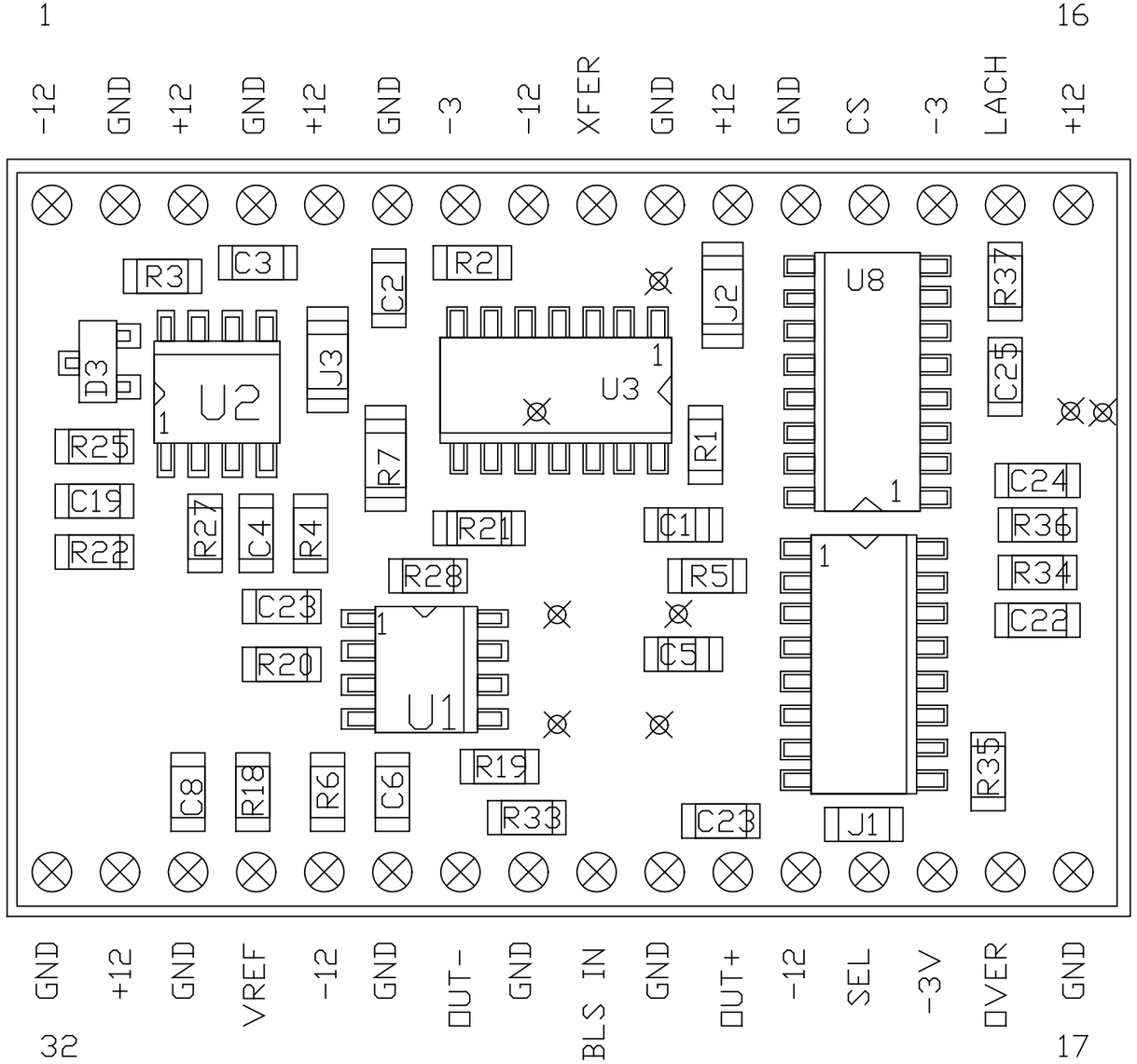
NEXT PAGE


+12V
-3V
R1 10 1%
R2 10 1%
C1 0.1uF
C2 0.1uF
4066
U3:C
24
BLS_IN
R27 1K 1%
4066
U3:A
R3 10 1%
C3 0.1uF
U2
OP35
C19 22pF
R25 7.15K 1%
D3
MMBD7000
C4 0.1uF
R22 1K 1%
R4 10 1%
-12V
U3:B
4066
R8 10 1%
C9 0.1uF
U4
OP16
C10 0.1uF
R9 10 1%
R33 100K 1%
X8
X1
A
B
U3:D
4066
R19 100 1%
R31 5.11K 1%
R30 5.11K 1%
C18 22pF
D1
MMBD7000
R10 10 1%
C11 0.1uF
U6
OP16
C12 0.1uF
R11 10 1%
R14 51 1%
C16 0.1uF
C20 4.7uF 25VDC
Q1
MRF3866
R16 51 1%
OUT+
22
R23 3K 1%
R26 10K 1%
R29 5.11K 1%
R12 10 1%
C13 0.1uF
U5
OP16
C14 0.1uF
R13 10 1%
D2
MMBD7000
R17 51 1%
OUT-
26
R32 5.11K 1%
C17 10pF
MRF5160
Q2
C15 4.7uF
C21 4.7uF 25VDC
R15 51 1%
R5 10 1%
C5 0.1uF
R21 1K 1%
U1
LM311MA
29
VREF
R18 100 1%
R20 100 1%
C8 0.1uF
R28 100K 1%
C6 0.1uF
C7 0.1uF
R6 10 1%
R7 10 1%
R34 10 1%
C22 0.1uF
U7
CD4539
C23 0.1uF
R35 10 1%
R36 10 1%
C24 0.1uF
U8
CD4042
CS
13
C25 0.1uF
R37 10 1%
3
11
16
31
18
FO
20
X8
15
LA
1
8
21
28
5
7
14
19
2
4
6
10
12
17
23
25
27
30
32
GND
Title 12:03:48 Mon Jun 05 2000
D0 CABLE DRIVER HYBRID
Size C
Number
Rev -
Date 1/91
D. WINTER
Filename ADHybrid.SCH
Sheet 1 of 1

NEXT PAGE



TOP VIEW

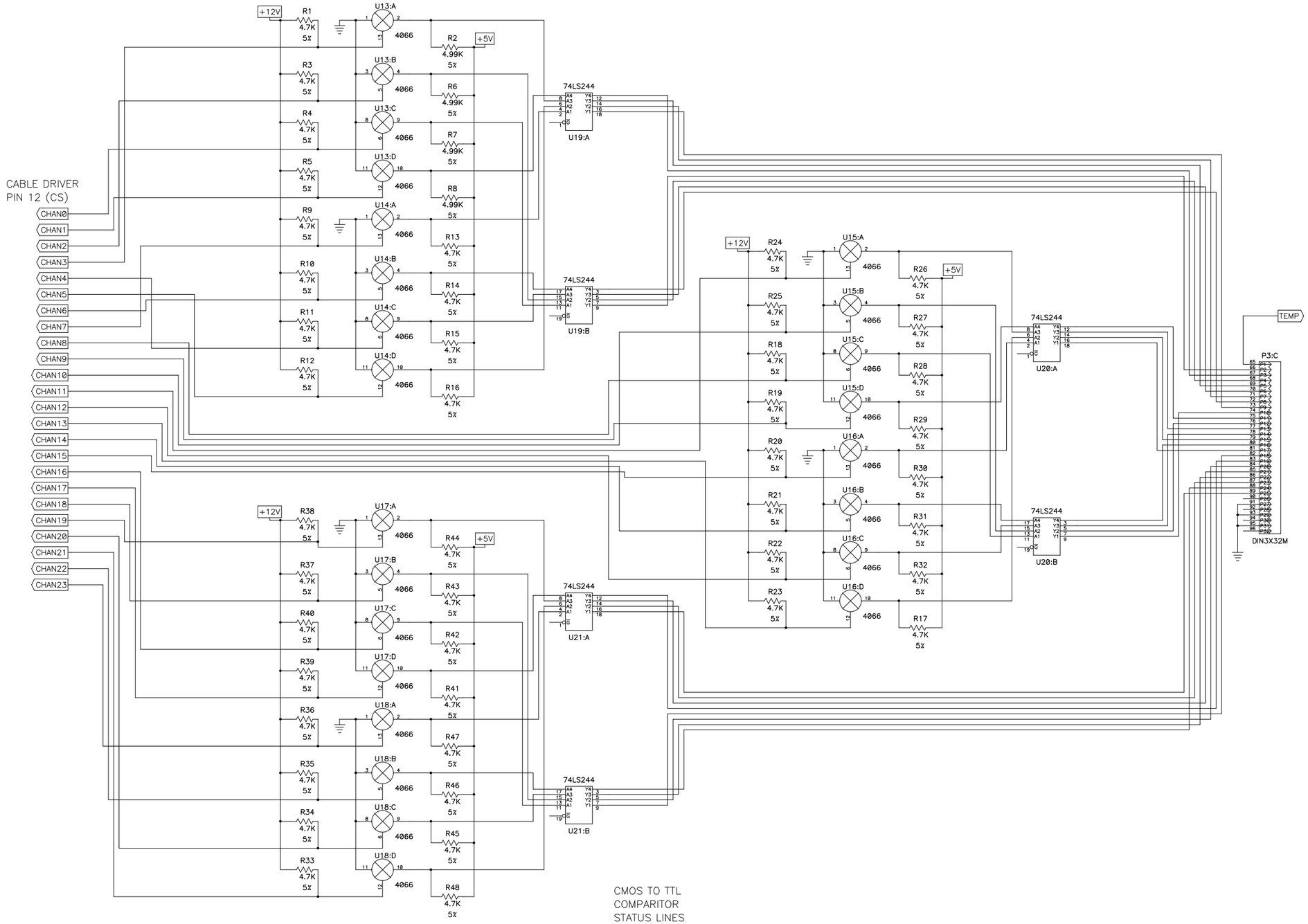


BOTTOM VIEW

DO CABLE DRIVER HYBRID

CDWBA410.DBF

NEXT PAGE



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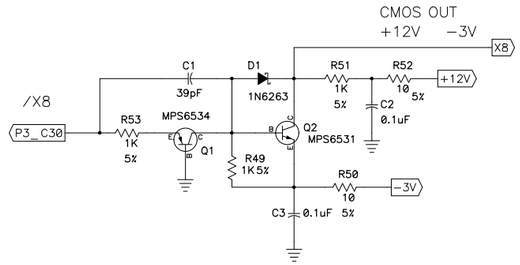
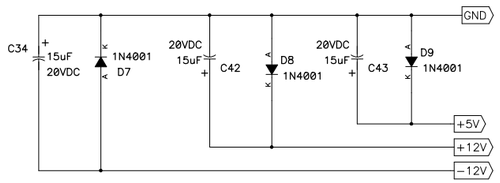
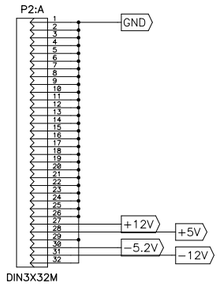
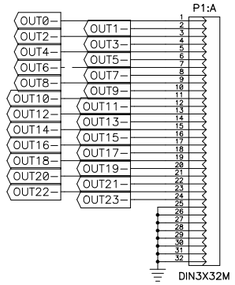
Size D	Number		Rev –
Date	1/28/91	D. WINTER	
Filename	AnalogDriver.SCH	Sheet 1 of 2	

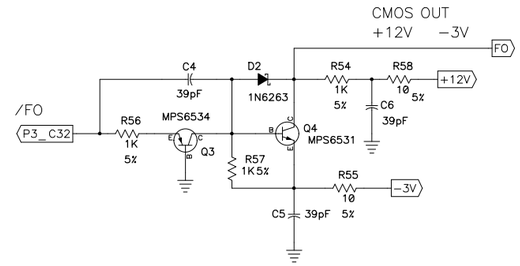
TOP

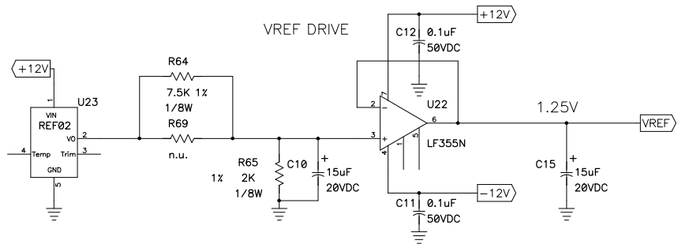


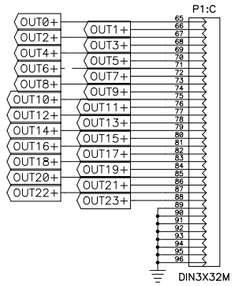


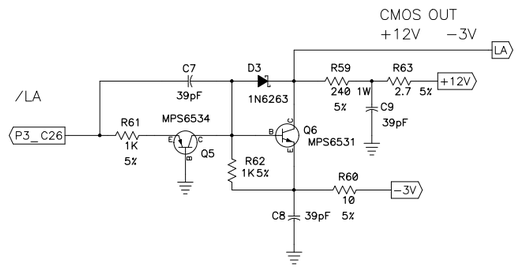


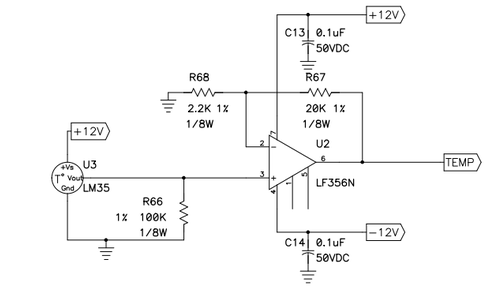


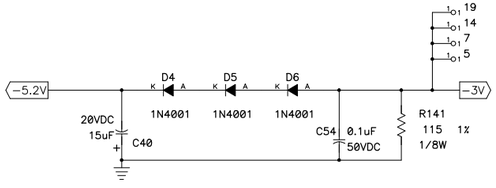


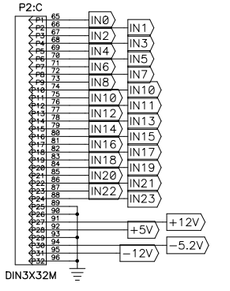












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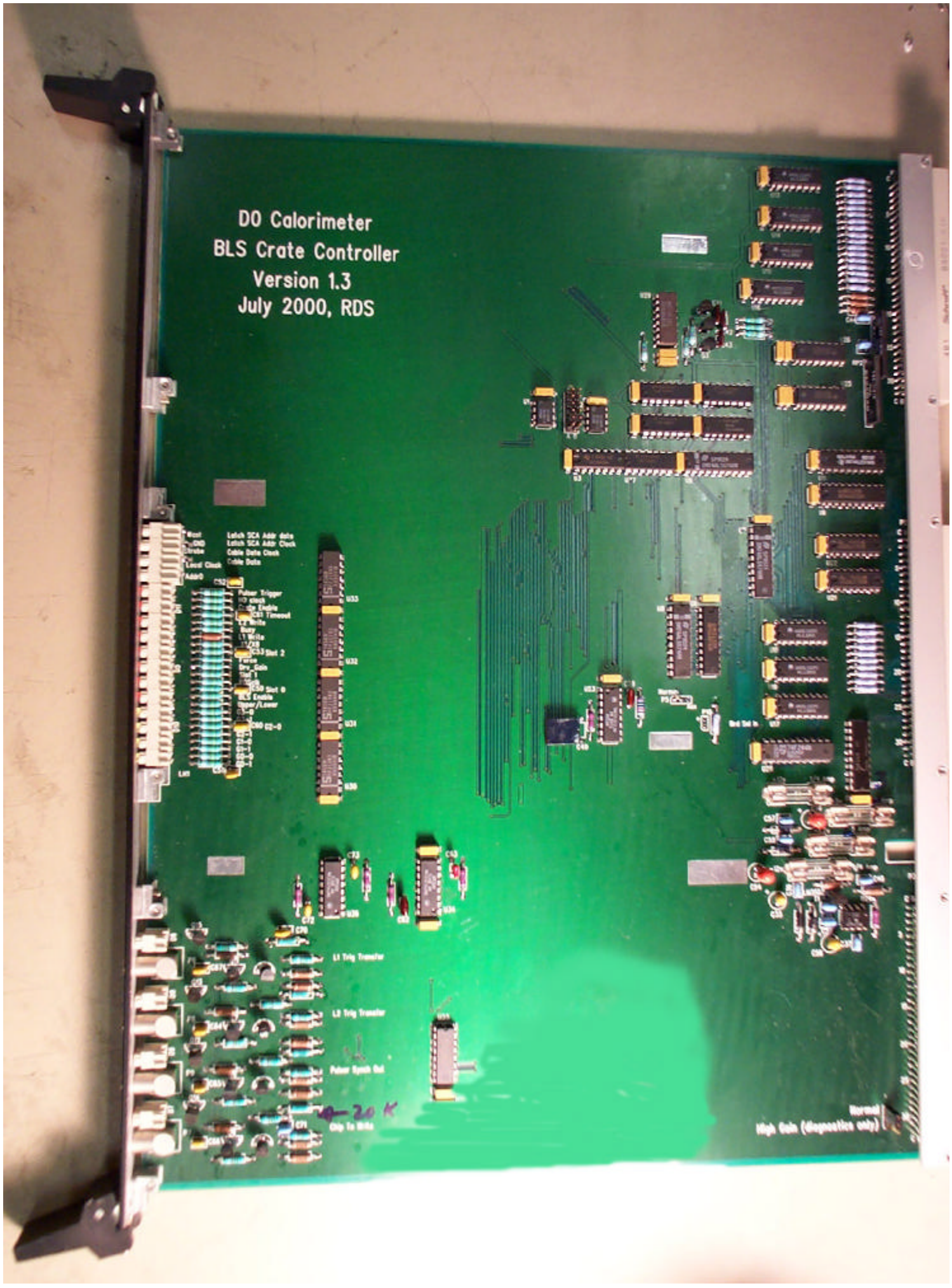
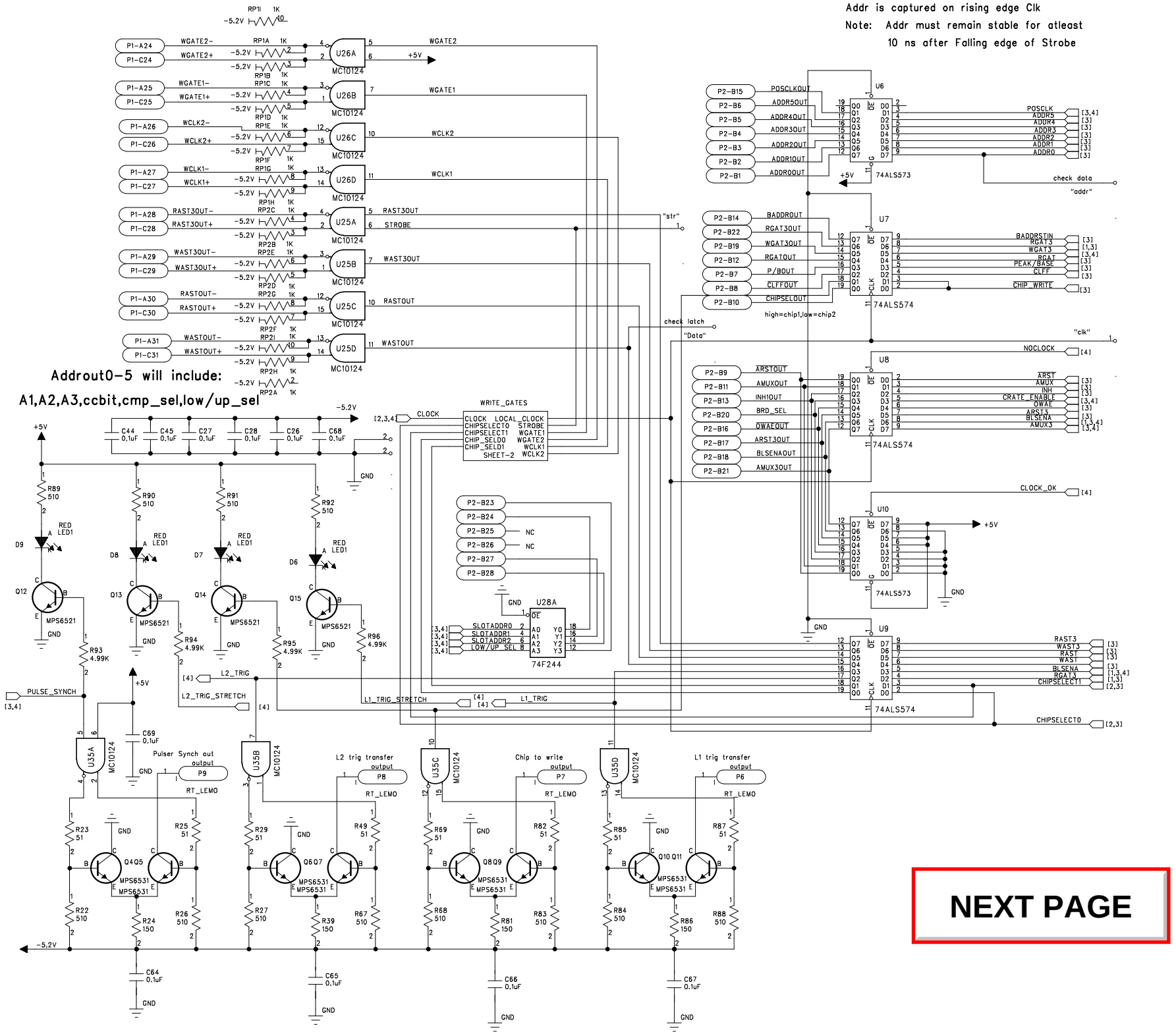
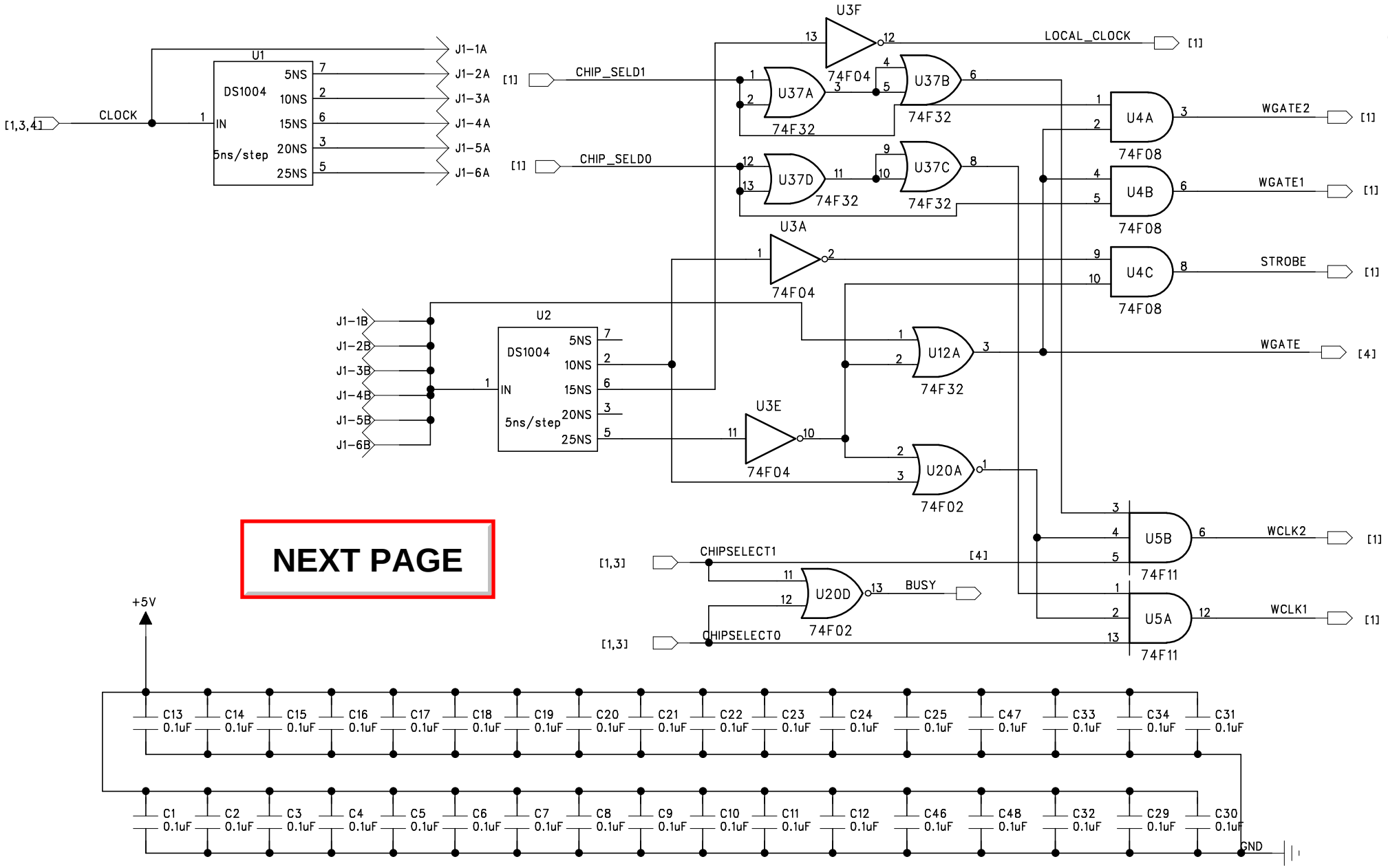
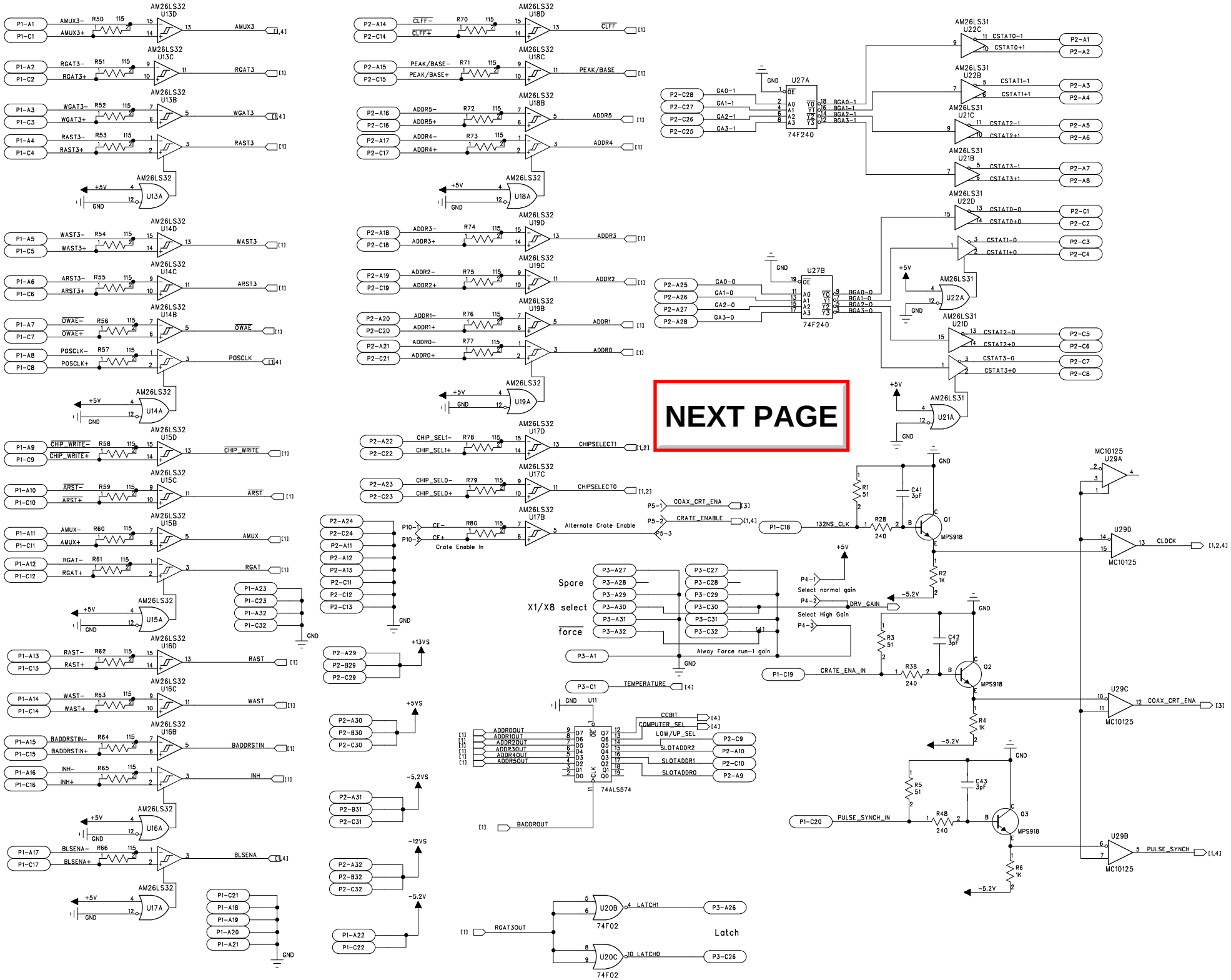
Size D	Number		Rev –
Date	1/28/91	D. WINTER	
Filename	AnalogDriver.SCH	Sheet 2 of 2	


D0 Calorimeter
BLS Crate Controller
Version 1.3
July 2000, RDS

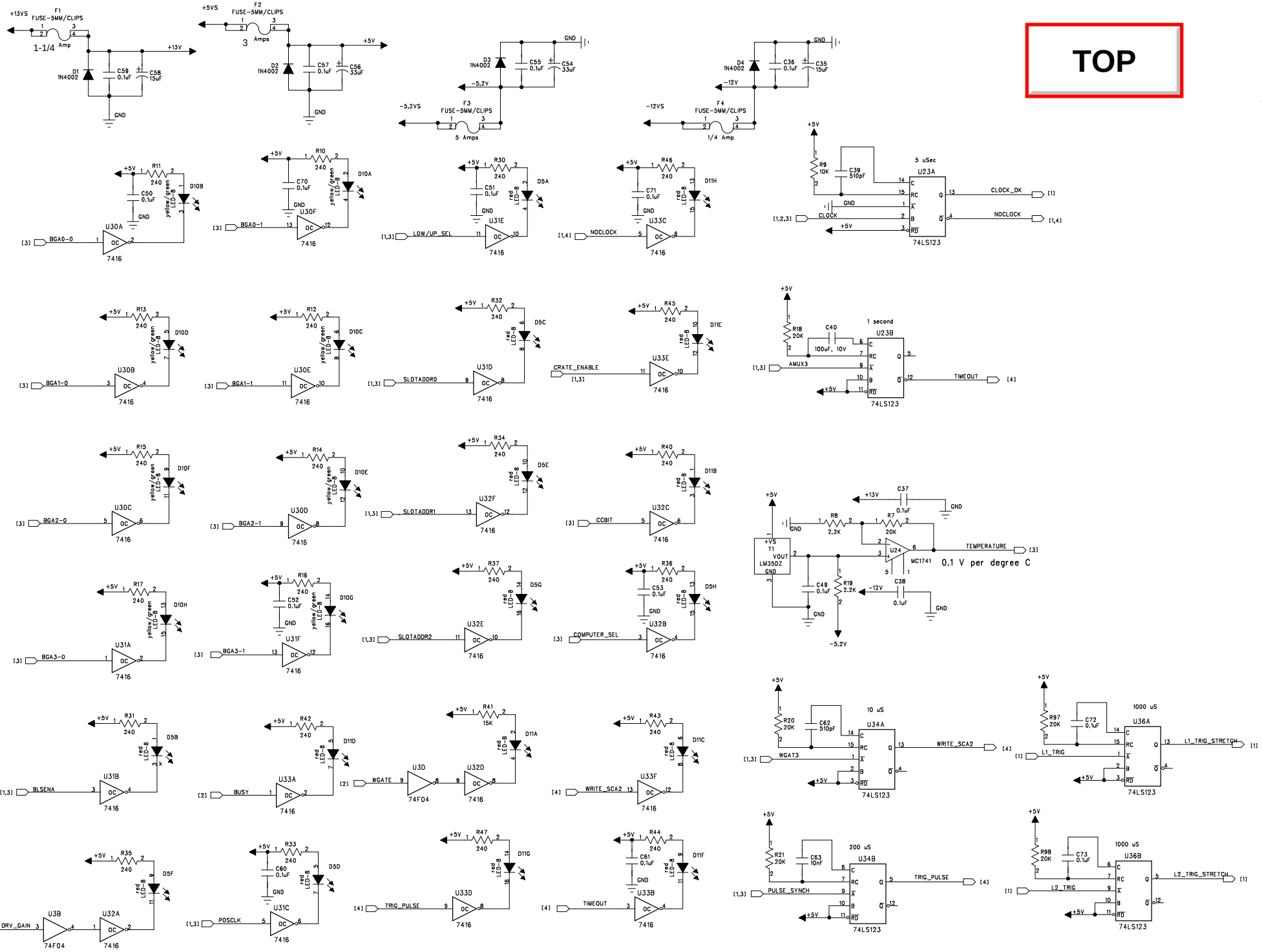

Addr is captured on rising edge Clk
Note: Addr must remain stable for atleast
10 ns after Falling edge of Strobe
Addrout0-5 will include:
A1,A2,A3,ccbit,cmp_sel,low/up_sel
WRITE_GATES
CLOCK LOCAL_CLOCK
CHIPSELECT0 STROBE
CHIPSELECT1 WGATE1
CHIP_SELD0 WGATE2
CHIP_SELD1 WCLK1
SHEET-2 WCLK2
U6
U7
U8
U9
U10
74ALS573
74ALS574
74F244
MC10124
MPS6521
MPS6531
high=chip1,low=chip2
check data
"addr"
check latch
"Data"
"str"
"clk"
NEXT PAGE


U1
DS1004
5ns/step
CLOCK
IN
5NS
10NS
15NS
20NS
25NS
J1-1A
J1-2A
J1-3A
J1-4A
J1-5A
J1-6A
[1,3,4]
[1]
CHIP_SELD1
CHIP_SELD0
U37A
U37B
U37C
U37D
74F32
U3F
74F04
U3A
U3E
LOCAL_CLOCK
U4A
U4B
U4C
74F08
WGATE2
WGATE1
STROBE
U2
J1-1B
J1-2B
J1-3B
J1-4B
J1-5B
J1-6B
U12A
WGATE
[4]
U20A
74F02
CHIPSELECT1
CHIPSELECT0
U20D
BUSY
[1,3]
U5B
U5A
74F11
WCLK2
WCLK1
+5V
GND
C13 0.1uF
C14 0.1uF
C15 0.1uF
C16 0.1uF
C17 0.1uF
C18 0.1uF
C19 0.1uF
C20 0.1uF
C21 0.1uF
C22 0.1uF
C23 0.1uF
C24 0.1uF
C25 0.1uF
C47 0.1uF
C33 0.1uF
C34 0.1uF
C31 0.1uF
C1 0.1uF
C2 0.1uF
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
C12 0.1uF
C46 0.1uF
C48 0.1uF
C32 0.1uF
C29 0.1uF
C30 0.1uF

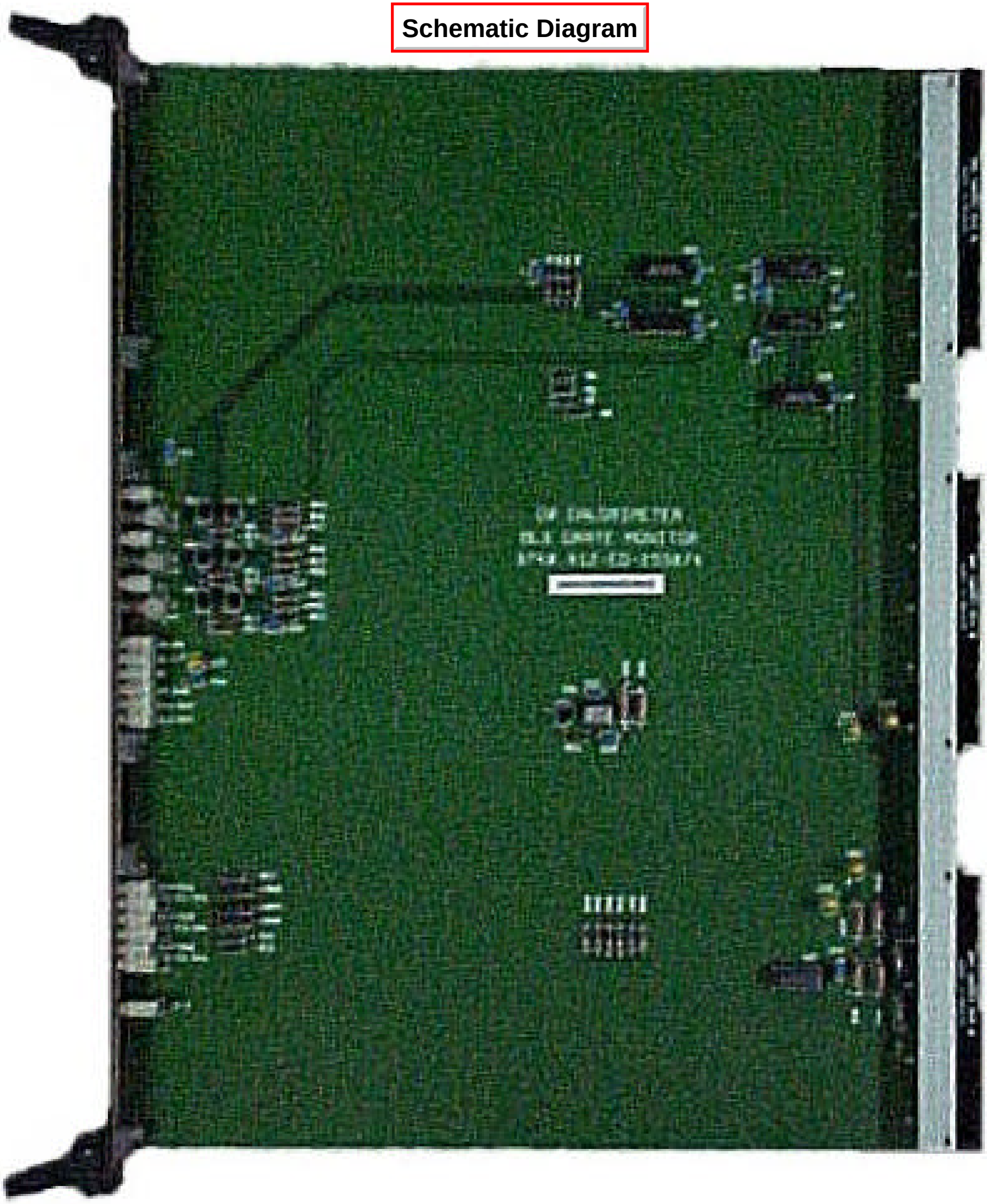
NEXT PAGE


NEXT PAGE
Spare
X1/X8 select
force
Alway Force run-1 gain
Select normal gain
Select High Gain
DRV_GAIN
Crate Enable In
Alternate Crate Enable
Latch
74F240
74ALS574
MPS918
MC10125
-3 - Fri Aug 11 09:45:13 2000

TOP

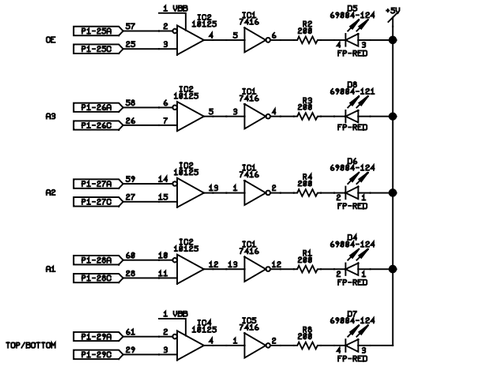

+13VS
F1
FUSE-5MM/CLIPS
1-1/4 Amp
D1 1N4002
C59 0.1uF
C58 15uF
GND
+5VS
F2
FUSE-5MM/CLIPS
3 Amps
D2 1N4002
C57 0.1uF
C56 33uF
-5.2VS
F3
FUSE-5MM/CLIPS
5 Amps
D3 1N4002
C55 0.1uF
C54 33uF
-5.2V
-12VS
F4
FUSE-5MM/CLIPS
1/4 Amp
D4 1N4002
C36 0.1uF
C35 15uF
-12V
U30A
U30B
U30C
U30D
U30E
U30F
7416
BGA0-0
BGA1-0
BGA2-0
BGA3-0
BGA0-1
BGA1-1
BGA2-1
BGA3-1
U31A
U31B
U31C
U31D
U31E
U31F
U32A
U32B
U32C
U32D
U32E
U32F
U33A
U33B
U33C
U33D
U33E
U33F
74F04
U3B
U3D
LOW/UP_SEL
NOCLOCK
SLOTADDR0
SLOTADDR1
SLOTADDR2
CCBIT
COMPUTER_SEL
BLSENA
BUSY
WGATE
WRITE_SCA2
DRV_GAIN
POSCLK
TRIG_PULSE
TIMEOUT
U23A
5 uSec
R9 10K
C39 510pF
CLOCK
CLOCK_OK
NOCLOCK
74LS123
U23B
1 second
R18 20K
C40 100uF, 10V
AMUX3
TIMEOUT
U24
MC1741
TEMPERATURE
0.1 V per degree C
R8 2.2K
R7 20K
R19 2.2K
C37 0.1uF
C38 0.1uF
C49 0.1uF
C53 0.1uF
T1
LM35DZ
U34A
10 uS
R20 20K
C62 510pF
WGAT3
U34B
200 uS
R21 20K
C63 10nF
PULSE_SYNCH
U36A
1000 uS
R97 20K
C72 0.1uF
L1_TRIG
L1_TRIG_STRETCH
U36B
R98 20K
C73 0.1uF
L2_TRIG
L2_TRIG_STRETCH

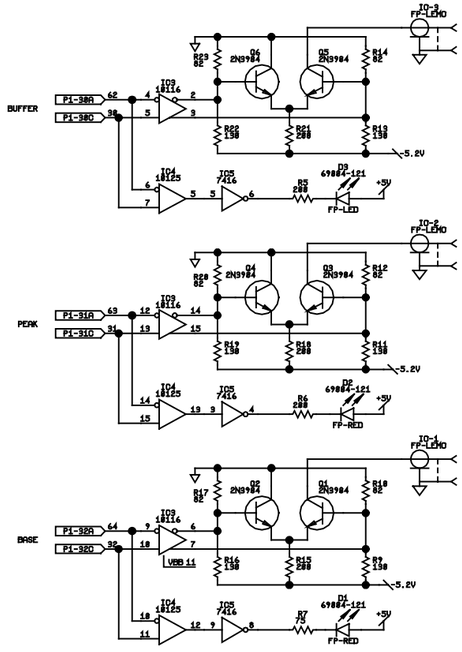
Schematic Diagram

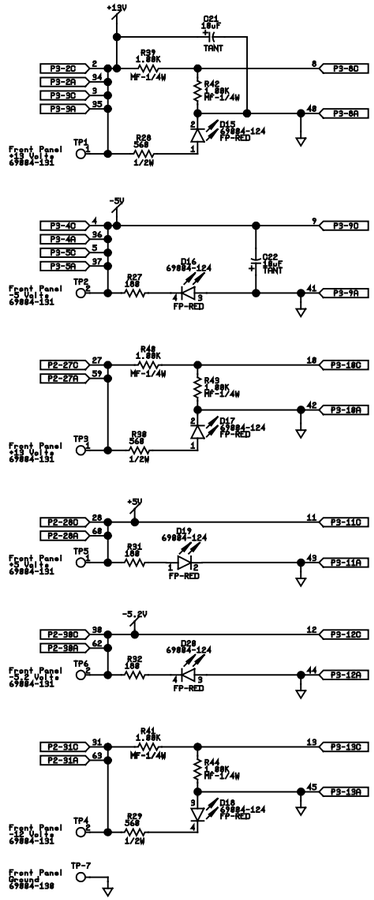


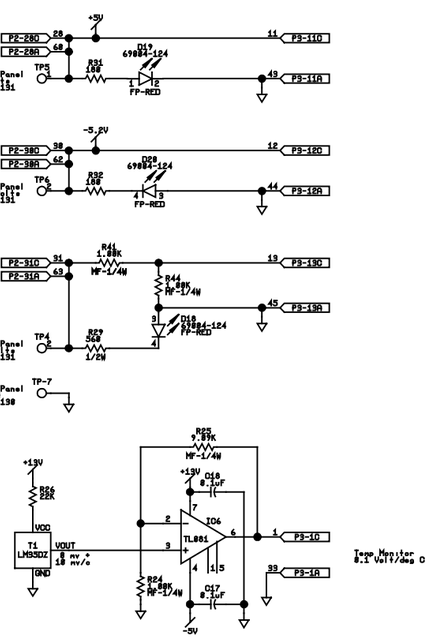
REV.	DESCRIPTION	DRAWN	DATE
		APPD.	DATE
A	CONVERTED TO AUTOCAD	A. KNUDSEN	5/22/00

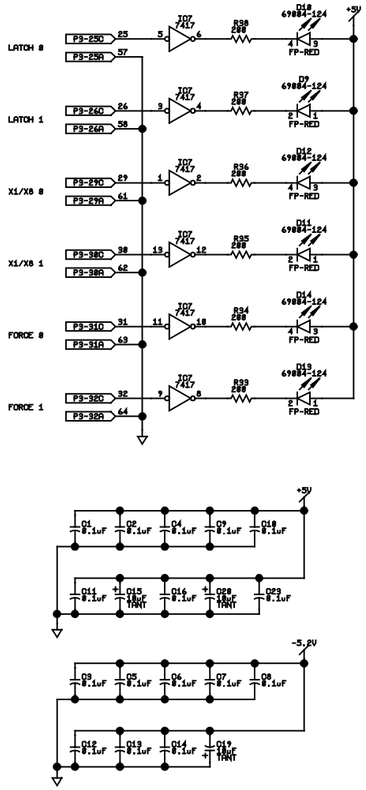
TOP

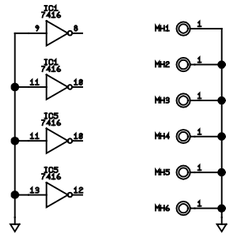


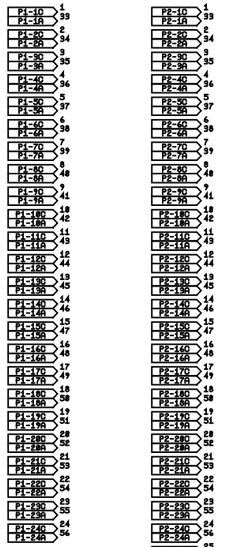


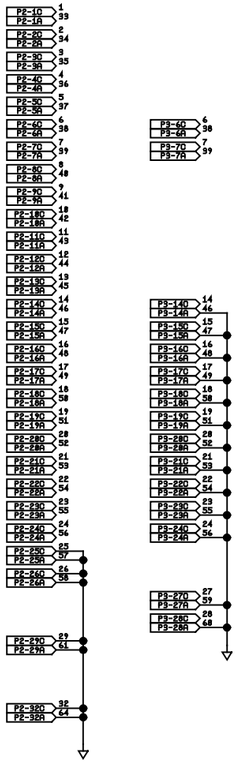












NOTES:

1. ALL RESISTORS ARE ALLEN-BRADLEY, 1/4 WATT, ±5 , HOT-MOLDED FIXED RESISTORS UNLESS OTHERWISE NOTED.
2. RESISTORS MARKED 1/2W ARE ALLEN-BRADLEY, 1/2 WATT, ±5 , HOT-MOLDED FIXED RESISTORS.
3. RESISTORS MARKED MF-1/4W ARE DALE, 1/4 WATT, ±1 , 100ppm/o, METAL FILM RESISTORS.
4. PARTS WITH DESIGNATORS MH1 THROUGH MH6 ARE FRONT PANEL MOUNTING HOLES. THESE HOLES ALLOW THE FRONT PANEL TO BE GROUNDED.

PRINTED CIRCUIT BOARD	
TITLE	DWG NO.
SCHEMATIC	ED-255874
ARTWORK	BD-255875
MASTER DWG	BD-255876
ASSEMBLY DWG	BD-255877
OUTLINE DWG	BD-255878
SOLDER MASK	BD-255879
SILKSCREEN	BD-255880
PARTS LIST	PL-255881

ITEM NO.	PART NO.	DESCRIPTION OR SIZE	QTY. REQ.

PARTS LIST

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	G. KRAFCZYK	8-3-89
FRACTIONS	DECIMALS	ANGLES	DRAWN	G. KRAFCZYK	8-3-89
+/-	+/-	+/-	CHECKED	G. KRAFCZYK	9-25-89
			APPROVED	G. KRAFCZYK	9-25-89

1. BREAK ALL SHARP EDGES 1/64 MAX.
2. DO NOT SCALE DRAWING.
3. DIMENSIONING IN ACCORD WITH ANSI Y14.5 STD S

MAX. ALL MACHINED SURFACE

SCIDESIGN Release 3.8

USED ON

MATERIAL

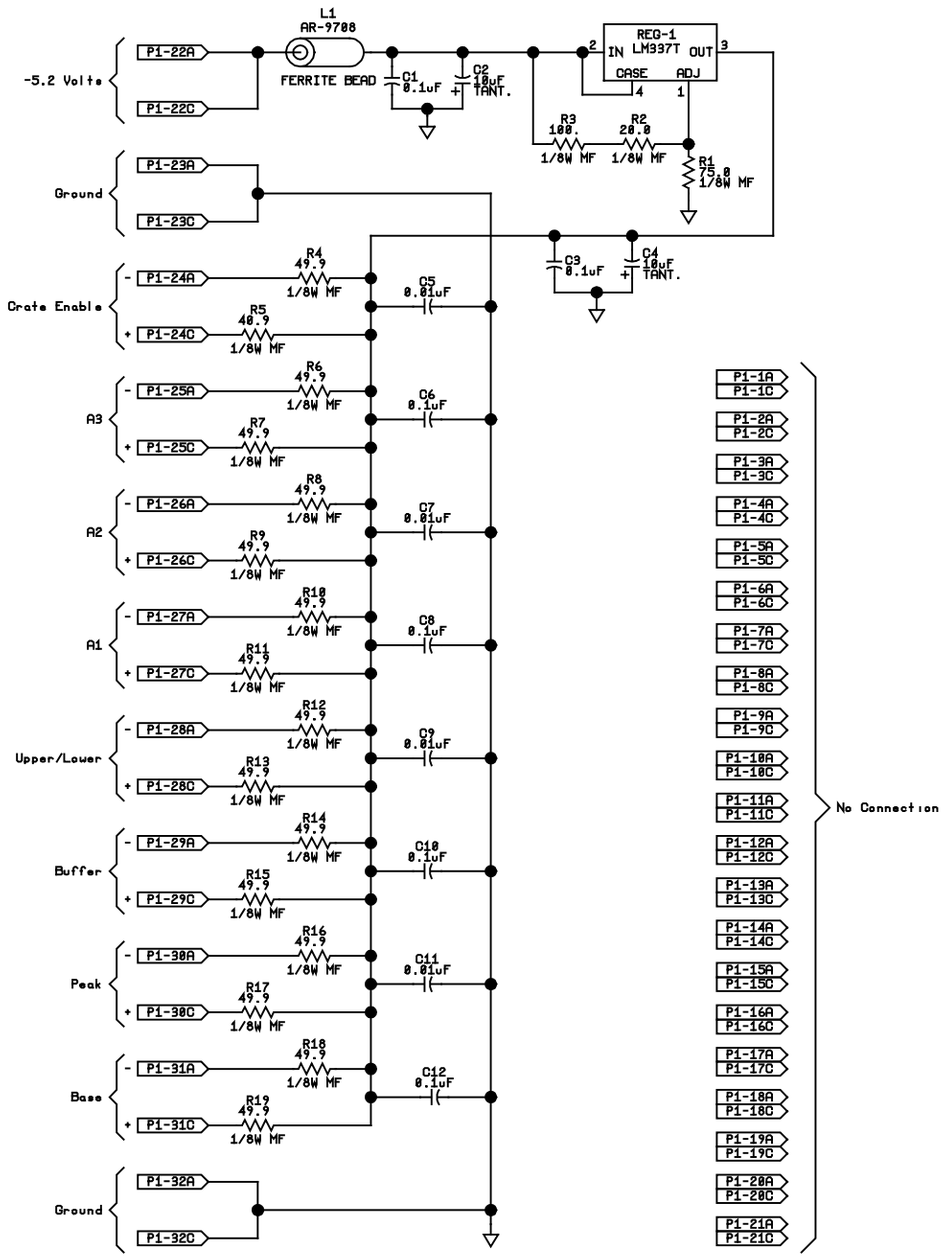
FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

D0 CALORIMETER
BLS CRATE MONITOR
SCHEMATIC

SCALE	FILMED	DRAWING NUMBER	REV.
		3740.412-ED-255874	A

REV.	DESCRIPTION	DRAWN	DATE
		APPD.	DATE
A	CONVERTED TO AUTOCAD	A. KNUDSON	5/22/00

TOP



NOTE:

BACKPLANE CONNECTORS P2 AND P3 ARE NOT USED FOR THIS 9U CARD.

ITEM NO.	PART NO.	DESCRIPTION OR SIZE	QTY. REQ.

PARTS LIST

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	G. KRAFCZYK	9-28-90
FRACTIONS	DECIMALS	ANGLES	DRAWN	G. KRAFCZYK	9-28-90
+/-	+/-	+/-	CHECKED		
			APPROVED		

1. BREAK ALL SHARP EDGES 1/64 MAX.
2. DO NOT SCALE DRAWING.
3. DIMENSIONING IN ACCORD WITH ANSI Y14.5 STD S

MAX. ALL MACHINED SURFACE

SCIDESIGN Release 3.0

USED ON

MATERIAL

PRINTED CIRCUIT BOARD	
TITLE	DWG NO.
SCHEMATIC	EC-255711
ARTWORK	BD-255819
MASTER DWG	BD-286153
ASSEMBLY DWG	BD-286157
OUTLINE DWG	BD-286156
SOLDER MASK	
SILKSCREEN	
PARTS LIST	PL-286155

FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

D0 CALORIMETER
BLS CRATE BUS TERMINATION
ELECTRICAL SCHEMATIC

SCALE	FILMED	DRAWING NUMBER	REV.
		3740.412-EC-255711	A