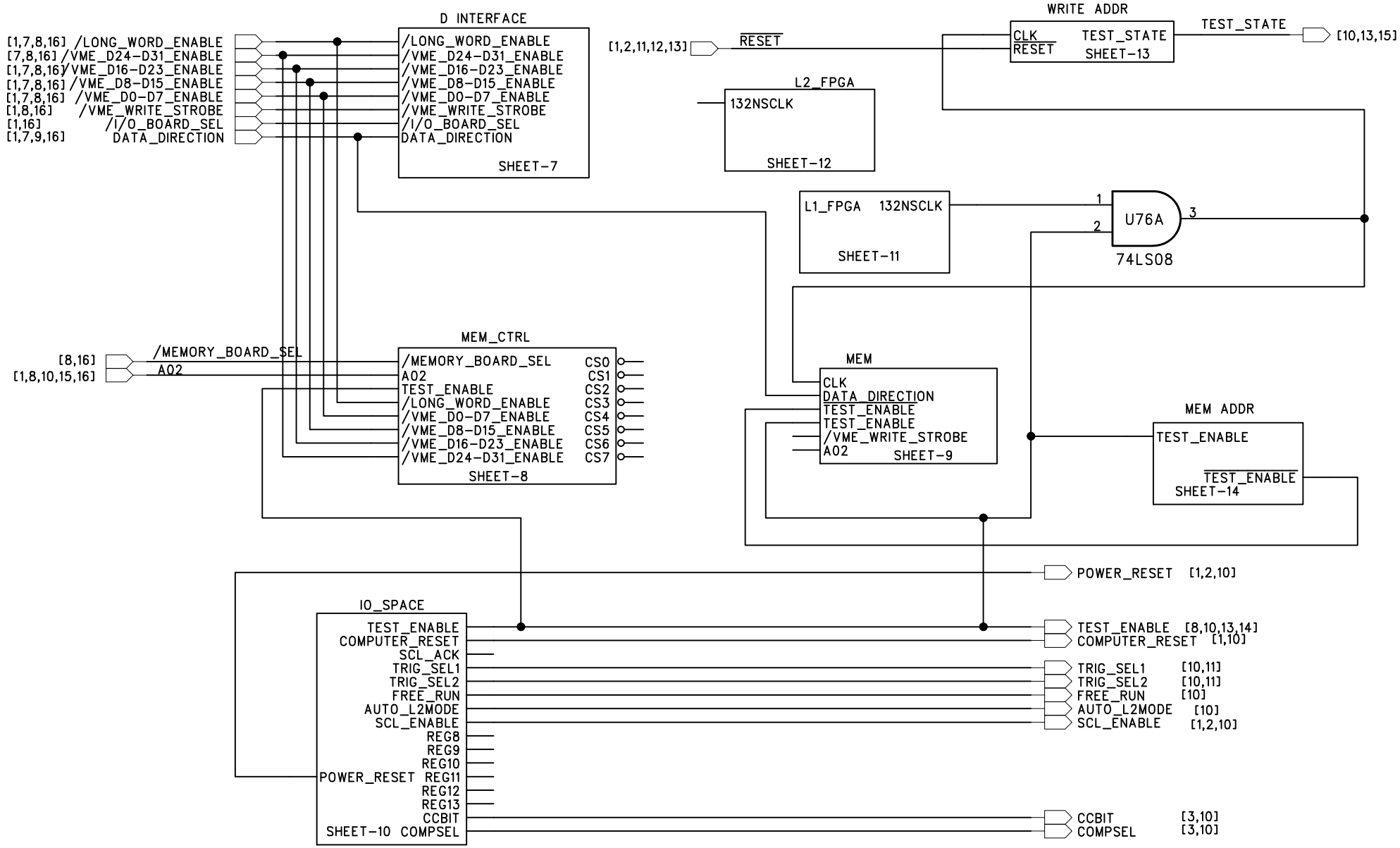
Memory


D INTERFACE
[1,7,8,16] /LONG_WORD_ENABLE
[7,8,16] /VME_D24-D31_ENABLE
[1,7,8,16] /VME_D16-D23_ENABLE
[1,7,8,16] /VME_D8-D15_ENABLE
[1,7,8,16] /VME_D0-D7_ENABLE
[1,8,16] /VME_WRITE_STROBE
[1,16] /I/O_BOARD_SEL
[1,7,9,16] DATA_DIRECTION
/LONG_WORD_ENABLE
/VME_D24-D31_ENABLE
/VME_D16-D23_ENABLE
/VME_D8-D15_ENABLE
/VME_D0-D7_ENABLE
/VME_WRITE_STROBE
/I/O_BOARD_SEL
DATA_DIRECTION
SHEET-7
[1,2,11,12,13] RESET
WRITE ADDR
CLK
RESET
TEST_STATE
SHEET-13
TEST_STATE
[10,13,15]
L2_FPGA
132NSCLK
SHEET-12
L1_FPGA 132NSCLK
SHEET-11
U76A
74LS08
MEM_CTRL
[8,16] /MEMORY_BOARD_SEL
[1,8,10,15,16] A02
/MEMORY_BOARD_SEL
A02
TEST_ENABLE
/LONG_WORD_ENABLE
/VME_D0-D7_ENABLE
/VME_D8-D15_ENABLE
/VME_D16-D23_ENABLE
/VME_D24-D31_ENABLE
CS0
CS1
CS2
CS3
CS4
CS5
CS6
CS7
SHEET-8
MEM
CLK
DATA_DIRECTION
TEST_ENABLE
TEST_ENABLE
/VME_WRITE_STROBE
A02
SHEET-9
MEM ADDR
TEST_ENABLE
TEST_ENABLE
SHEET-14
POWER_RESET [1,2,10]
IO_SPACE
TEST_ENABLE
COMPUTER_RESET
SCL_ACK
TRIG_SEL1
TRIG_SEL2
FREE_RUN
AUTO_L2MODE
SCL_ENABLE
REG8
REG9
REG10
POWER_RESET REG11
REG12
REG13
CCBIT
SHEET-10 COMPSEL
TEST_ENABLE [8,10,13,14]
COMPUTER_RESET [1,10]
TRIG_SEL1 [10,11]
TRIG_SEL2 [10,11]
FREE_RUN [10]
AUTO_L2MODE [10]
SCL_ENABLE [1,2,10]
CCBIT [3,10]
COMPSEL [3,10]