

DFE2
Digital Front End Upgrade Board
Design Specification

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September 20, 2007

Contents

1	Introduction	3
2	DFE2 Architecture	3
2.1	LVDS Inputs	3
2.2	Main FPGA	4
2.2.1	Clocking	4
2.3	Helper FPGA	5
2.3.1	PROM	5
2.4	Temperature Sensor	5
2.5	Serial Number	5
2.6	Flash Memory	5
2.7	Backplane Connection	5
3	Backplane Registers	6
3.1	Base Address	6
3.2	Board Register	6
3.3	Device Register	7
3.4	Configuration Register	7
3.5	Parameter Registers	7
3.6	Test Register	7
3.7	Temperature Registers	7
3.8	Peripheral Status Register	8
3.9	Serial Number Registers	8
3.10	Helper Firmware Version Register	8
4	Slow Monitor Interface	8
5	Front Panel LEDs	9
5.1	LED Serial Bus	9
A	Memory Map	10
B	Backplane Timing	11
C	Backplane Connectors	11
D	Front Panel Connector	11

1 Introduction

The DZERO Central Track Trigger (CTT) is a fast low latency L1 trigger used to identify particle tracks. Due to the tight latency requirements the trigger algorithms are implemented in a massively parallel fashion in hardware. The digital front end (DFE) [3] boards were designed as a scalable modular building block used to construct the backend of the CTT system [2].

Legacy DFE hardware is based upon three field programmable gate array (FPGA) devices soldered to a daughterboard which is bolted to a 6U motherboard. The motherboard plugs into a custom backplane in the DFE crate. Transition boards located behind the backplane enable the DFE boards to drive different media such as fiber optics, copper LVDS cables, and coaxial gigabit copper.

A DFE crate controller (DFEC) resides in the first slot of the crate and uses a CompactFlash card to provide non-volatile storage for the firmware files. The DFEC communicates with the DZERO online system via a 1553 network bus which is nominally 1Mbps. Each DFE motherboard supports a few registers which may be accessed by the DFEC through a simple 8-bit bus; these registers are used for programming the FPGAs, reading status bits, and setting post-initialization parameters (e.g. pipeline depth, mode, etc.). The DFEC also controls a slow serial bus which collects 192 status bits from each DFE board. The string of status bits are placed in a buffer which is read several times a second by the online system.

The Digital Front End Upgrade boards (DFE2) are intended to replace the aging legacy DFE hardware used in the DZERO Central Track Trigger (CTT) system. The multiple field programmable gate array (FPGA) components used on the legacy DFE boards are quickly becoming too costly to replace – newer FPGA devices are cheaper, faster, consume less power, and are rich in resources such as embedded RAMs, FIFOs, and global clock resources. The cost to build a legacy DFE board in 2007 is approximately \$3500 while a DFE2 costs approximately \$600.

2 DFE2 Architecture

The block diagram of the DFE2 board is shown in Figure 1.

2.1 LVDS Inputs

Ten LVDS channel links enter the board through a connector on the front panel as shown in Figure 15. Unlike the legacy DFE boards there are no gaps between the cable connectors and the inputs are numbered straight with input link0 on the top and input link9 on the bottom. The Helper FPGA has the option of disabling the LVDS receiver chips to reduce EMI and reduce power consumption, however it is unlikely that this feature will be implemented in firmware.

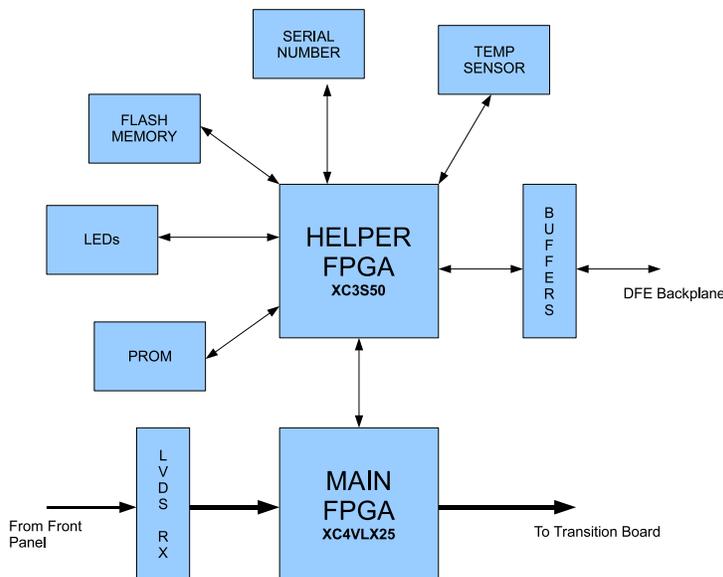


Figure 1: DFE2 Block Diagram

Each LVDS link is 28-bits running at the 53.1047MHz Tevatron RF clock rate (1.486 Gbps). The data format changes depending on the board's location in the trigger chain; for details refer to the DFE Protocols webpage.

2.2 Main FPGA

The physics algorithms are implemented in the firmware which resides in this device. Connections to the Main FPGA have been optimized to maximize data rates through the use of wide parallel buses and fast clocks. The Main FPGA drives four parallel 28-bit buses out to the transition board through the backplane connectors. These four buses are unbuffered on the DFE2 board.

Note that the Main FPGA is a static RAM based FPGA and powers up in a completely erased state.

2.2.1 Clocking

One of the ten LVDS input link clocks is selected to become the DFE2 master clock. The clock selection is handled in the Main FPGA using the clock mux and digital clock manager (DCM) functions. Most of the logic in the Main FPGA is clocked by the master clock. The Main FPGA output buses are synchronous to the master clock and this clock is provided to the transition board.

A 53.125MHz local oscillator (`osc_clk`) is connected to the Main and Helper FPGAs. This clock is used primarily for logic functions that must operate when the input links are not functional (e.g. status logic). The local oscillator may

be selected as the source for the master clock.

Note that if the Main FPGA is erased the master clock will forced to a logic low level!

2.3 Helper FPGA

The Helper FPGA is the device that implements the DFE backplane logic and the “glue logic” that connects the various peripherals together.

2.3.1 PROM

Since the Helper FPGA implements the backplane interface logic it must be programmed before any communication with the board occurs. The PROM device contains the Helper FPGA configuration bitstream and is wired to automatically load the Helper FPGA after a power cycle.

The PROM device is XCF01S a 1Mbit flash memory and is the first device in the JTAG programming chain. Note that this PROM may only be programmed using the front panel JTAG connector and Xilinx programming cable.

2.4 Temperature Sensor

A temperature sensor device (MAX1617) measures both the ambient board temperature and the temperature of the Main FPGA die itself. Note that the Helper does not read the temperatures automatically – the update cycle is triggered by a write to either of the temperature backplane registers. Temperatures are reported in degrees centigrade.

2.5 Serial Number

Each DFE2 board features a serial number chip (DS2041) which contain a unique 48-bit number. The board serial number may be read back at any time from the backplane registers. The Helper FPGA reads out this “one wire” device and performs a CRC check immediately after a hard reset or power cycle.

2.6 Flash Memory

A small serial 8Mbit flash memory is attached to the Helper FPGA. This memory has enough capacity to store a single Main FPGA configuration bitstream. At present time this feature is not supported by the Helper firmware.

2.7 Backplane Connection

The DFE2 boards are compatible with the legacy DFE backplane. The +5V power pins are unused and the +3.3V backplane power pins are fused per Fermilab / DZERO safety guidelines [1]. Most signals going to and coming from the backplane are buffered. The backplane pinout is shown in Appendix X.

Initial power consumption estimates are 3W quiescent and 6W active.

Slot	Base Address	Slot	Base Address
2	0x0200	12	0x0C00
3	0x0300	13	0x0D00
4	0x0400	14	0x0E00
5	0x0500	15	0x0F00
6	0x0600	16	0x1000
7	0x0700	17	0x1100
8	0x0800	18	0x1200
9	0x0900	19	0x1300
10	0x0A00	20	0x1400
11	0x0B00	21	0x1500

Figure 2: DFE crate base addresses.

7	6	5	4	3	2	1	0
Board Type = 0000				0	TRST	RST	RDY

Figure 3: The Board Register

3 Backplane Registers

The DFE Crate Controller is the master of a simple 16-bit address 8-bit data bus. This bus supports read and write operations and is synchronous to a 12MHz backplane clock. Registers may be read or written to at any time. In the following register figures read only bits are indicated by a shaded box while the boxes with a white background are read/write.

3.1 Base Address

The base address of each DFE board is determined by the slot position. The slot number becomes the upper byte of the board's base address. Refer to Figure 2 for details.

3.2 Board Register

The Board Register is located at BASE+0 and is shown in Figure 3. The RDY bit is set when the Main FPGA has been successfully programmed and raised the DONE pin.

TRST and RST are self-clearing bits. Set the TRST bit to hard reset ONLY the transition board. This is useful when the G-LINK transmitters are behaving badly. Setting the RST bit will hard reset the DFE2 board and the transition board. The Board Type field is no longer used and reads back 0000.

7	6	5	4	3	2	1	0
DONE	PROG	CERR	1	Device Select			

Figure 4: The Device Register

3.3 Device Register

The Device Register is at BASE+1 selects the current device (the DFE2 supports one device, 0000). The DONE bit is set when the Main FPGA has been successfully programmed and raised the DONE pin – this is a copy of the RDY bit in the Board Register.

Setting the PROG bit will erase the Main FPGA and this bit must be explicitly cleared before programming begins. If at any time during programming the Main FPGA detects an error (such as a failed CRC check) the CERR bit will be set. Once set the CERR will remain set until a hard reset or an new programming cycle is started by setting and clearing the PROG bit. Refer to Figure 4 for details.

3.4 Configuration Register

The Main FPGA configuration bitstream is written to this register which is at BASE+2. Reading from this register will return the last value written.

3.5 Parameter Registers

The DFE2 supports eight parameter registers located at BASE+3, BASE+4, BASE+5, BASE+6, BASE+8, BASE+9, BASE+0xA, and BASE+0xB. Data written to these registers is serialized in the Helper and passed to the Main FPGA after it has been programmed. These registers are application specific and determined by the Main FPGA firmware.

3.6 Test Register

The Test Register is located at BASE+7 and is a dummy register, meaning that it does nothing useful. Reading this register will return the last value written. A hard reset will force this register to zero.

3.7 Temperature Registers

The DFE2 board monitors the ambient temperature and the temperature of the Main FPGA die. These temperatures are reported in degrees centigrade at BASE+0xD and BASE+0xE respectively.

The temperature registers are not updated automatically. Write any value to either temperature register to trigger an update.

7	6	5	4	3	2	1	0
0	0	SERNO ERROR	SERNO BUSY	0	0	TEMP ERROR	TEMP BUSY

Figure 5: The Peripheral Status Register

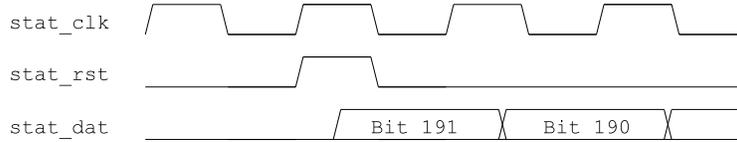


Figure 6: The Slow Monitor Interface Signals

3.8 Peripheral Status Register

The Peripheral Status Register is located at $\text{BASE}+0xC$ and is read-only. The status of the serial number device and temperature sensor is reported here. Refer to Figure 5 for details.

3.9 Serial Number Registers

The 48-bit board serial number is reported at $\text{BASE}+0xF$ (least significant byte) to $\text{BASE}+0x14$ (most significant byte).

3.10 Helper Firmware Version Register

The version number of the Helper firmware is reported at $\text{BASE}+0x15$.

4 Slow Monitor Interface

The DFEC continuously collects 192 status bits from each DFE board and stores these bits in a buffer that is periodically read by the online system (in EPICs this is called MBSTAT). The status bits are sent serially using three signals: `stat_clk`, `stat_rst`, and `stat_dat`. The status bits are sent back to the DFEC most significant bit (191) first as shown in Figure 6. The clock frequency is 750kHz, hence the name *slow* monitor interface.

Once the Main FPGA is programmed the Helper FPGA simply passes the `stat_clk`, `stat_rst`, and `stat_dat` signals through to the Main FPGA. If the Main FPGA is not programmed the `stat_dat` signal (which goes back to the DFEC) is forced to zero.

- +3.3V
- +2.5V
- +1.2V
- READY
- 0: Temperature Busy
- 1: Temperature Error
- 2: Serial Number Error
- 3:
- 4: Erasing Main FPGA
- 5: Writing Configuration Register
- 6: Configuration Error
- 7:
- 8: Parameter Write
- 9: DTACK

Figure 7: Front Panel LEDs in Status Page 0.

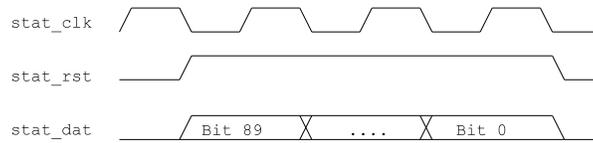


Figure 8: LED serial bus timing.

5 Front Panel LEDs

The DFE2 front panel features three red leds for the power indicators (+3.3V, +2.5V, and +1.2V). The next LED is a green “Ready” LED. The ready LED is solid on when the Main FPGA is programmed, otherwise it blinks slowly.

The remaining ten LEDs are firmware-defined and divided into ten status “pages”. Advancing to the next status page requires tapping the reset button. After the button is pushed the ten yellow LEDs will briefly indicate the current status page, then go dark, and then the status bit LEDs will “fade in”.

Status page 0 is reserved for Helper status bits and is shown in Figure 7.

5.1 LED Serial Bus

Once the Main FPGA is programmed the Helper FPGA begins the process of collecting 90 status bits from the Main FPGA. These 90 status bits will become LED status pages 1-9. These status bits are defined by the Main FPGA firmware and are completely separate from the 192 “slow monitor” status bits.

The LED bits are shifted out Main FPGA serially synchronously to 53.125MHz `osc_clk` most significant bit first as shown in Figure 8.

Data bit 89 will become the most significant bit of status page 9 and bit 0 will become the least significant bit of status page 1.

A Memory Map

The DFE2 registers are shown in Figure 9. White cells are read/write, grey cells are read only, and yellow cells are read/write and self-clearing.

OFFSET \ BIT	7	6	5	4	3	2	1	0
0x00	board type = 0000				0	Trans reset	reset	ready
0x01	done	prog	Config error	1	device select			
0x02	configuration data							
0x03	reserved for parameter 0							
0x04	reserved for parameter 1							
0x05	reserved for parameter 2							
0x06	reserved for parameter 3							
0x07	Test register							
0x08	reserved for parameter 4							
0x09	reserved for parameter 5							
0x0A	reserved for parameter 6							
0x0B	reserved for parameter 7							
0x0C	0	0	semo error	semo busy	0	0	temp error	temp busy
0x0D	ambient temperature in deg C							
0x0E	main FPGA die temperature in deg C							
0x0F	serial number byte 0 (LSB)							
0x10	serial number byte 1							
0x11	serial number byte 2							
0x12	serial number byte 3							
0x13	serial number byte 4							
0x14	serial number byte 5 (MSB)							
0x15	Helper FPGA firmware version							

Figure 9: DFE2 memory map.

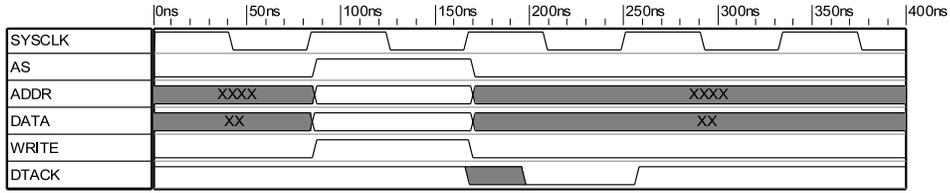


Figure 10: DFE backplane bus write cycle.

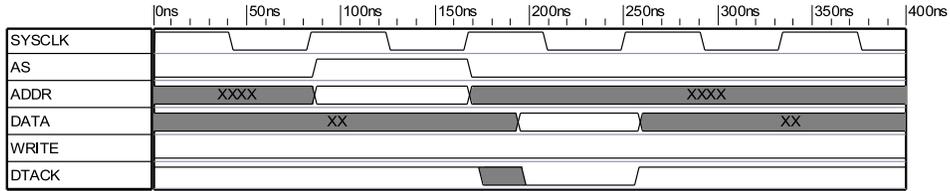


Figure 11: DFE backplane bus read cycle.

B Backplane Timing

A simple bidirectional 8-bit data 16-bit address bus is used for communication between the DFEC and the DFE2 board. This bus is synchronous to a 12MHz backplane clock. A write cycle is shown in Figure 10. Each write operation requires two clock cycles: the address and data lines are registered on the first rising edge and the DTACK signal is sampled on the following rising edge of the backplane clock.

The read cycle is shown in Figure 11. Each read cycle requires 3 clock cycles. The address bits are registered on the rising edge of the backplane clock (180ns) and the DTACK signal is sampled on the following rising edge. There is a single cycle wait state following each read cycle.

C Backplane Connectors

The DFE2 backplane connectors are composed of three “hard metric” connectors type A, B, and C. The type A connector is at the top of the backplane and the type C connector is at the bottom. The backplane connectors are used for power as well as communication with the DFEC and transition board. The connector pinouts are shown in Figure 12, Figure 13, and Figure 14.

D Front Panel Connector

Ten LVDS cables plug into the DFE2 front panel connector as shown in Figure 15. Note that unlike the legacy DFE motherboard there are no gaps in between connectors and there are no flips in the cable numbering.

	A	B	C	D	E
2		TOP_MUON_27		TOP_MUON_26	
3	TOP_MUON_25	TOP_MUON_24	TOP_MUON_23	TOP_MUON_22	TOP_MUON_21
4	TOP_MUON_20		TOP_MUON_19		TOP_MUON_18
5	TOP_MUON_17	TOP_MUON_16	TOP_MUON_15	TOP_MUON_14	TOP_MUON_13
6		TOP_MUON_12		TOP_MUON_11	
7	TOP_MUON_10	TOP_MUON_9	TOP_MUON_8	TOP_MUON_7	TOP_MUON_6
8	TOP_MUON_5		TOP_MUON_4		TOP_MUON_3
9	TOP_MUON_2	TOP_MUON_1	TOP_MUON_0		
KEY					
		TOP_L1L2_27	+3.3V	TOP_L1L2_26	
16	TOP_L1L2_25	TOP_L1L2_24	TOP_L1L2_23	TOP_L1L2_22	TOP_L1L2_21
17	TOP_L1L2_20	+3.3V	TOP_L1L2_19	+3.3V	TOP_L1L2_18
18	TOP_L1L2_17	TOP_L1L2_16	TOP_L1L2_15	TOP_L1L2_14	TOP_L1L2_13
19	+3.3V	TOP_L1L2_12	+3.3V	TOP_L1L2_11	
20	TOP_L1L2_10	TOP_L1L2_9	TOP_L1L2_8	TOP_L1L2_7	TOP_L1L2_6
21	TOP_L1L2_5		TOP_L1L2_4		TOP_L1L2_3
22	TOP_L1L2_2	TOP_L1L2_1	TOP_L1L2_0	DATA0	
23				DATA1	
24	DATA2	DATA3	DATA4		CLOCK
25			DATA5		

Figure 12: DFE2 backplane connector type A.

1	+3.3V	DATA6	+3.3V	DATA7	BPCLK
2		SYSRST_N			WRITE
3		+3.3V			
4		AS			
5	+3.3V	A15		A7	
6	A14	A6	A13	A5	A12
7	A4	+3.3V	A11		
8	A3	A10	A2	A9	
9	+3.3V	A1	+3.3V	A8	
10	A0	SLOT0	SLOT1	SLOT2	SLOT3
11	SLOT4		SLOT2		DTACK
12					
13			STAT_RST	STAT_CLK	STAT_DAT
14					
		BOT_MUON_27		BOT_MUON_26	
16	BOT_MUON_25	BOT_MUON_24	BOT_MUON_23	BOT_MUON_22	BOT_MUON_21
17	BOT_MUON_20	+3.3V	BOT_MUON_19	+3.3V	BOT_MUON_18
18	BOT_MUON_17	BOT_MUON_16	BOT_MUON_15	BOT_MUON_14	BOT_MUON_13
19	+3.3V	BOT_MUON_12		BOT_MUON_11	
20	BOT_MUON_10	BOT_MUON_9	BOT_MUON_8	BOT_MUON_7	BOT_MUON_6
21	BOT_MUON_5	+3.3V	BOT_MUON_4		BOT_MUON_3
22	BOT_MUON_2	BOT_MUON_1	BOT_MUON_0	BOT_L1L2_27	BOT_L1L2_26
23	+3.3V	BOT_L1L2_25	+3.3V	BOT_L1L2_24	
24	BOT_L1L2_23	BOT_L1L2_22	BOT_L1L2_21	BOT_L1L2_20	BOT_L1L2_19
25	BOT_L1L2_18		BOT_L1L2_17	+3.3V	BOT_L1L2_16

Figure 13: DFE2 backplane connector type B.

1					
3	+3.3V	BOT_L1L2_10	+3.3V	+3.3V	BOT_L1L2_9
4	BOT_L1L2_8	+3.3V	+3.3V	BOT_L1L2_7	BOT_L1L2_6
5	BOT_L1L2_5	BOT_L1L2_4	BOT_L1L2_3		
6	+3.3V	BOT_L1L2_2			
7	BOT_L1L2_1	BOT_L1L2_0			
8					
					RESET_N

Figure 14: DFE2 backplane connector type C.

A	B	C	D	E	
D1	D1*		D2	D2*	LINK 0
D0*	D0		CLK	CLK*	
			D3	D3*	
D1	D1*		D2	D2*	LINK 1
D0*	D0		CLK	CLK*	
			D3	D3*	
D1	D1*		D2	D2*	LINK 2
D0*	D0		CLK	CLK*	
			D3	D3*	
D1	D1*		D2	D2*	LINK 3
D0*	D0		CLK	CLK*	
			D3	D3*	
D1	D1*		D2	D2*	LINK 4
D0*	D0		CLK	CLK*	
			D3	D3*	
D1	D1*		D2	D2*	LINK 5
D0*	D0		CLK	CLK*	
			D3	D3*	
D1	D1*		D2	D2*	LINK 6
D0*	D0		CLK	CLK*	
			D3	D3*	
D1	D1*		D2	D2*	LINK 7
D0*	D0		CLK	CLK*	
			D3	D3*	
D1	D1*		D2	D2*	LINK 8
D0*	D0		CLK	CLK*	
			D3	D3*	
D1	D1*		D2	D2*	LINK 9
D0*	D0		CLK	CLK*	
			D3	D3*	

Figure 15: DFE2 front panel connector.

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