

CTOC

Firmware Specification

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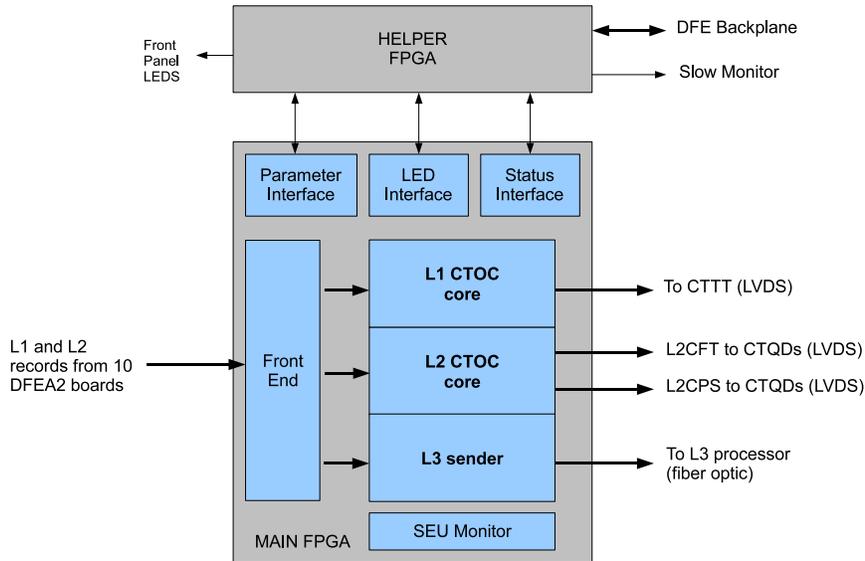


Figure 1: The CTOC block diagram.

1 Introduction

The CTOC boards collect L1 and L2 data from the DFEA2 boards and output data to the CTTT, CTQDs, and the L3 readout crate. The CTOC boards are a part of the DZERO Central Track Trigger (CTT) system [1].

The previous incarnation of the CTOC board used a DFE motherboard and a double-wide daughterboard which contained three medium sized Field Programmable Gate Arrays (FPGAs). The legacy DFE hardware was replaced in 2007 with the DFE2 board which contains one large main FPGA and a small helper FPGA [2]. The helper FPGA implements the DFE backplane logic and is rather generic, meaning that the overall “flavour” of the board is determined exclusively by the firmware loaded into the main FPGA. This document describes the CTOC firmware that has been rewritten for the DFE2 board architecture.

2 Block Diagram

The block diagram of the CTOC firmware is shown in Figure 1.

2.1 Front End

Each upstream DFEA2 board sends L1 and L2 records to the CTOC board over an LVDS link. Each LVDS link uses an embedded 53MHz clock to synchronize the serial data stream which runs at 1.7 Gbps. The purpose of the front end

block is to select one of the ten input link clocks and distribute that clock as the master board clock. Small dual-port RAMs are used to cleanly cross from the link clock domains into the master clock domain. The data streams are continuously resynchronized by detecting the beginning of record (BOR) marker.

A counter in the front end keeps track of the tick and turn numbers by checking the embedded SCLimit and First Crossing (FX) control bits in the synchronized data streams. The tick turn counter continuously checks the FX bit to insure that it is properly aligned with the data streams – if it is aligned the `Tick turn counter locked` status bit is asserted. Note that this locked bit is different than the `Master clock DCM locked` status bit.

The front end block also contains logic to check that the synchronized data streams are properly aligned. The master BOR marker and control bits are determined by simple majority logic in the front end.

2.1.1 Clock Selection

One of the ten input link clocks must be selected to be the master board clock simply by writing to a the master link backplane register. The clock selection logic resides in the main FPGA where dedicated low skew routing resources, clock multiplexers, and digital delay locked loops (DLLs) are used.

Care must be taken to avoid discontinuities in the clock signal which is fed into the FPGA’s Digital Clock Manager (DCM) unit. If the DCM input clock changes suddenly (e.g. an upstream DFEA2 board is reprogrammed, the master link register is changed, etc.) the DCM *may* lose lock. When a DCM is unlocked the output clock stability is not guaranteed and the data from the CTOC will be garbage. The DCM locked status is reported in the status bits. The DCM may be reset by writing to the DCM reset backplane register.

2.2 L1 CTOC Core

The CTOC normally receives ten L1 records from the upstream DFEA2 boards. These records contain occupancy information as well as CFT track counts and isolated track information. In L1 mode the CTOC sums the track counts and occupancy data and passes this information downstream to the CTTT boards. The L1 core design is heavily pipelined with a fixed latency of 371 ns. For more information on the data fields in the L1 records refer to the DFE Protocols website [3].

When a L1accept is issued the CTOC suspends L1 record transmission momentarily and sends a “dummy” L2 record downstream to the CTTT boards as shown in Figure 2. This dummy record is used to inform the CTTT that a L1accept has occurred. The dummy record consists of an L2 header (0xE000028, 0x1123456) followed by a parity word (0x012347E) and 46 null frames.

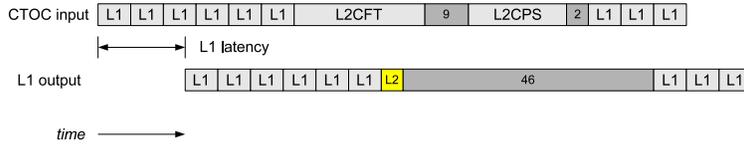


Figure 2: CTOC L1 output latency.

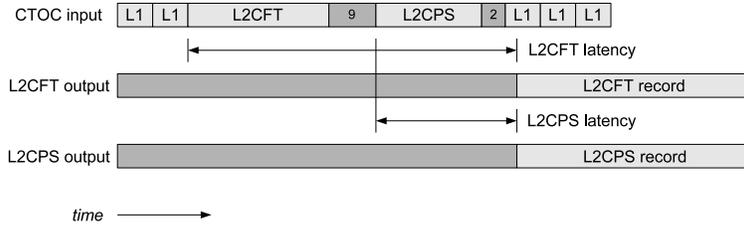


Figure 3: CTOC L2CFT and L2CPS output latency.

2.3 L2 CTOC Core

When a L1accept is issued the upstream DFEA2 boards “jump back” to the event in question and produce lists of CFT axial tracks and CPS axial clusters. L1 record transmission is interrupted as the L2CFT and L2CPS records are sent to the CTOC.

Incoming L2CFT records may contain up to 24 tracks and they are sorted by pT. The L2 CTOC core logic concatenates and sorts the tracks and up to 24 of the highest pT tracks are sent downstream to the CTQD.

Incoming L2CPS records contain up to 8 CPS axial clusters sorted by phi value. These clusters are sorted in the CTOC L2 core logic and reported sorted in order of increasing phi. The resulting L2CPS record is sent downstream to the CTQD.

The outgoing L2CFT record is delayed so that it is aligned with the outgoing L2CPS record as shown in Figure 3. The L2CFT latency is 1029 ns and the L2CPS latency is 353 ns. When the L2CFT and L2CPS outputs are not transmitting their respective L2 records the links send all zeros.

2.4 L3 Sender

In the CTOC a L1accept is signaled by the arrival of the L2CFT record. In response to the L1accept the L3 sender module “jumps back” PIPE_DEPTH 132ns crossings and concatenates the ten L1 input records into a L3 record which is sent downstream to the L3 readout crate. The CTOC supports pipeline depths from 0 to 63. If the pipeline depth is set to zero the L3 record will contain the first seven frames of the L2CFT records. The L3 output latency is 334 ns as shown in Figure 4. For more information refer to the DFE Protocols website [3].

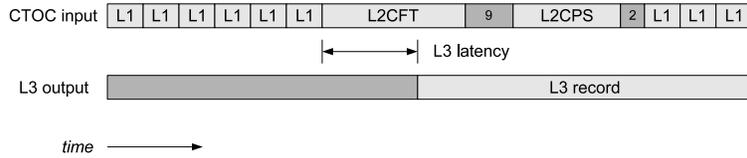


Figure 4: CTOC L3 output latency.

Mode	Description
0	Normal data (default)
1	Send empty L1 records
2-13	reserved
14	Send all zeros
15	Send special L1 link test pattern

Table 1: CTOC L1 test modes.

2.5 Parameter Interface

After the main FPGA is programmed it is necessary to write (and verify) operating parameters such as the pipeline depth, operation modes, and octant number. These parameters are written to backplane registers and may be read back for verification at any time. Many of these parameters are reported back via the status interface.

2.5.1 Pipeline Depth

Specifies the L3 sender depth in 132 ns crossings. Valid numbers are from zero to 63 with the power on default being 37. The pipeline depth may be changed by writing to backplane register offset 3.

2.5.2 Test Modes

The L1 and L2 core logic modules each contain various test modes which are useful for debugging. The power on default value is zero and in both cases is corresponds to normal data taking mode. The L1 test modes are defined in table 1 and may be changed by writing to backplane register offset 4. The L2 test modes are defined in Table 2 and may be changed by writing to backplane register offset 6.

2.5.3 Error Persistence

Many of the status bits are “glitchy” by their nature and very difficult to observe directly. The status interface logic pulse stretches some of these signals for n seconds, where n is determined by this register. Set this register to zero for infinite persistence, which is useful for debugging. Normally EPICs reads the

Mode	Description
0	Normal data (default)
1	L2CFT incrementing track
2-15	reserved

Table 2: CTOC L2 test modes.

status bits at 10 Hz so setting this register to 1 or more seconds is enough for the online system to catch momentary intermittent errors. The upper limit is 15 seconds and the power on default value is 1 second. This register may be changed by writing to backplane register offset 9.

2.5.4 Home Octant

Each CTOC needs to be told what its home octant is. Valid numbers are zero through seven and they follow the slot numbers in the crate (slot2 = octant 0, etc.). The home octant may be changed by writing to backplane register offset 5.

2.5.5 Master Link

Write to this register to specify which input link clock is to be used as the master board clock. Valid numbers are zero through nine. Be sure to check the **Master clock DCM locked** status bit (see Table 3) when changing this register. The default value is zero. The master link may be changed by writing to backplane register offset 8.

2.5.6 DCM Reset

Write anything to backplane register offset ten (“cmd writebyte A” in DFE-Ware) to force a reset of the DCM clock module. Do this only if the **Master clock DCM locked** status bit is zero. Typically the DCM will unlock if the upstream DFEA2 boards are erased or if the master link register is changed. Reading this register will return zero.

2.6 Status Interface

Every few hundred milliseconds the DFE crate controller (DFEC) requests 192 bits of status data from each DFE board in the crate. This “slow monitor” process runs automatically without any user intervention. The DFEC writes the status bits into a dual-port buffer which is read periodically by the DZERO online EPICS system. The CTOC status bits are shown in Table 3.

Bit Position	Description
191:188	Header 1000
187:178	L1accept link error
177:168	FX link error
167:158	SCLinit link error
157:148	Parity link error
147:138	L1 pattern link error
137:128	Synchronization link error
127:118	Clock link error
117:112	L3 pipeline depth
111	L1accept detect
110	FX detect
109:106	L1 mode
105	Tick turn counter error
104	Tick turn counter locked
103	SCLinit detect
102	Master clock DCM locked
101:99	Home octant
98:92	Trailer 101 + header 1000
91:82	L2 object link error
81:80	reserved, zero
79:72	Firmware version
71:62	Johnson pattern link error
61:56	reserved, zero
55:52	Master link selection
51:42	Tick turn link error
41:32	Header timeout link error
31:22	FPGA core temperature
21:12	Octant link error
11	SEU detected
10	SEU monitor active
9:6	L2 mode
5:3	Home octant (repeated)
2:0	Trailer 101

Table 3: CTOC status bits.

2.6.1 First Crossing, SCLinit, and L1accept Link Errors

Each input link contains embedded control bits for FX and SCLinit. After synchronizing the data streams the front end module votes to determine the master FX, SCLinit, and L1accept control bits. The vote result is exclusive-OR'ed against the embedded link bits and if there is a difference the corresponding bit will be flagged.

2.6.2 Parity and Pattern Link Errors

Incoming L1 and L2 records have both vertical and horizontal parity bits which are checked by the front end and reported in the status bits. Two types of patterns are used to exercises all of the link bits The Johnson counter pattern is a simple rotating pattern across all 28 bits of the of LVDS link. The L1 link test pattern contains a walking one pattern wrapped in a L1 record. The patterns must be enabled by writing to the upstream DFEA2 boards.

2.6.3 Clock, Sync, and Timeout Link Errors

The front end firmware contains logic to compare the link clock against a known frequency reference. If a link clock frequency is not within approximately 5% of nominal the corresponding clock error bit is set. If a L1 or L2 header is not observed on a link within 32 clock cycles the corresponding header timeout link error bit is set. Under normal conditions the synchronized data streams should be aligned with the global beginning of record signal. If a link data stream is not properly aligned with BOR the corresponding bit in the synchronization link error is set.

2.6.4 Tick Turn Counter Status Bits

If the tick turn counter is not locked issue an SCLinit. The tick turn counter expects to see the FX control bit asserted in crossing number 7 – if this is not the case the tick turn error bit is set. Usually if the tick turn counter is out of sync it just needs an SCLinit.

Each incoming L2CFT and L2CPS record contains the tick and turn numbers. These numbers are compared in the L2 core and if there are differences the corresponding error bits are set in the tick turn link error field. Since the L2CFT and L2CPS records are variable length it is very important to insure that the number of objects field is correct and thus this field has special parity bits associated with it. If there is an error in these parity bits, or the number is out of range the corresponding bit in the Object link error field is set.

2.6.5 Temperature Status

The DFE2 board contains a special sensor chip that continuously monitors the die temperature of the main FPGA. The FPGA core temperature is reported back in degrees Celsius.

LED \ PAGE	0	1	2	3	4	5	6	7	8	9	
0	Reserved for helper status bits	Link Clock Error	Link Timeout Error	Link Parity Error	Link Pattern Error	Link Sync Error	Master Link	Pipeline Depth	L2 Mode	Firmware Version	
1							Reset DCM		0		
2							0		0		
3							0		0		
4							link0		link0		link0
5							:		:		:
6							:		:		:
7							:		:		:
8							link9		link9		link9
9							:		:		:
							Octant	0	L1 Mode	0	
							TTC Lock	0		0	

Figure 5: LED status pages.

2.7 LED Interface

The DFE2 front panel features ten user defined LEDs which are multiplexed into ten “pages” each containing ten status bits. Each LED is driven by a digital “one shot” to stretch the pulse wide enough so that momentary glitches are observable by the human eye.

Tapping the front panel reset button cycles through the ten LED pages. Hold the reset button down for more than two seconds to force a hard reset of the board.

The default page (page0) displays status bits from the helper FPGA and are described in the DFE2 board specification document. The remaining 90 LED status bits are continuously sent from the main FPGA to the helper FPGA and appear as LED status pages 1 through 9. These status bits are shown in Table 5. Note that the front panel LEDs are arranged zero (LSb) on the top to nine (MSb) on the bottom.

2.8 Single Event Upset Monitor

The configuration bits which determine the operation of the main FPGA are stored in static RAM. A single event upset (SEU) bit error could alter the firmware operation and could even damage the device. Xilinx has produced a slick embedded processor that continuously scans the configuration memory of the FPGA checking for SEU errors. If an error is found an status bit is asserted and the bit error is repaired if possible. This module runs continuously “in the background” and has no affect on device operation. In a sense the main FPGA becomes another “silicon detector” in the experiment.

References

- [1] J. Olsen et al., "The DØCentral Track Trigger," IEEE Trans. Nucl. Sci., vol. 51, pp. 345-350, June 2004.
- [2] DFE2 Design Specification
<http://www-d0.fnal.gov/hardware/dfe/dfe2>
- [3] DFE Hardware and Firmware Homepage
<http://www-d0.fnal.gov/hardware/dfe>