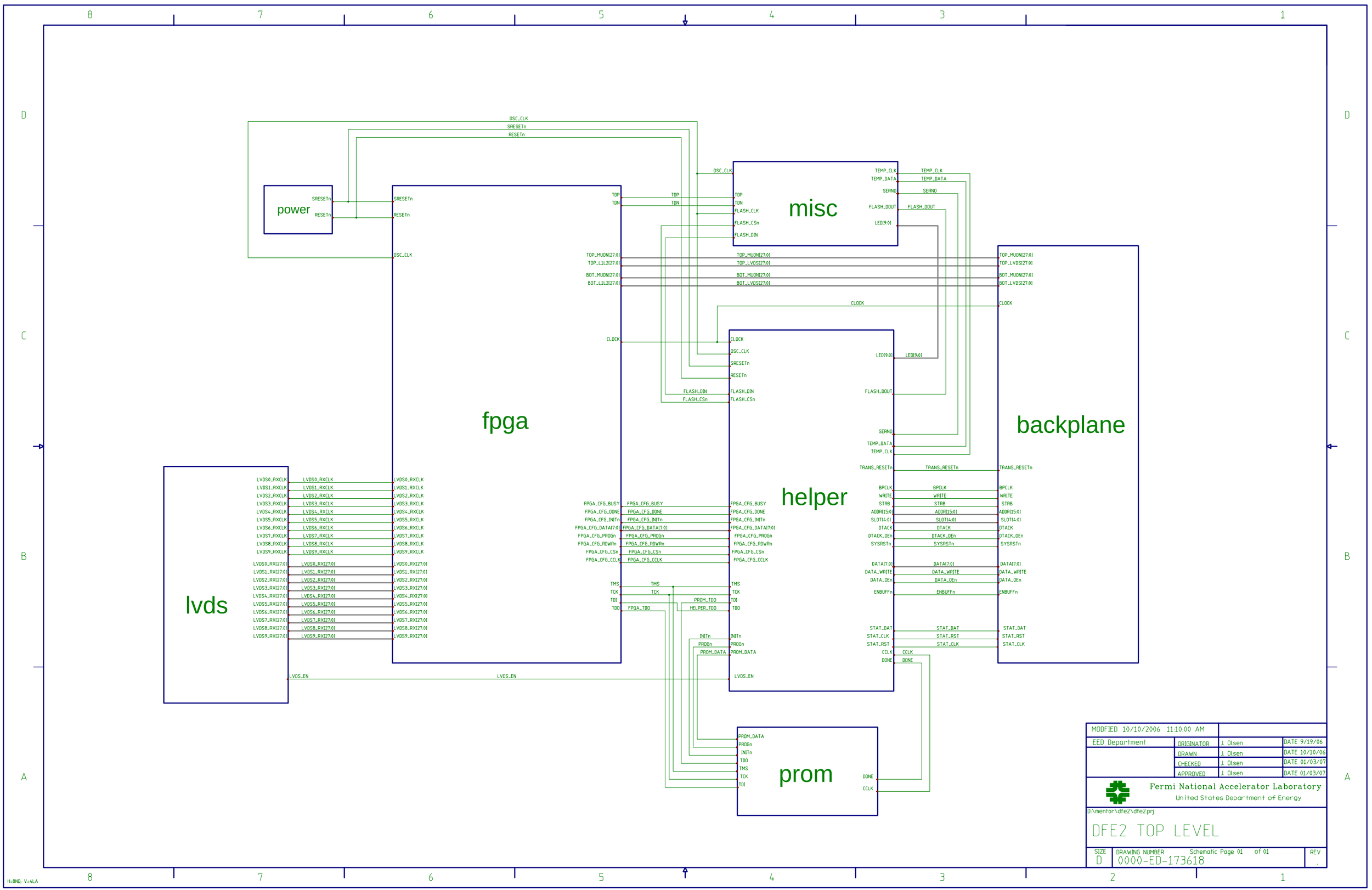

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EED Department	ORIGINATOR	J. Olsen	DATE 9/19/06
	DRAWN	J. Olsen	DATE 10/10/06
	CHECKED	J. Olsen	DATE 01/03/07
	APPROVED	J. Olsen	DATE 01/03/07

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DFE2 TOP LEVEL

SIZE	DRAWING NUMBER		REV
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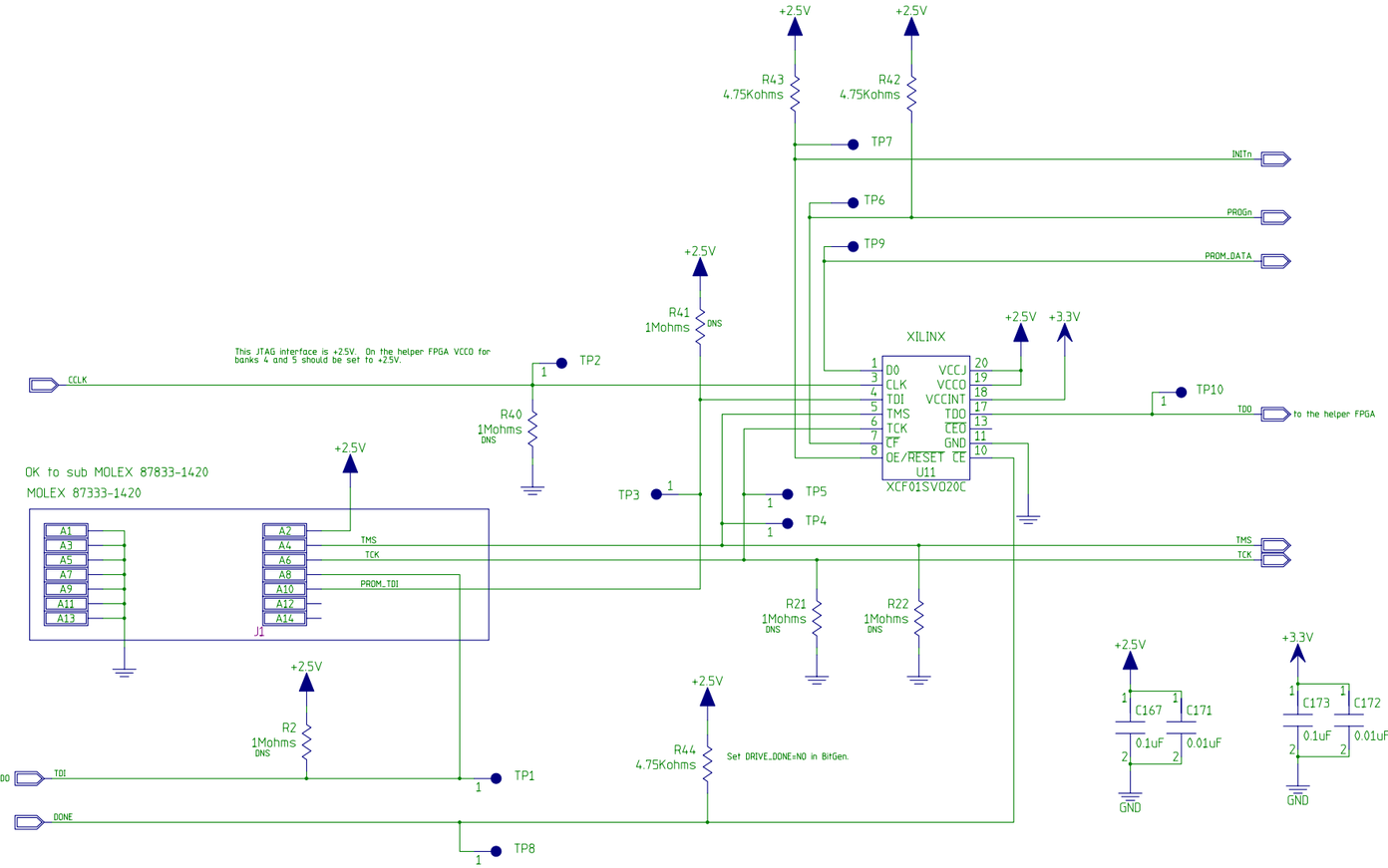
H:8ND; V:4LA

Front panel JTAG connector.
Chain order is:
1) PROM
2) helper FPGA
3) main FPGA

Use with Parallel Cable IV
or USB cable.



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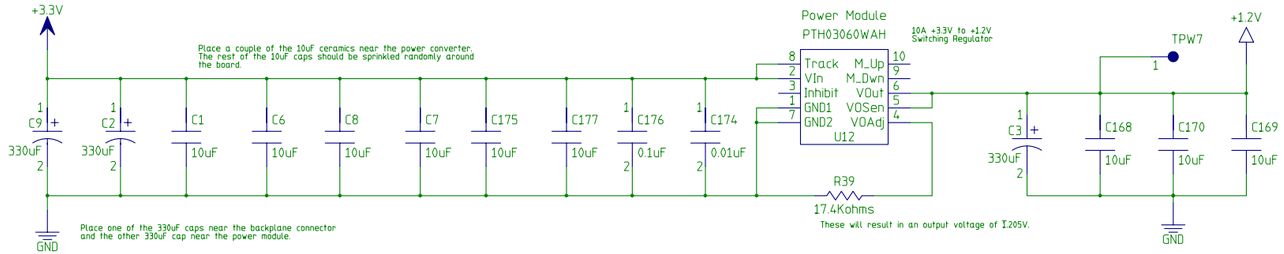
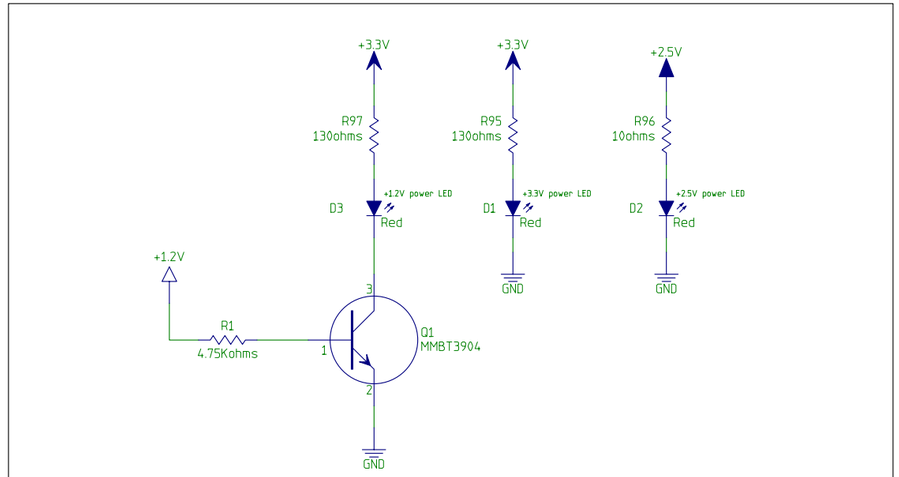
JTAG and PROM

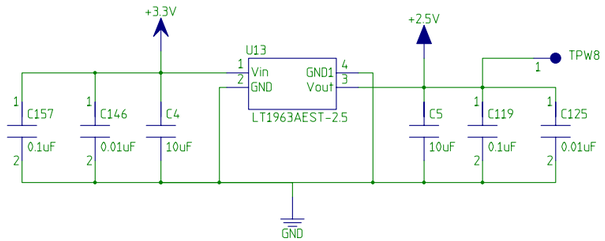
SIZE	DRAWING NUMBER	REV
D	0000-ED-173618 Schematic Page 01 of 01	.

H=8ND; V=4LA

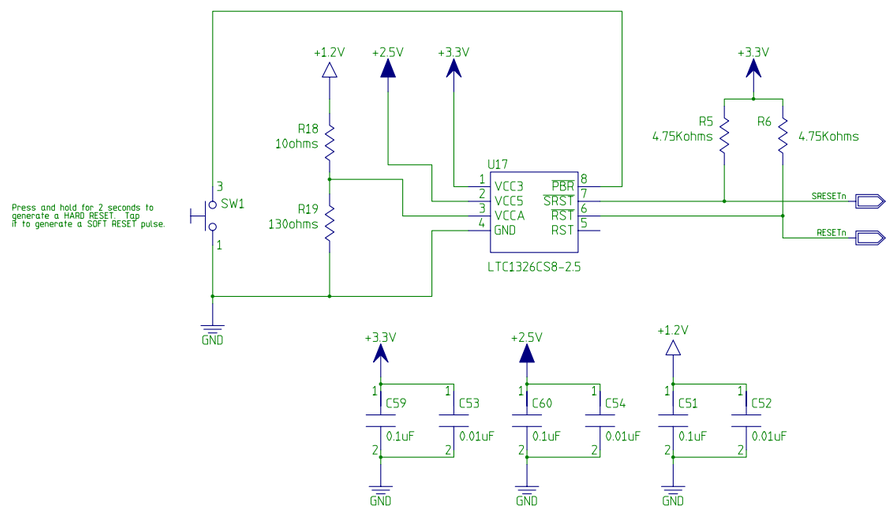




This linear regulator is used to supply
a reference voltage to the FPGAs.
Max output current is 1.5A. Heatsink the
tab into the ground plane.



Power on reset and "soft" reset
generator and voltage supervisor.



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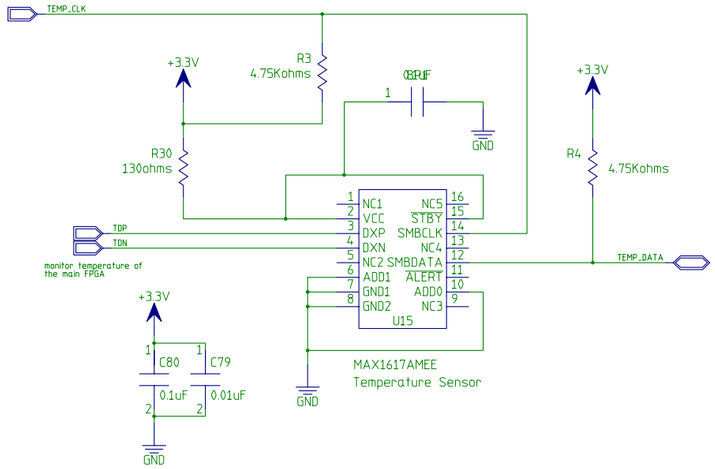
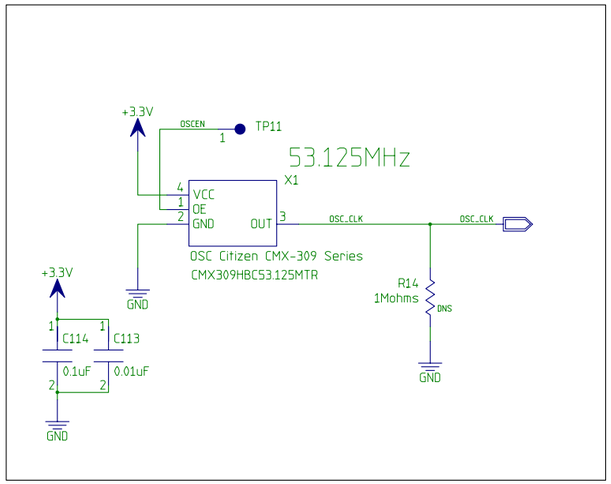
POWER

SIZE	DRAWING NUMBER	REV
D	0000-ED-173618 Schematic Page 01 of 01	.

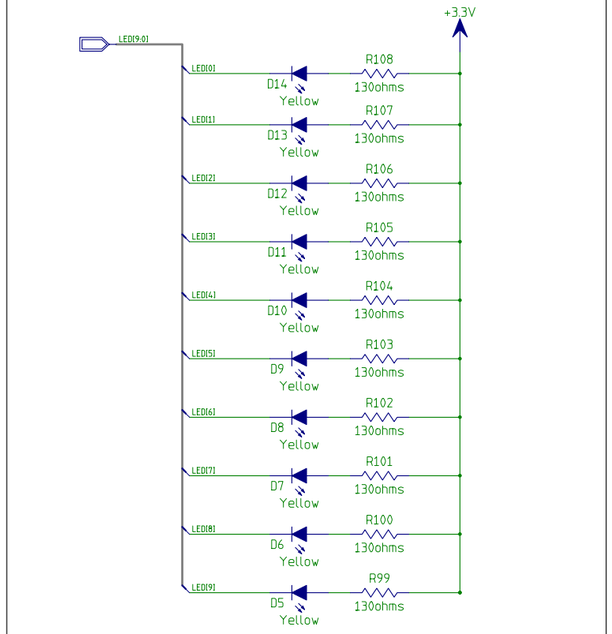
H=8ND; V=4LA

This sensor monitors the die temperature
of the main FPGA and the ambient
temperature of the board. FMAX = 400kHz.

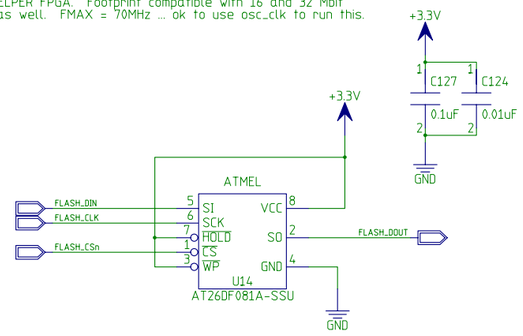




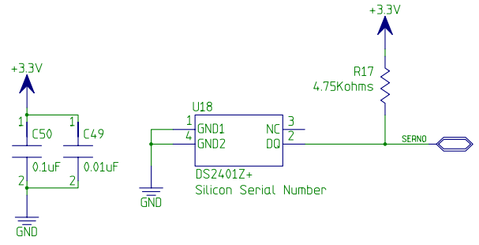
Ten general purpose LEDs go
on the front panel.



ATMEL 8Mbit serial FLASH memory may be used for storing
configuration data for the large FPGA. This memory is connected
to the HELPER FPGA. Footprint compatible with 16 and 32 Mbit
devices as well. FMAX = 70MHz ... ok to use osc_clk to run this.



Silicon Serial Number



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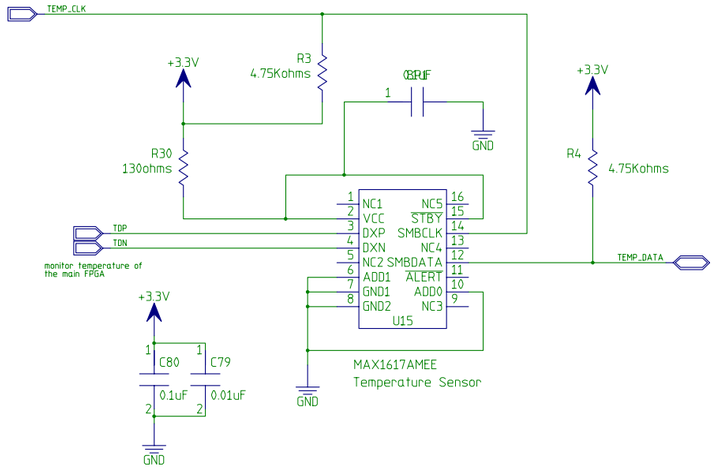
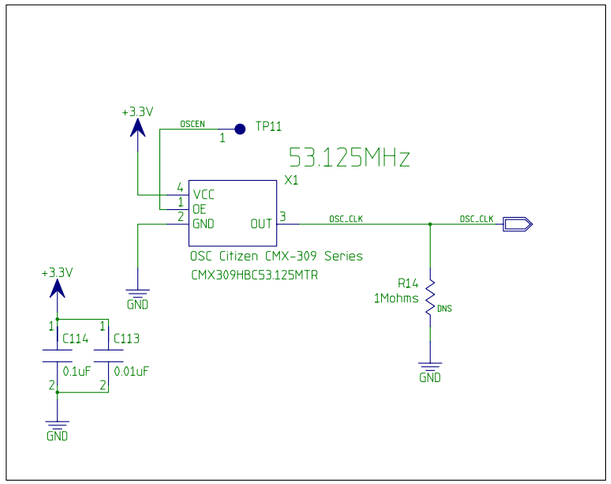
MISC STUFF

SIZE	DRAWING NUMBER	REV
D	0000-ED-173618 Schematic Page 01 of 01	.

H:8ND; V:4LA

This sensor monitors the die temperature
of the main FPGA and the ambient
temperature of the board. FMAX = 400kHz.





Ten general purpose LEDs go
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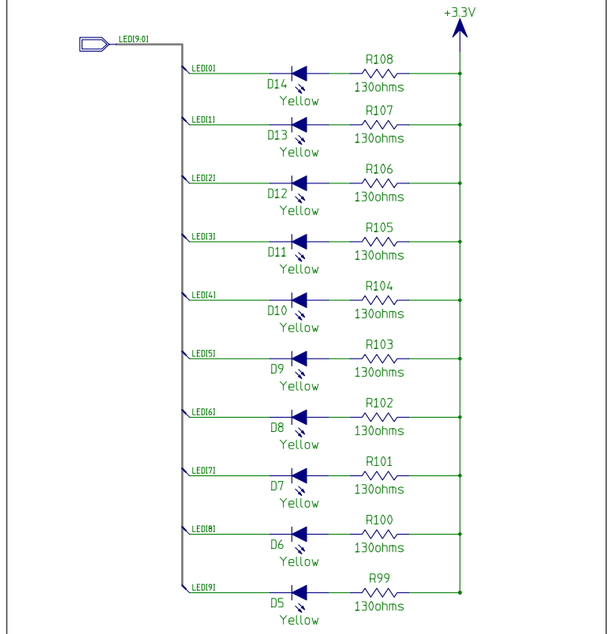

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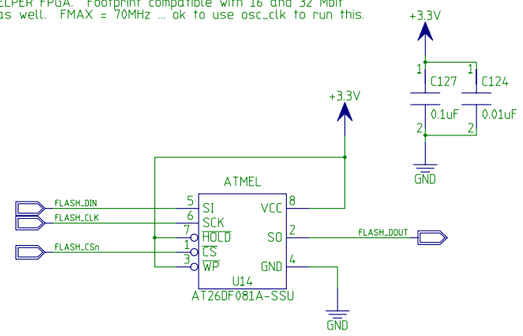

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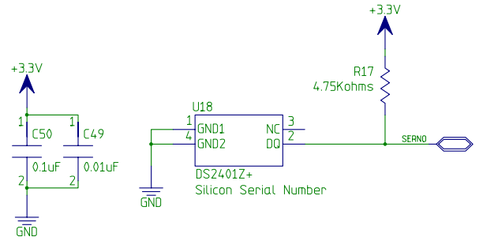

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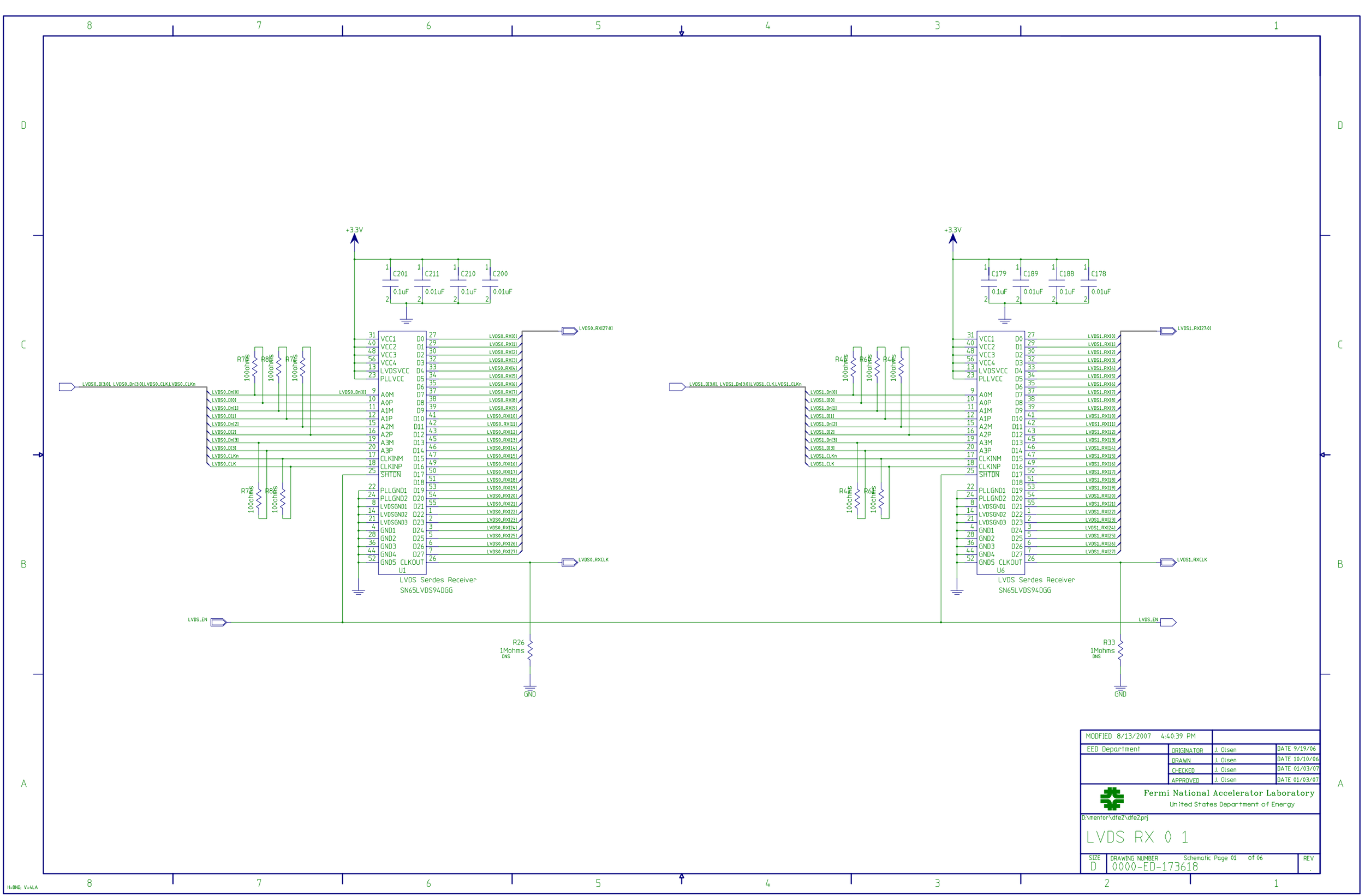
MISC STUFF

SIZE	DRAWING NUMBER	REV
D	0000-ED-173618 Schematic Page 01 of 01	.

H:8ND; V:4LA


+3.3V
C201 0.1uF
C211 0.01uF
C210 0.1uF
C200 0.01uF
LVDS0_DI[3:0], LVDS0_DIn[3:0],LVDS0_CLK,LVDS0_CLKn
LVDS0_DIn[0]
LVDS0_DI[0]
LVDS0_DIn[1]
LVDS0_DI[1]
LVDS0_DIn[2]
LVDS0_DI[2]
LVDS0_DIn[3]
LVDS0_DI[3]
LVDS0_CLKn
LVDS0_CLK
R7 100ohms
R8 100ohms
R7 100ohms
R7 100ohms
R8 100ohms
VCC1
VCC2
VCC3
VCC4
LVDSVCC
PLLVCC
A0M
A0P
A1M
A1P
A2M
A2P
A3M
A3P
CLKINM
CLKINP
SHTDN
PLLGND1
PLLGND2
LVDSGND1
LVDSGND2
LVDSGND3
GND1
GND2
GND3
GND4
GND5
CLKOUT
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
LVDS0_RX[27:0]
LVDS0_RX[0]
LVDS0_RX[1]
LVDS0_RX[2]
LVDS0_RX[3]
LVDS0_RX[4]
LVDS0_RX[5]
LVDS0_RX[6]
LVDS0_RX[7]
LVDS0_RX[8]
LVDS0_RX[9]
LVDS0_RX[10]
LVDS0_RX[11]
LVDS0_RX[12]
LVDS0_RX[13]
LVDS0_RX[14]
LVDS0_RX[15]
LVDS0_RX[16]
LVDS0_RX[17]
LVDS0_RX[18]
LVDS0_RX[19]
LVDS0_RX[20]
LVDS0_RX[21]
LVDS0_RX[22]
LVDS0_RX[23]
LVDS0_RX[24]
LVDS0_RX[25]
LVDS0_RX[26]
LVDS0_RX[27]
LVDS0_RXCLK
U1
LVDS Serdes Receiver
SN65LVDS94DGG
LVDS_EN
R26 1Mohms DNS
GND
+3.3V
C179 0.1uF
C189 0.01uF
C188 0.1uF
C178 0.01uF
LVDS1_DI[3:0], LVDS1_DIn[3:0],LVDS1_CLK,LVDS1_CLKn
LVDS1_DIn[0]
LVDS1_DI[0]
LVDS1_DIn[1]
LVDS1_DI[1]
LVDS1_DIn[2]
LVDS1_DI[2]
LVDS1_DIn[3]
LVDS1_DI[3]
LVDS1_CLKn
LVDS1_CLK
R4 100ohms
R6 100ohms
R4 100ohms
R4 100ohms
R6 100ohms
LVDS1_RX[27:0]
LVDS1_RX[0]
LVDS1_RX[1]
LVDS1_RX[2]
LVDS1_RX[3]
LVDS1_RX[4]
LVDS1_RX[5]
LVDS1_RX[6]
LVDS1_RX[7]
LVDS1_RX[8]
LVDS1_RX[9]
LVDS1_RX[10]
LVDS1_RX[11]
LVDS1_RX[12]
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LVDS1_RX[14]
LVDS1_RX[15]
LVDS1_RX[16]
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LVDS1_RX[23]
LVDS1_RX[24]
LVDS1_RX[25]
LVDS1_RX[26]
LVDS1_RX[27]
LVDS1_RXCLK
U6
LVDS Serdes Receiver
SN65LVDS94DGG
LVDS_EN
R33 1Mohms DNS
GND
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EED Department
ORIGINATOR J. Olsen DATE 9/19/06
DRAWN J. Olsen DATE 10/10/06
CHECKED J. Olsen DATE 01/03/07
APPROVED J. Olsen DATE 01/03/07
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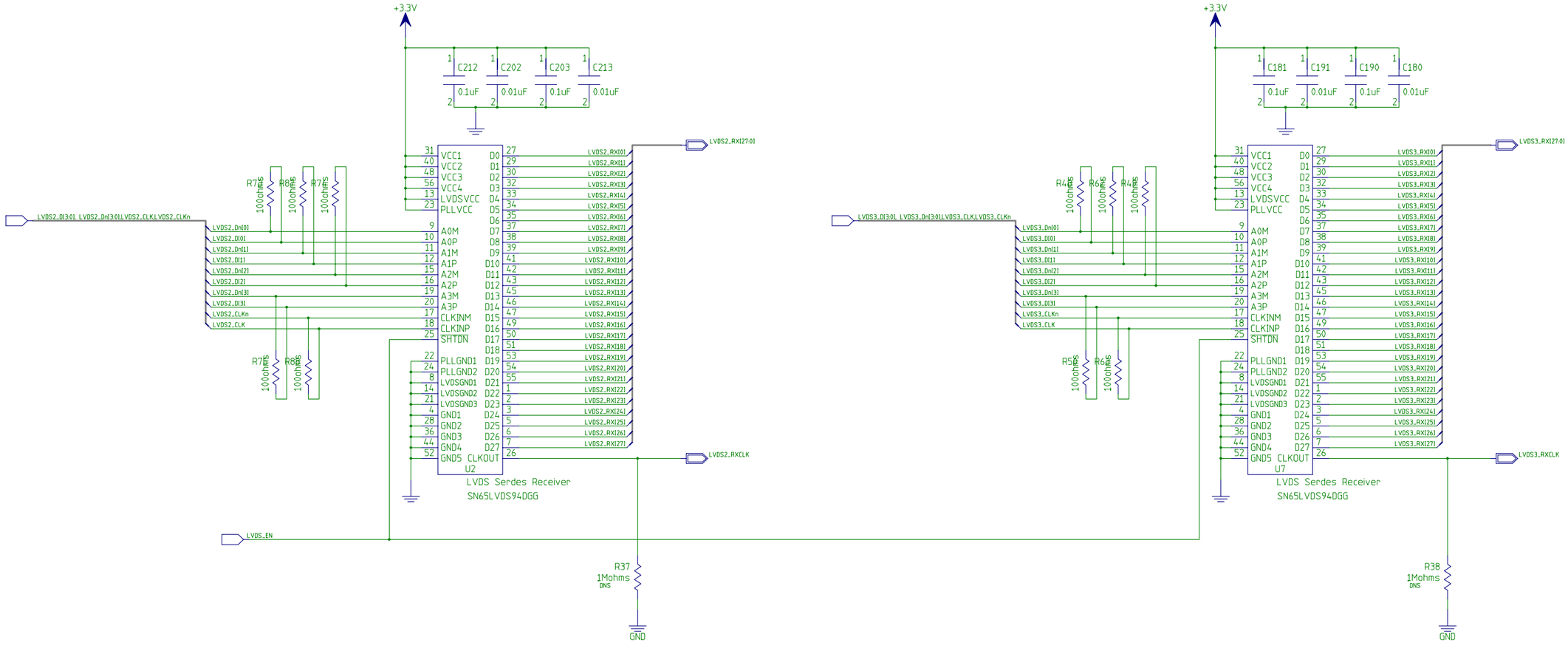
LVDS RX 0 1
SIZE D
DRAWING NUMBER 0000-ED-173618
Schematic Page 01 of 06
REV .
H=8ND; V=4LA



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LVDS RX 2 3

SIZE	DRAWING NUMBER		REV
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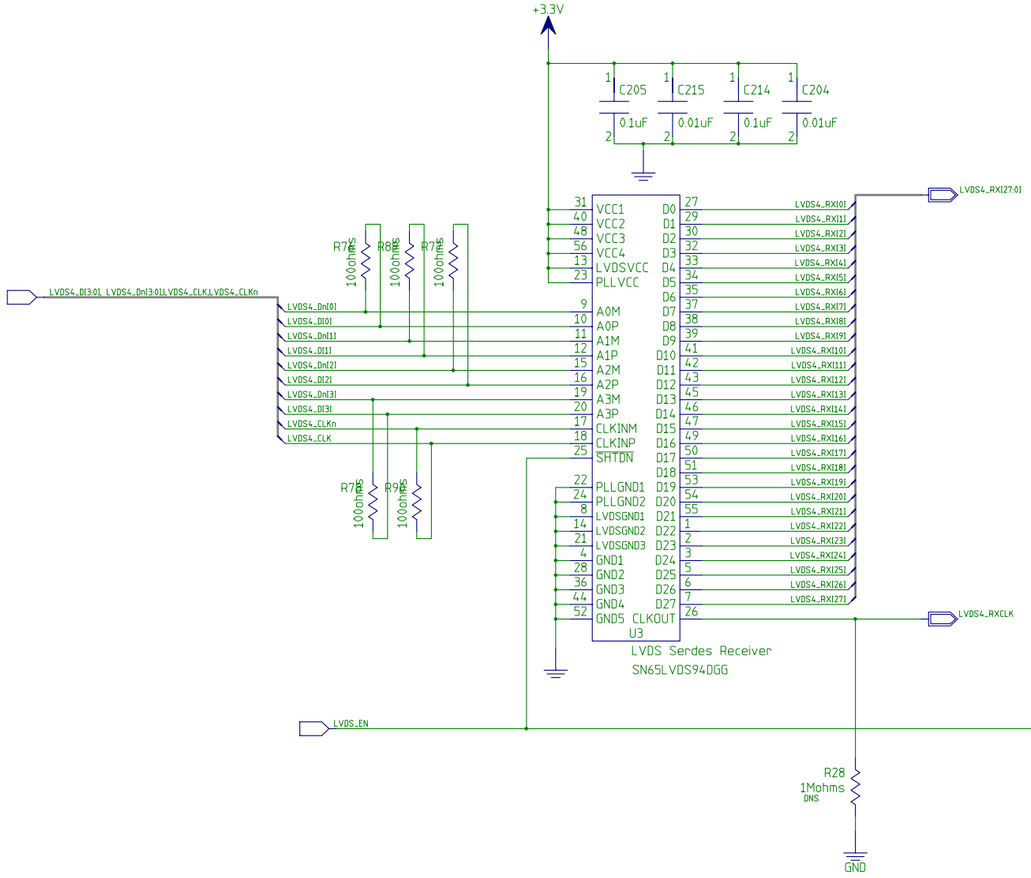

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LVDS RX 4 5

SIZE	DRAWING NUMBER	REV
D	0000-ED-173618 Schematic Page 03 of 06	.

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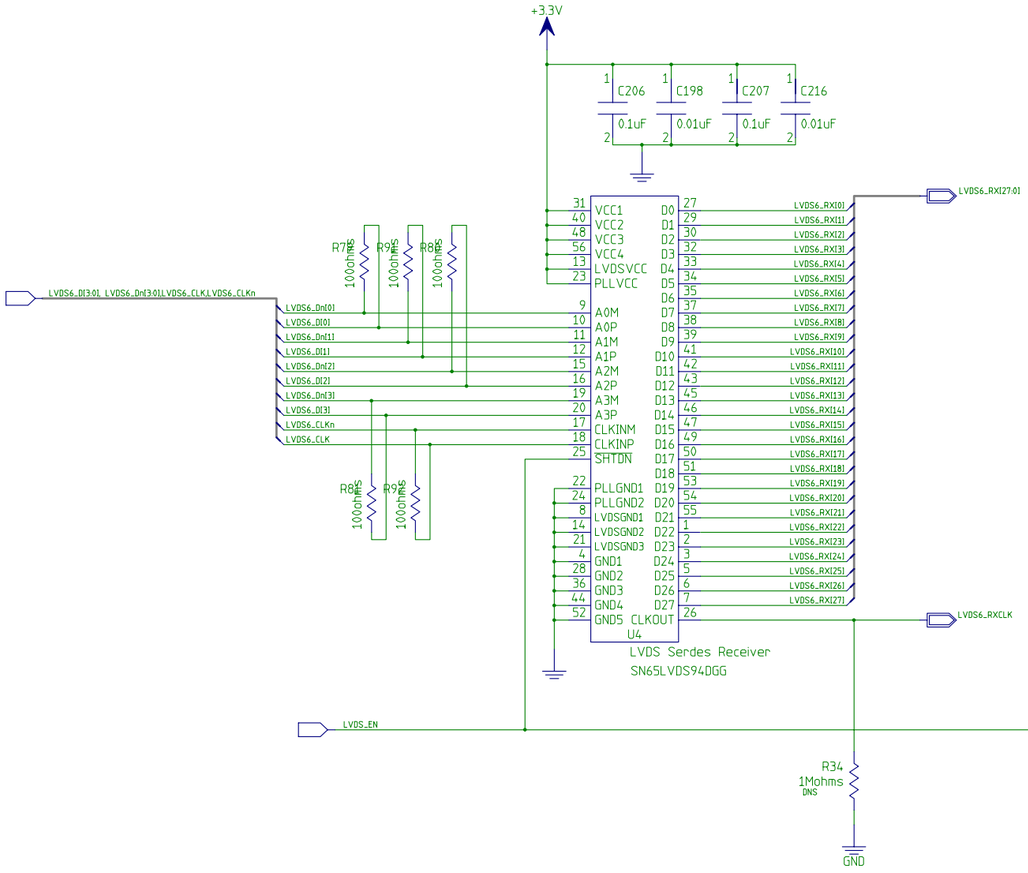

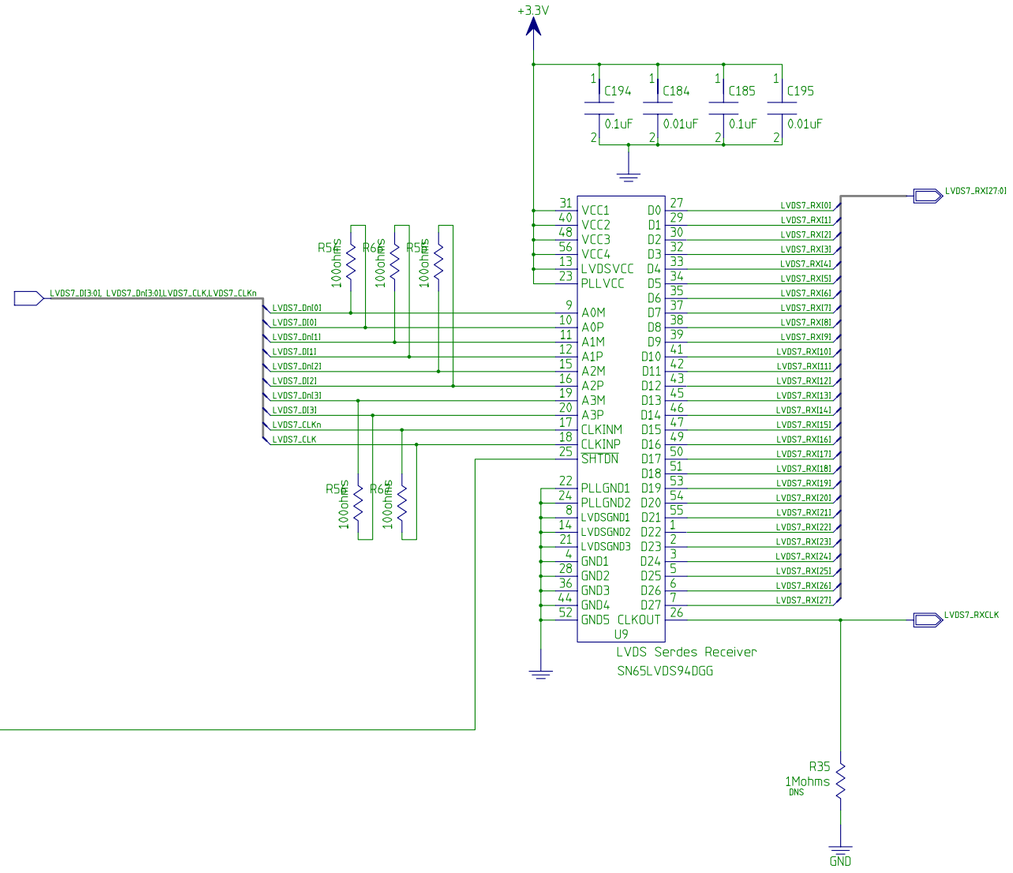

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LVDS RX 6 7

SIZE	DRAWING NUMBER		REV
D	0000-ED-173618	Schematic Page 04 of 06	.

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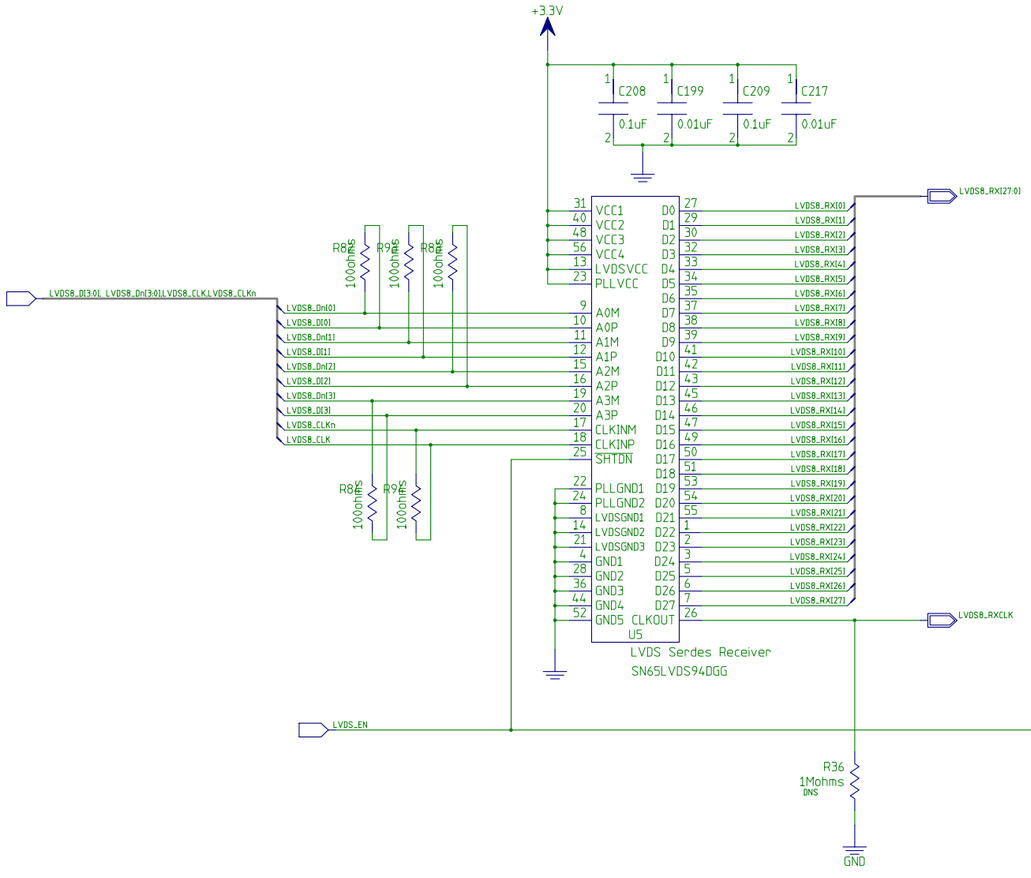

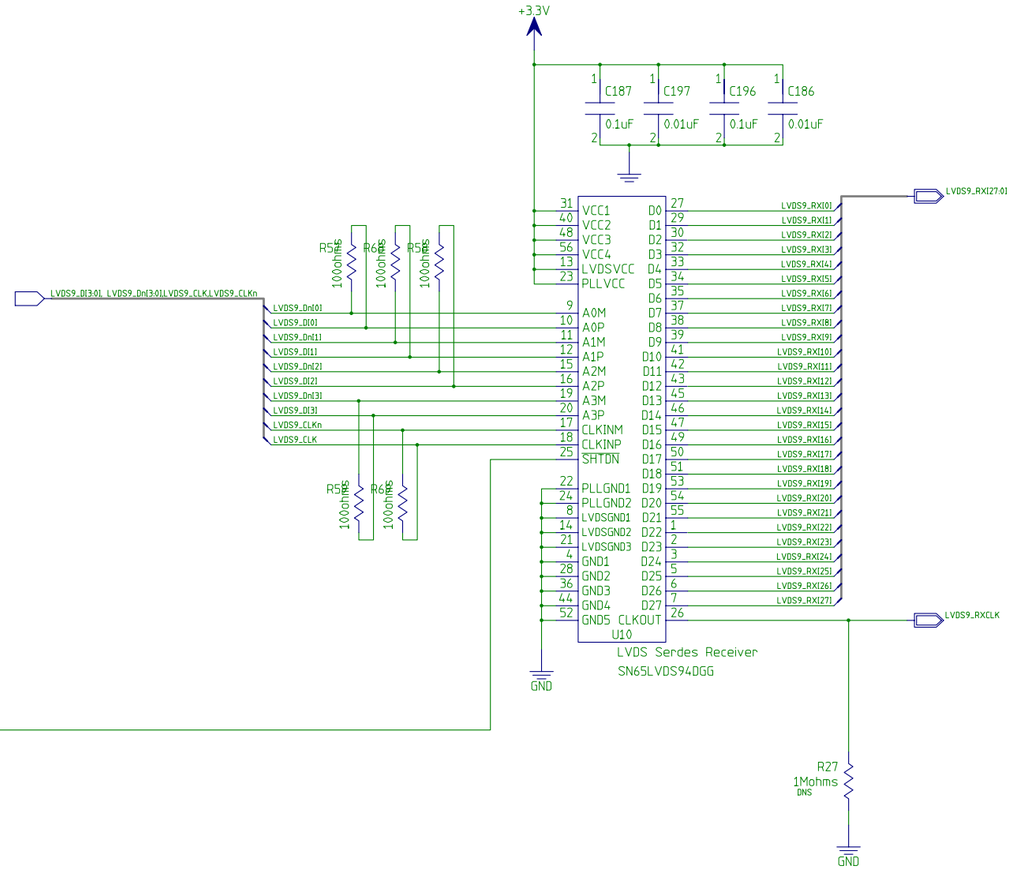

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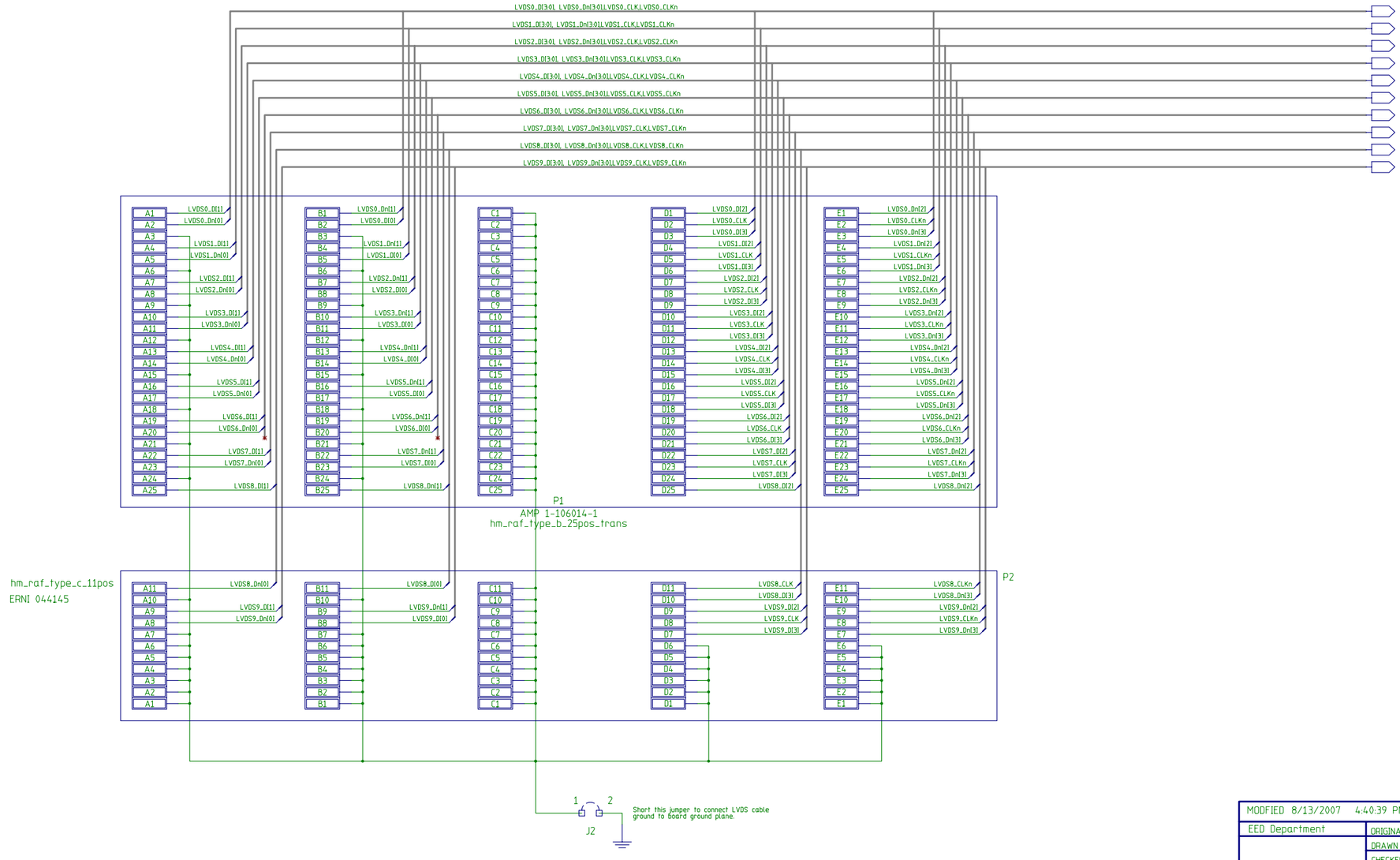
LVDS RX 8 9

SIZE	DRAWING NUMBER		REV
D	0000-ED-173618	Schematic Page 05 of 06	.

H:8ND; V:4LA



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LVDS / FRONT CONNECTOR

SIZE	DRAWING NUMBER	REV
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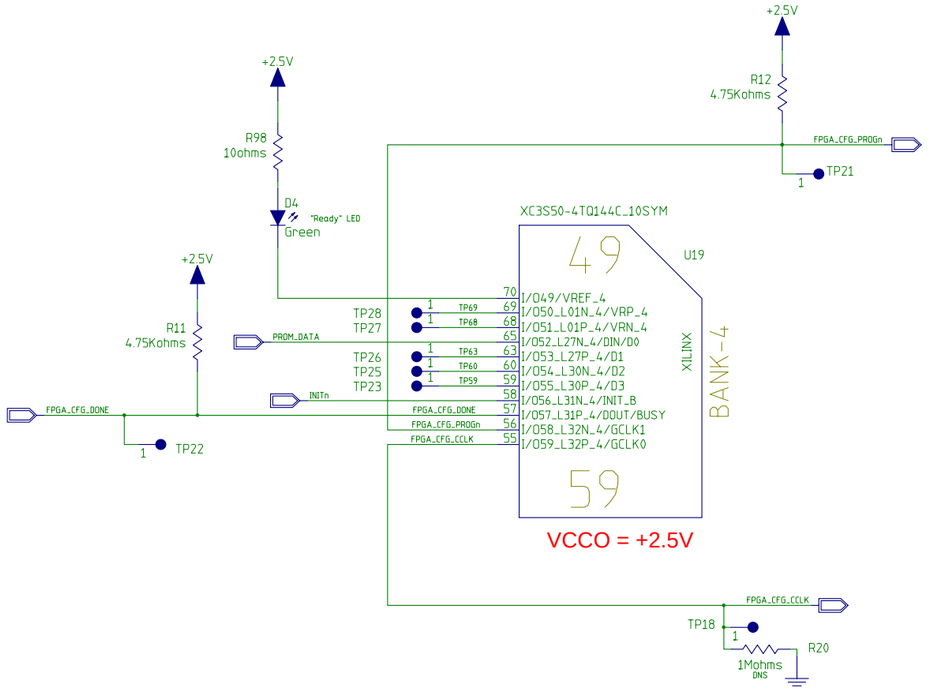

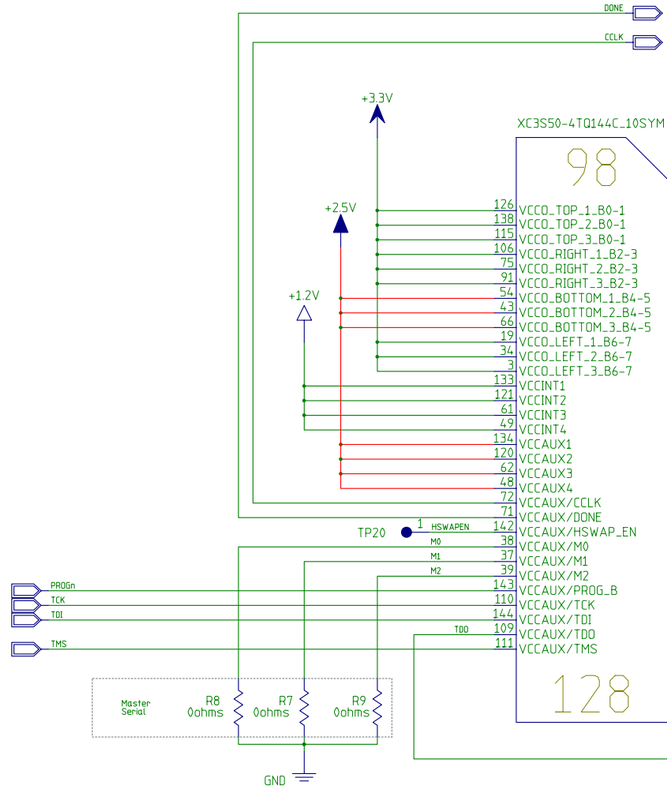

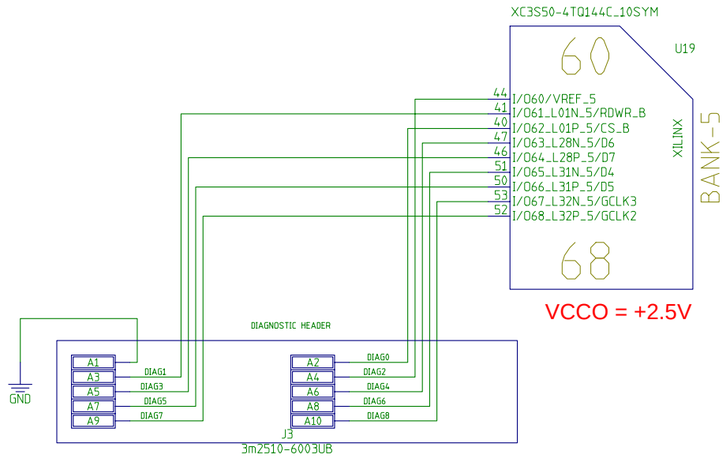

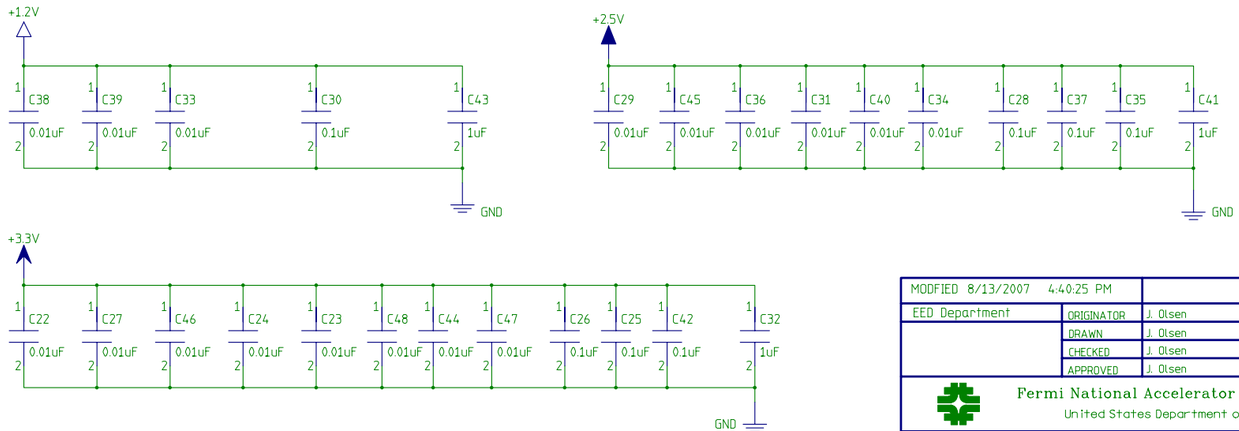

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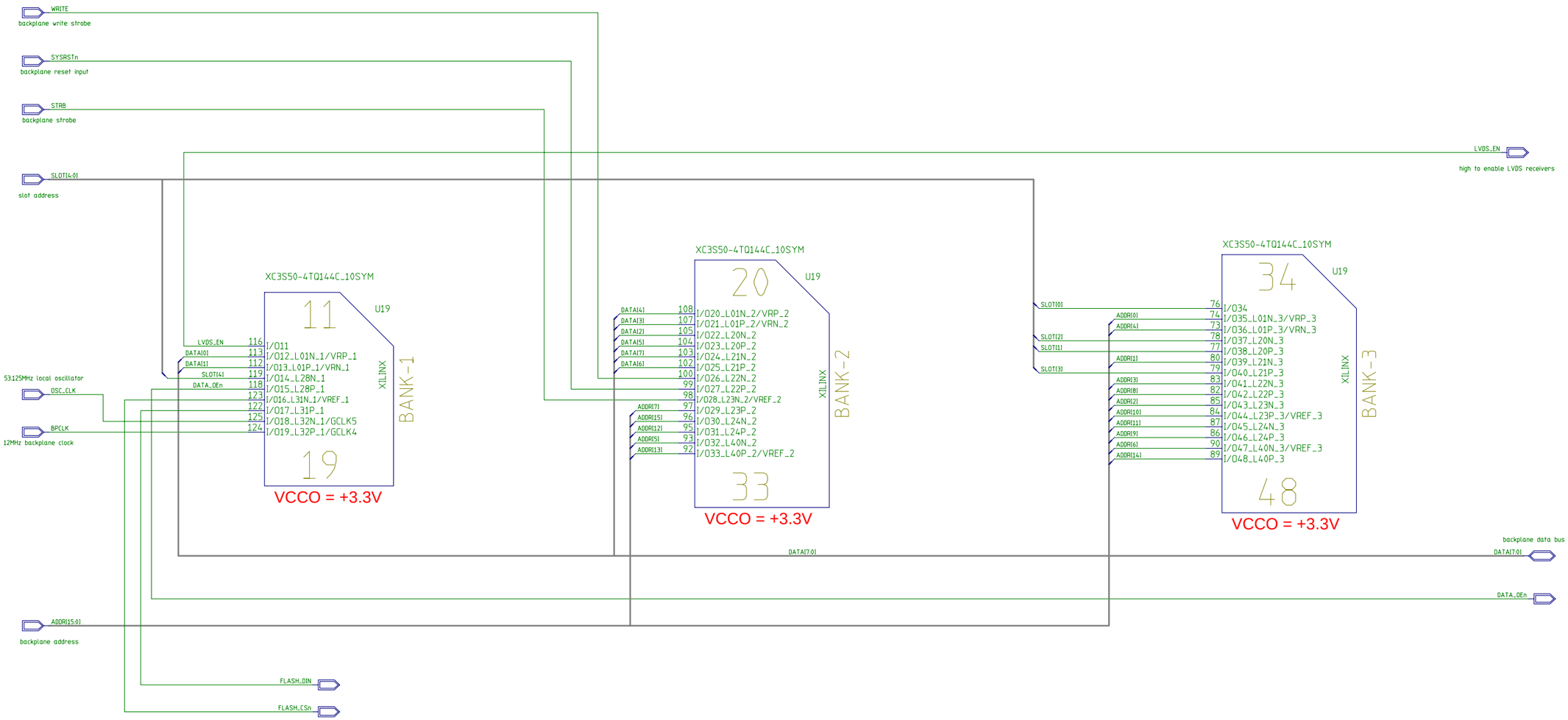
HELPER / CONFIG

SIZE	DRAWING NUMBER		REV
D	0000-ED-173618	Schematic Page 01 of 03	.

H:8ND; V:4LA



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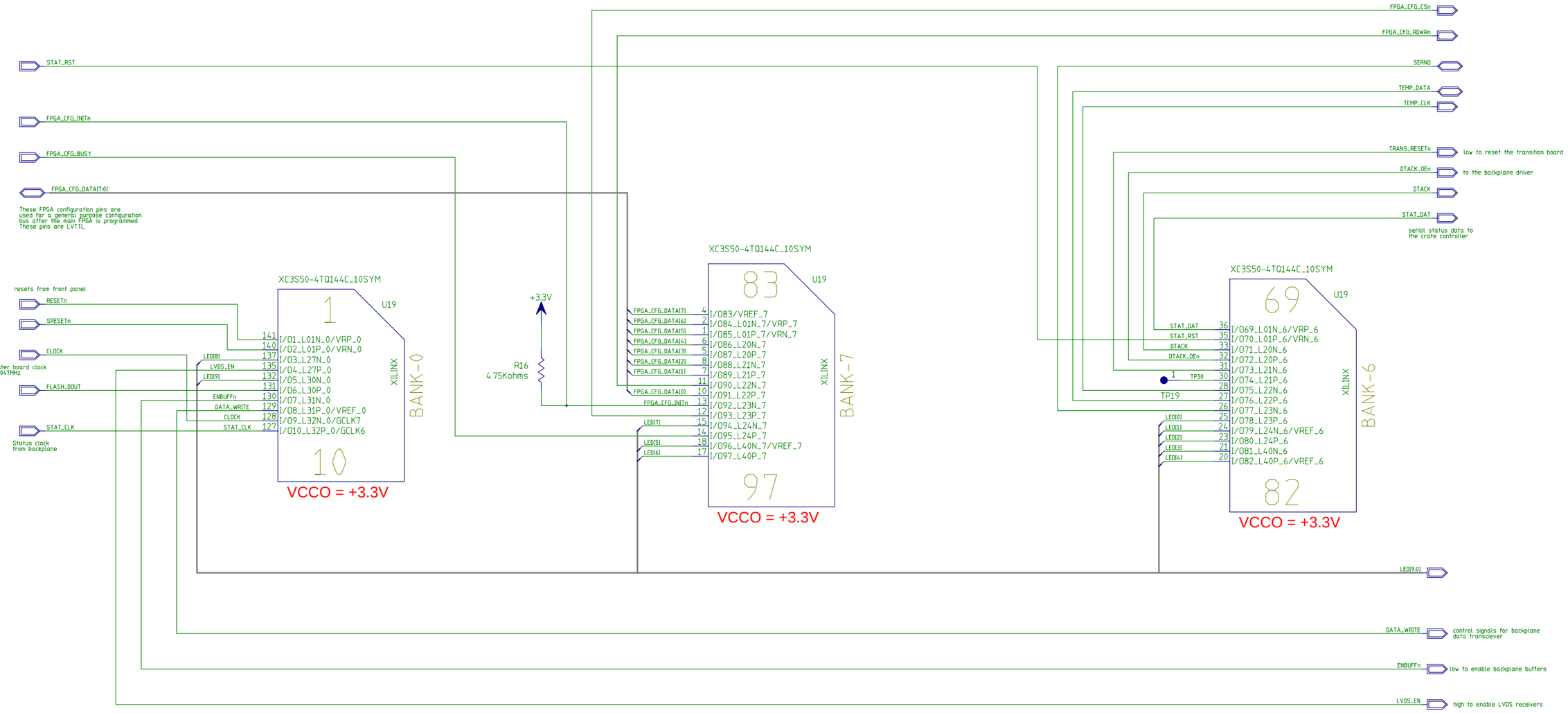
HELPER / BANKS 1 2 3

SIZE	DRAWING NUMBER		REV
D	0000-ED-173618	Schematic Page 02 of 03	.

H=8ND; V=4LA



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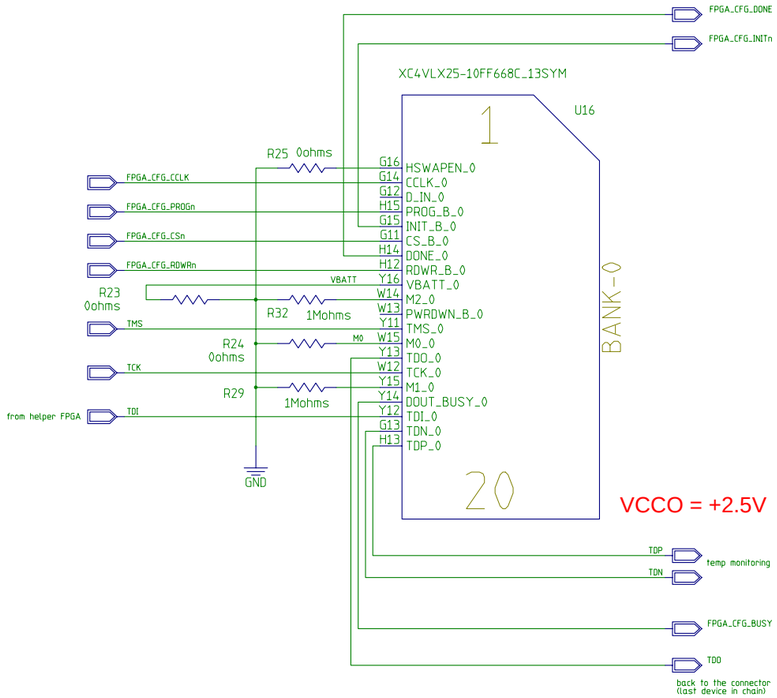
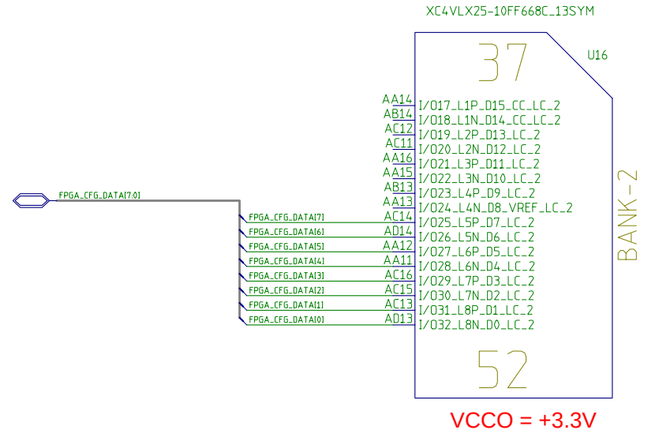
HELPER / BANKS 0 7 6

SIZE	DRAWING NUMBER		REV
D	0000-ED-173618	Schematic Page 03 of 03	.

H:8ND; V:4LA





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	CHECKED	J. Olsen	DATE 01/03/07
	APPROVED	J. Olsen	DATE 01/03/07

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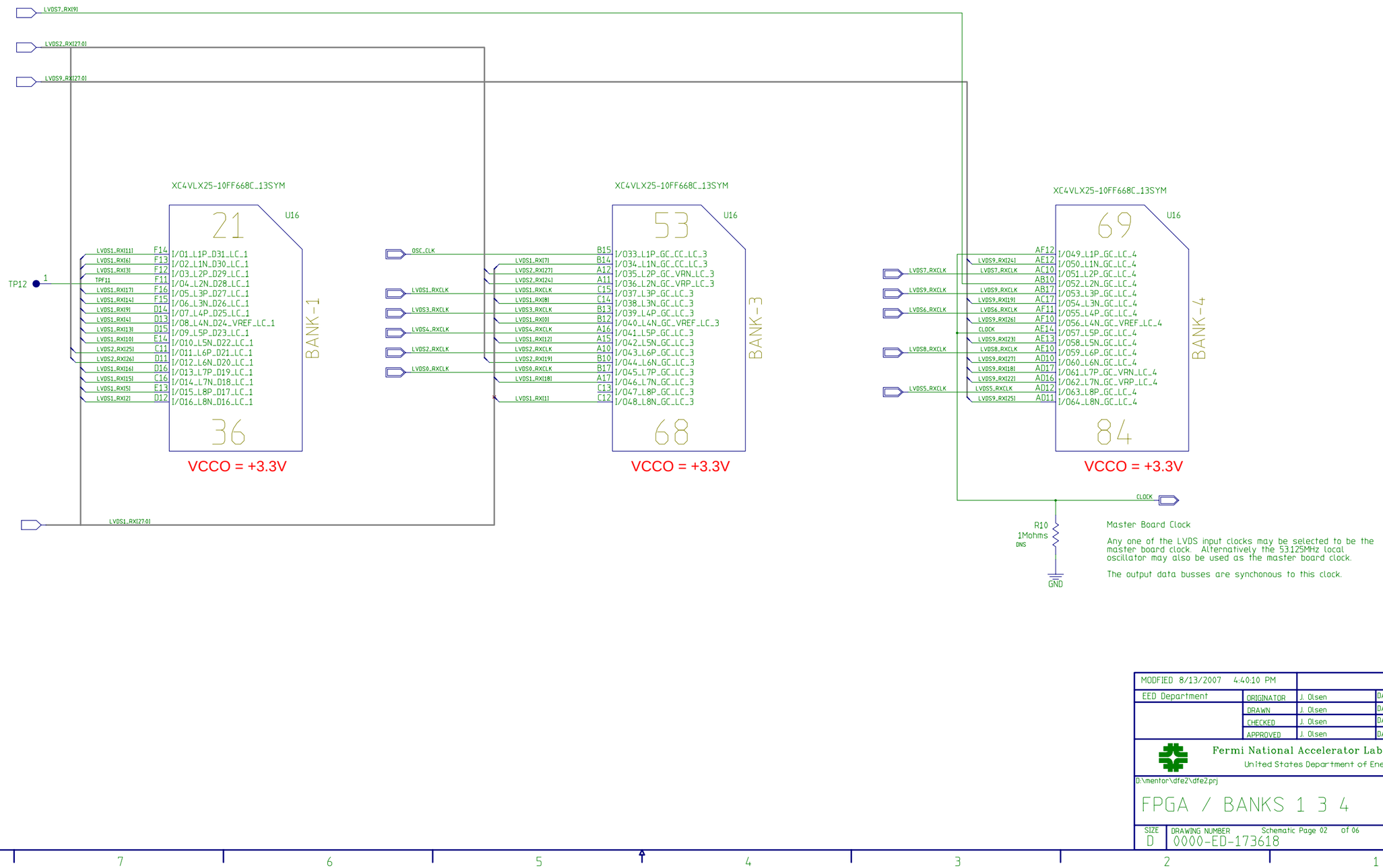

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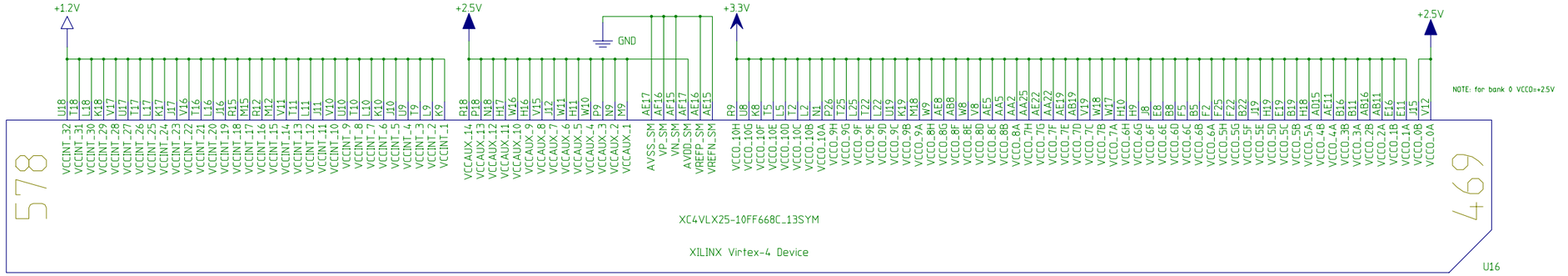

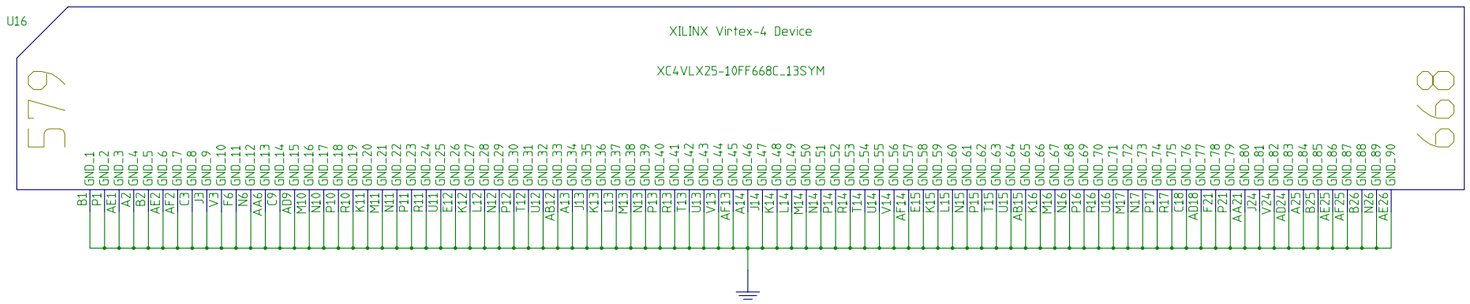

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FPGA / POWER and GROUND

SIZE	DRAWING NUMBER		REV
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H:8ND; V:4LA

RESETn

SRESETn

TOP_MUON[27:0]

LVDS9_RX[27:0]

LVDS1_RX[27:0]

LVDS0_RX[27:0]

TOP_L1L2[27:0]

TOP_L1L2[27:0]

TOP_MUON[27:0]

to bank 4

to banks 1 and 3

XC4VLX25-10FF668C_13SYM

U16

85

LVDS1_RX[19]	C17	I/O65_L1P_5
LVDS1_RX[20]	D17	I/O66_L1N_5
LVDS0_RX[9]	C20	I/O67_L2P_5
LVDS0_RX[8]	B20	I/O68_L2N_5
LVDS0_RX[1]	B18	I/O69_L3P_5
LVDS0_RX[0]	A18	I/O70_L3N_5
LVDS0_RX[10]	D20	I/O71_L4P_5
LVDS0_RX[4]	D19	I/O72_L4N_VREF_5
LVDS1_RX[21]	E17	I/O73_L5P_5
LVDS1_RX[22]	F17	I/O74_L5N_5
LVDS0_RX[15]	C21	I/O75_L6P_5
LVDS0_RX[14]	B21	I/O76_L6N_5
LVDS0_RX[3]	C19	I/O77_L7P_5
LVDS1_RX[24]	D18	I/O78_L7N_5
LVDS0_RX[25]	A24	I/O79_L8P_CC_LC_5
LVDS0_RX[21]	A23	I/O80_L8N_CC_LC_5
LVDS0_RX[6]	G19	I/O81_L17P_5
LVDS0_RX[5]	F19	I/O82_L17N_5
TOP_MUON[21]	E23	I/O83_L18P_5
TOP_MUON[20]	E22	I/O84_L18N_5
LVDS0_RX[12]	F20	I/O85_L19P_5
LVDS0_RX[11]	E20	I/O86_L19N_5
	C26	I/O87_L20P_5
	C25	I/O88_L20N_VREF_5
LVDS0_RX[24]	D23	I/O89_L21P_5
LVDS0_RX[23]	C23	I/O90_L21N_5
	H20	I/O91_L22P_5
	G20	I/O92_L22N_5
TOP_MUON[12]	G22	I/O93_L23P_VRN_5
	G21	I/O94_L23N_VRP_5
TOP_MUON[18]	F24	I/O95_L24P_CC_LC_5
TOP_MUON[17]	F23	I/O96_L24N_CC_LC_5
LVDS1_RX[27]	G18	I/O97_L9P_CC_LC_5
LVDS1_RX[23]	G17	I/O98_L9N_CC_LC_5
LVDS0_RX[26]	B24	I/O99_L10P_5
LVDS0_RX[22]	B23	I/O100_L10N_5
LVDS1_RX[26]	F18	I/O101_L11P_5
LVDS1_RX[25]	E18	I/O102_L11N_5
LVDS0_RX[17]	E21	I/O103_L12P_5
LVDS0_RX[16]	D21	I/O104_L12N_VREF_5
LVDS0_RX[7]	A20	I/O105_L13P_5
LVDS0_RX[2]	A19	I/O106_L13N_5
LVDS0_RX[20]	D22	I/O107_L14P_5
LVDS0_RX[19]	C22	I/O108_L14N_5
LVDS0_RX[18]	A22	I/O109_L15P_5
LVDS0_RX[13]	A21	I/O110_L15N_5
TOP_MUON[25]	D24	I/O111_L16P_5
LVDS0_RX[27]	C24	I/O112_L16N_5
TOP_MUON[27]	D26	I/O113_L25P_CC_LC_5
TOP_MUON[26]	D25	I/O114_L25N_CC_LC_5
TOP_MUON[7]	H22	I/O115_L26P_5
	H21	I/O116_L26N_5
TOP_MUON[23]	E25	I/O117_L27P_5
TOP_MUON[22]	E24	I/O118_L27N_5
TOP_MUON[14]	G24	I/O119_L28P_5
TOP_MUON[13]	G23	I/O120_L28N_VREF_5
TOP_MUON[19]	F26	I/O121_L29P_5
TOP_MUON[24]	E26	I/O122_L29N_5
TOP_MUON[9]	H24	I/O123_L30P_5
TOP_MUON[8]	H23	I/O124_L30N_5
TOP_MUON[16]	G26	I/O125_L31P_5
TOP_MUON[15]	G25	I/O126_L31N_5
TOP_MUON[11]	H26	I/O127_L32P_5
TOP_MUON[10]	H25	I/O128_L32N_5

148

BANK-5

VCCO = +3.3V

XC4VLX25-10FF668C_13SYM

U16

341

TOP_L1L2[11]	N21	I/O321_L17P_9
TOP_L1L2[10]	N20	I/O322_L17N_9
TOP_L1L2[9]	P25	I/O323_L18P_9
TOP_L1L2[8]	P24	I/O324_L18N_9
TOP_L1L2[7]	P23	I/O325_L19P_9
TOP_L1L2[6]	P22	I/O326_L19N_9
BOT_MUON[27]	R26	I/O327_L20P_9
TOP_L1L2[5]	R25	I/O328_L20N_VREF_9
	P20	I/O329_L21P_9
	P19	I/O330_L21N_9
TOP_L1L2[4]	R24	I/O331_L22P_9
TOP_L1L2[3]	R23	I/O332_L22N_9
TOP_L1L2[2]	R22	I/O333_L23P_VRN_9
TOP_L1L2[1]	R21	I/O334_L23N_VRP_9
BOT_MUON[25]	T24	I/O335_L24P_CC_LC_9
BOT_MUON[24]	T23	I/O336_L24N_CC_LC_9
RESETn	J21	I/O337_L1P_9
	J20	I/O338_L1N_9
TOP_MUON[4]	J23	I/O339_L2P_9
TOP_MUON[3]	J22	I/O340_L2N_9
TOP_MUON[0]	K22	I/O341_L3P_9
SRESETn	K21	I/O342_L3N_9
TOP_MUON[6]	J26	I/O343_L4P_9
TOP_MUON[5]	J25	I/O344_L4N_VREF_9
	L19	I/O345_L5P_9
	K20	I/O346_L5N_9
TOP_L1L2[22]	L21	I/O347_L6P_9
	L20	I/O348_L6N_9
TOP_MUON[2]	K24	I/O349_L7P_9
TOP_MUON[1]	K23	I/O350_L7N_9
TOP_L1L2[27]	K26	I/O351_L8P_CC_LC_9
TOP_L1L2[26]	K25	I/O352_L8N_CC_LC_9
	M19	I/O353_L9P_CC_LC_9
	N19	I/O354_L9N_CC_LC_9
TOP_L1L2[24]	L24	I/O355_L10P_9
TOP_L1L2[23]	L23	I/O356_L10N_9
TOP_L1L2[20]	M25	I/O357_L11P_9
TOP_L1L2[19]	M24	I/O358_L11N_9
TOP_L1L2[25]	L26	I/O359_L12P_9
TOP_L1L2[21]	M26	I/O360_L12N_VREF_9
TOP_L1L2[16]	M21	I/O361_L13P_9
	M20	I/O362_L13N_9
TOP_L1L2[18]	M23	I/O363_L14P_9
TOP_L1L2[17]	M22	I/O364_L14N_9
TOP_L1L2[15]	N25	I/O365_L15P_9
TOP_L1L2[14]	N24	I/O366_L15N_9
TOP_L1L2[13]	N23	I/O367_L16P_9
TOP_L1L2[12]	N22	I/O368_L16N_9
TOP_L1L2[10]	R20	I/O369_L25P_CC_LC_9
	R19	I/O370_L25N_CC_LC_9
BOT_MUON[26]	T26	I/O371_L26P_9
BOT_MUON[22]	U26	I/O372_L26N_9
BOT_MUON[19]	U23	I/O373_L27P_9
BOT_MUON[14]	V23	I/O374_L27N_9
BOT_MUON[21]	U25	I/O375_L28P_9
BOT_MUON[20]	U24	I/O376_L28N_VREF_9
BOT_MUON[18]	U22	I/O377_L29P_9
BOT_MUON[17]	U21	I/O378_L29N_9
BOT_MUON[23]	T21	I/O379_L30P_9
TPT20	T20	I/O380_L30N_9
TPU20	U20	I/O381_L31P_9
TPT19	T19	I/O382_L31N_9
BOT_MUON[16]	V26	I/O383_L32P_9
BOT_MUON[15]	V25	I/O384_L32N_9

TP16 TP15 TP13

404

BANK-9

VCCO = +3.3V

BOT_MUON[27:0]

XC4VLX25-10FF668C_13SYM

U16

213

LVDS9_RX[7]	AD19	I/O193_L25P_CC_SM7_LC_7
LVDS9_RX[8]	AC19	I/O194_L25N_CC_SM7_LC_7
LVDS9_RX[9]	AA19	I/O195_L26P_SM6_7
LVDS9_RX[5]	AA20	I/O196_L26N_SM6_7
LVDS9_RX[21]	Y17	I/O197_L27P_SM5_7
LVDS9_RX[20]	AA17	I/O198_L27N_SM5_7
LVDS9_RX[4]	AB20	I/O199_L28P_7
LVDS9_RX[3]	AC20	I/O200_L28N_VREF_7
LVDS9_RX[14]	AC18	I/O201_L29P_SM4_7
LVDS9_RX[15]	AB18	I/O202_L29N_SM4_7
BOT_L1L2[20]	AF21	I/O203_L30P_SM3_7
BOT_L1L2[21]	AF22	I/O204_L30N_SM3_7
LVDS9_RX[12]	AF18	I/O205_L31P_SM2_7
LVDS9_RX[13]	AE18	I/O206_L31N_SM2_7
BOT_L1L2[25]	AE21	I/O207_L32P_SM1_7
BOT_L1L2[8]	AD21	I/O208_L32N_SM1_7
LVDS9_RX[6]	AF19	I/O209_L17P_7
LVDS9_RX[0]	AF20	I/O210_L17N_7
LVDS9_RX[10]	Y19	I/O211_L18P_7
LVDS9_RX[11]	W19	I/O212_L18N_7
BOT_L1L2[3]	AF23	I/O213_L19P_7
BOT_L1L2[6]	AE23	I/O214_L19N_7
TPY20	Y20	I/O215_L20P_7
BOT_L1L2[26]	Y21	I/O216_L20N_VREF_7
LVDS9_RX[16]	AA16	I/O217_L21P_7
LVDS9_RX[17]	Y18	I/O218_L21N_7
BOT_L1L2[4]	AF24	I/O219_L22P_7
BOT_L1L2[7]	AE24	I/O220_L22N_7
LVDS9_RX[1]	AE20	I/O221_L23P_VRN_7
LVDS9_RX[2]	AD20	I/O222_L23N_VRP_7
BOT_L1L2[2]	AC21	I/O223_L24P_CC_LC_7
TPAB21	AB21	I/O224_L24N_CC_LC_7
BOT_MUON[12]	V21	I/O225_L1P_7
BOT_MUON[13]	V22	I/O226_L1N_7
BOT_MUON[9]	W25	I/O227_L2P_7
BOT_MUON[10]	W26	I/O228_L2N_7
BOT_MUON[5]	W21	I/O229_L3P_7
BOT_MUON[6]	W22	I/O230_L3N_7
BOT_MUON[7]	W23	I/O231_L4P_7
BOT_MUON[8]	W24	I/O232_L4N_VREF_7
BOT_MUON[4]	W20	I/O233_L5P_7
BOT_MUON[11]	V20	I/O234_L5N_7
BOT_MUON[2]	Y25	I/O235_L6P_7
BOT_MUON[3]	Y26	I/O236_L6N_7
BOT_L1L2[20]	AB24	I/O237_L7P_7
BOT_L1L2[21]	AB25	I/O238_L7N_7
BOT_L1L2[24]	AA24	I/O239_L8P_CC_LC_7
BOT_MUON[1]	Y24	I/O240_L8N_CC_LC_7
BOT_L1L2[16]	AC25	I/O241_L9P_CC_LC_7
BOT_L1L2[17]	AC26	I/O242_L9N_CC_LC_7
BOT_L1L2[22]	AB26	I/O243_L10P_7
BOT_L1L2[25]	AA26	I/O244_L10N_7
BOT_L1L2[11]	AD25	I/O245_L11P_7
BOT_L1L2[12]	AD26	I/O246_L11N_7
BOT_L1L2[27]	Y22	I/O247_L12P_7
BOT_MUON[0]	Y23	I/O248_L12N_VREF_7
BOT_L1L2[13]	AC22	I/O249_L13P_7
BOT_L1L2[18]	AB22	I/O250_L13N_7
BOT_L1L2[19]	AB23	I/O251_L14P_7
BOT_L1L2[23]	AA23	I/O252_L14N_7
BOT_L1L2[9]	AD22	I/O253_L15P_7
BOT_L1L2[10]	AD23	I/O254_L15N_7
BOT_L1L2[14]	AC23	I/O255_L16P_7
BOT_L1L2[15]	AC24	I/O256_L16N_7

TP14 TP17

276

BANK-7

VCCO = +3.3V

BOT_L1L2[27:0]

BOT_MUON[27:0]

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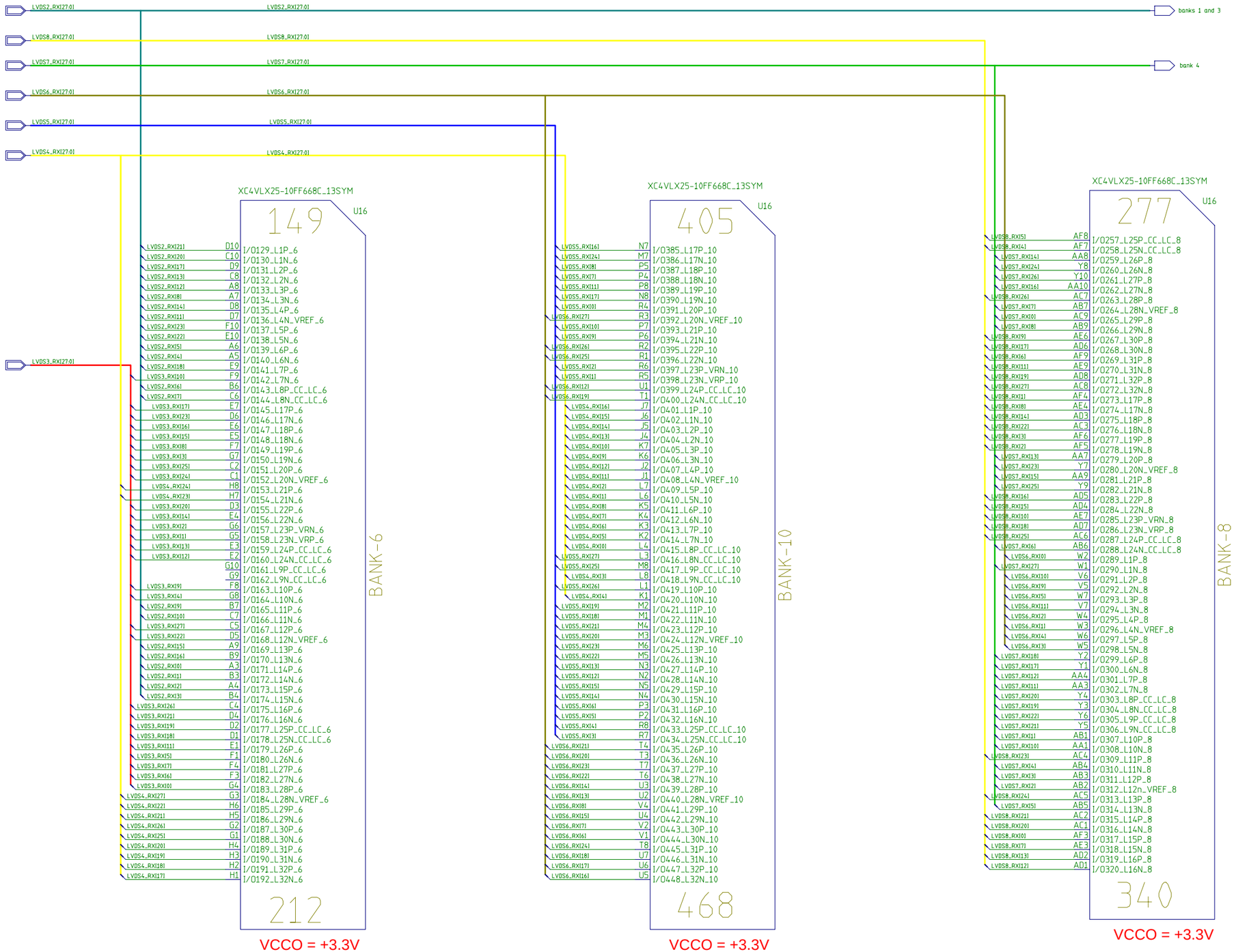

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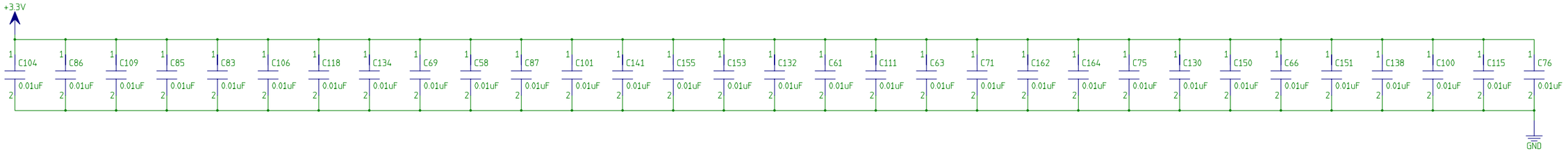

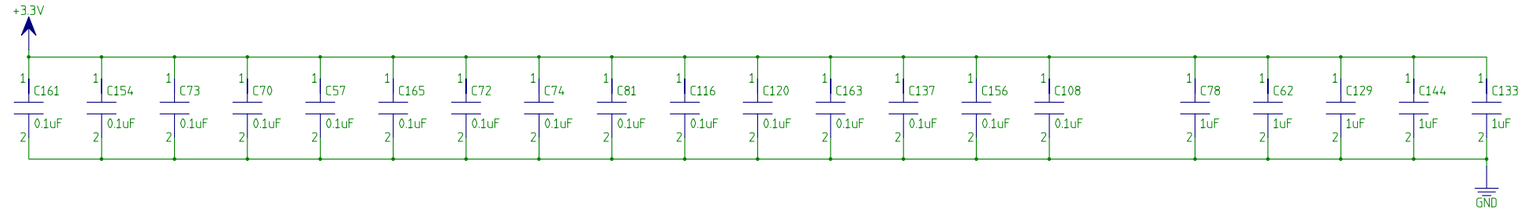

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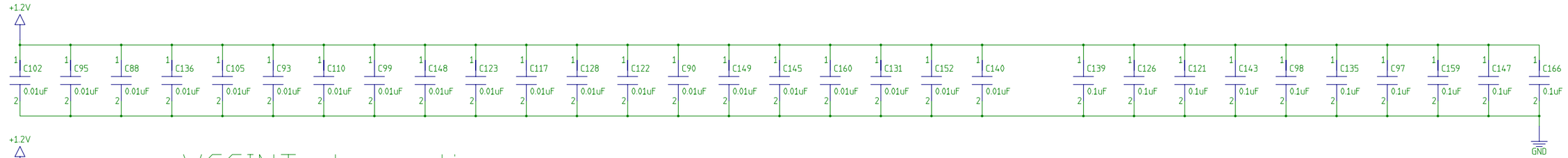
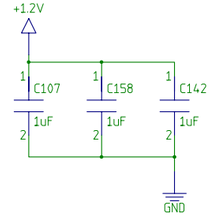
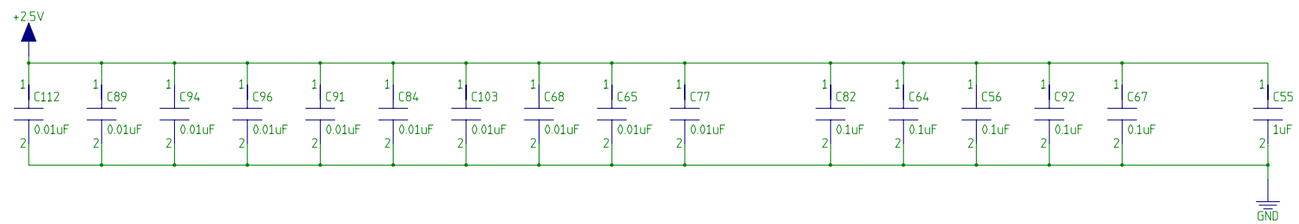
30 x 0.01uF 0402
15 x 0.1uF 0603
5 x 1uF 0805





VCCINT decoupling
20 x 0.01uF 0402
10 x 0.1uF 0603
3 x 1uF 0805



VCCAUX decoupling
10 x 0.01uF 0402
5 x 0.1uF 0603
1 x 1uF 0805

SORRY!

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FPGA / BYPASS CAPS

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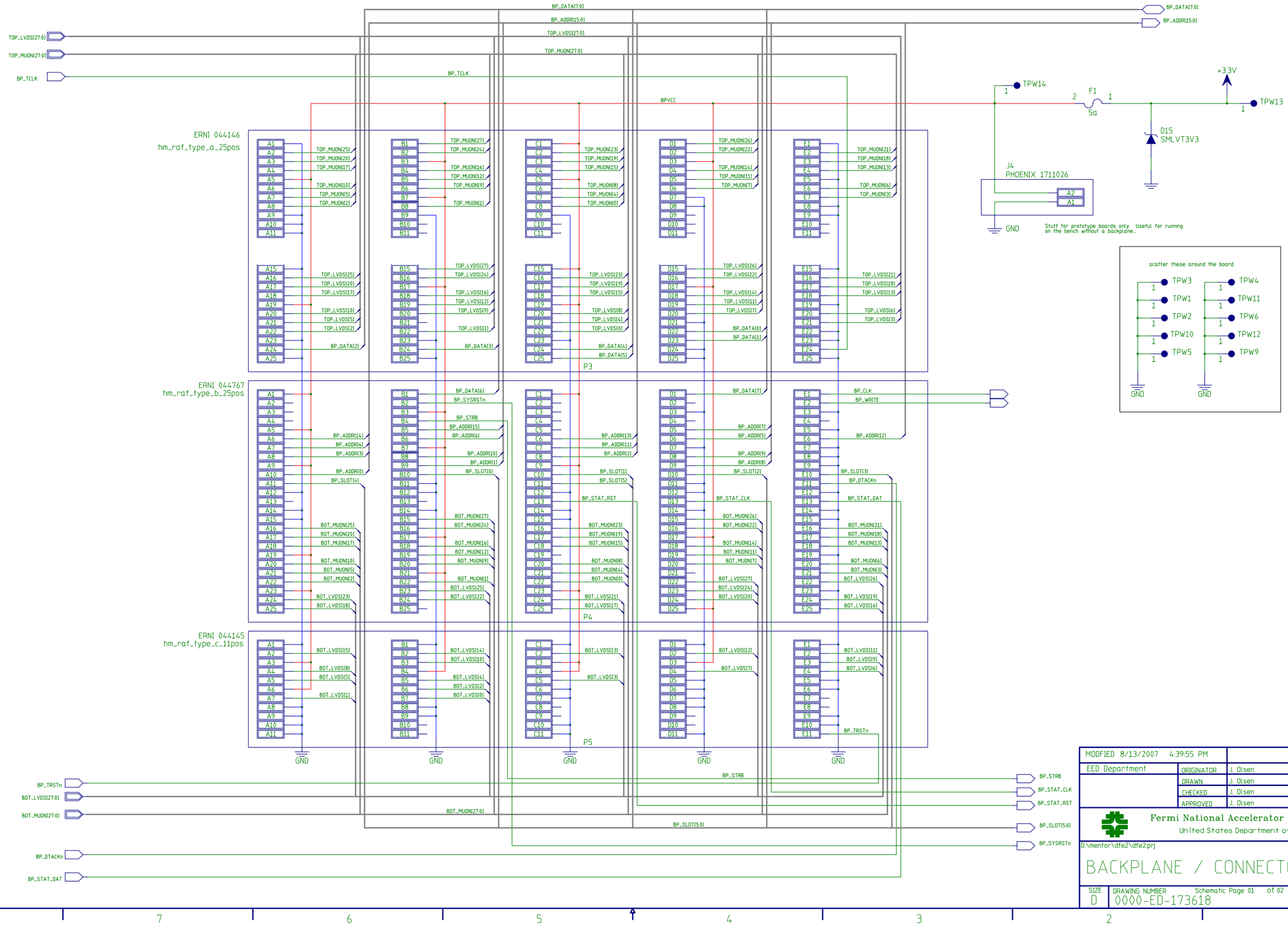

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BACKPLANE / CONNECTORS

SIZE	DRAWING NUMBER		REV
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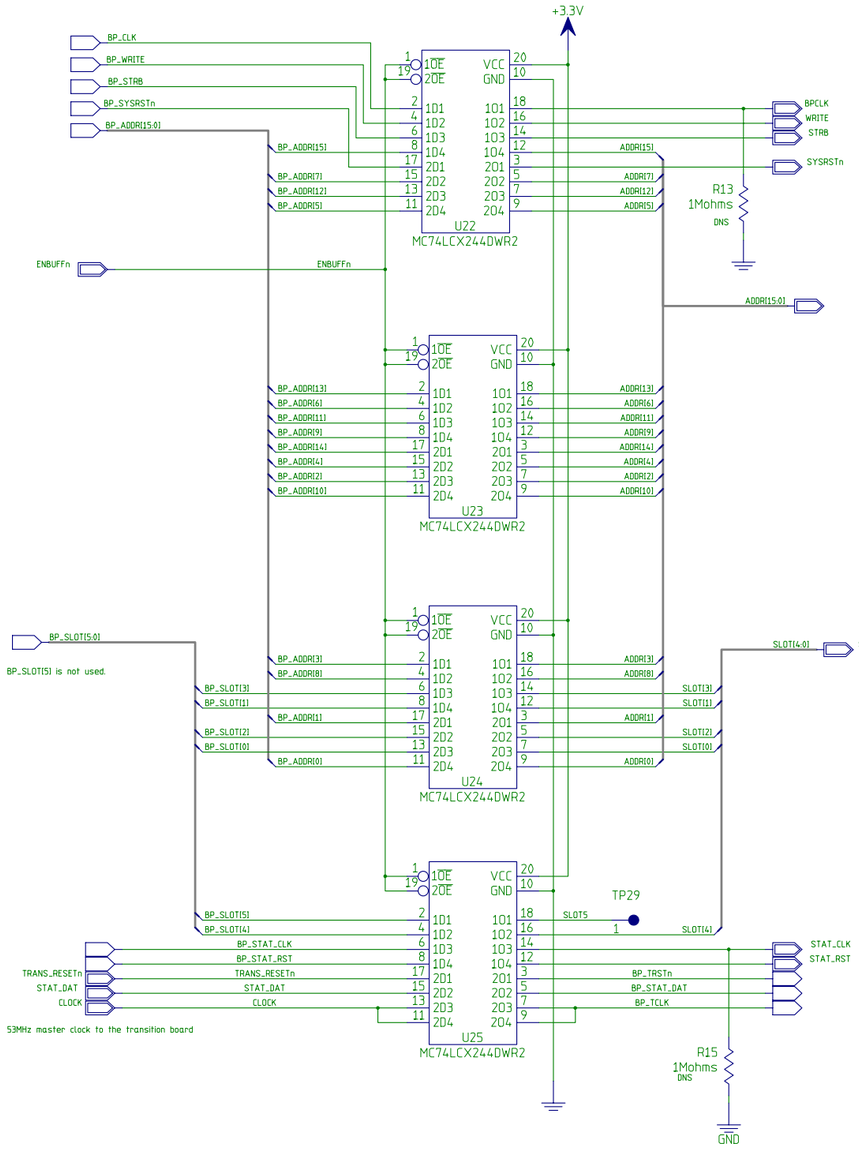

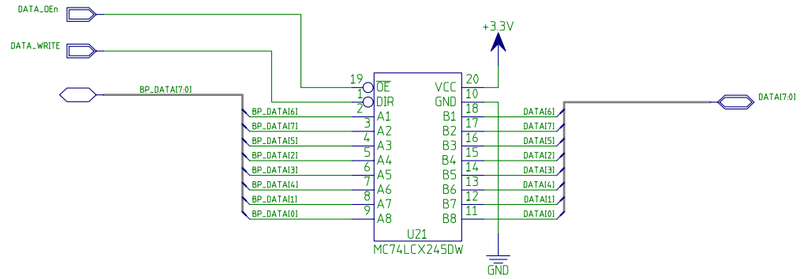

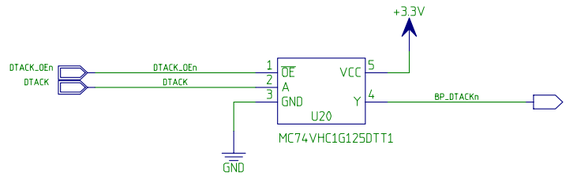

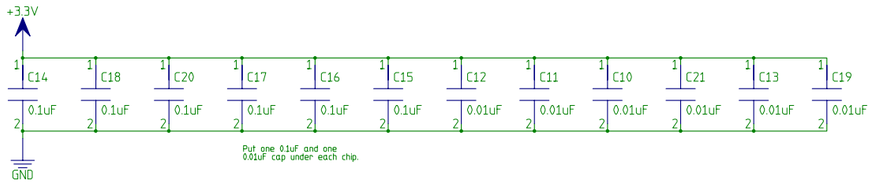

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BACKPLANE / BUFFERS

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