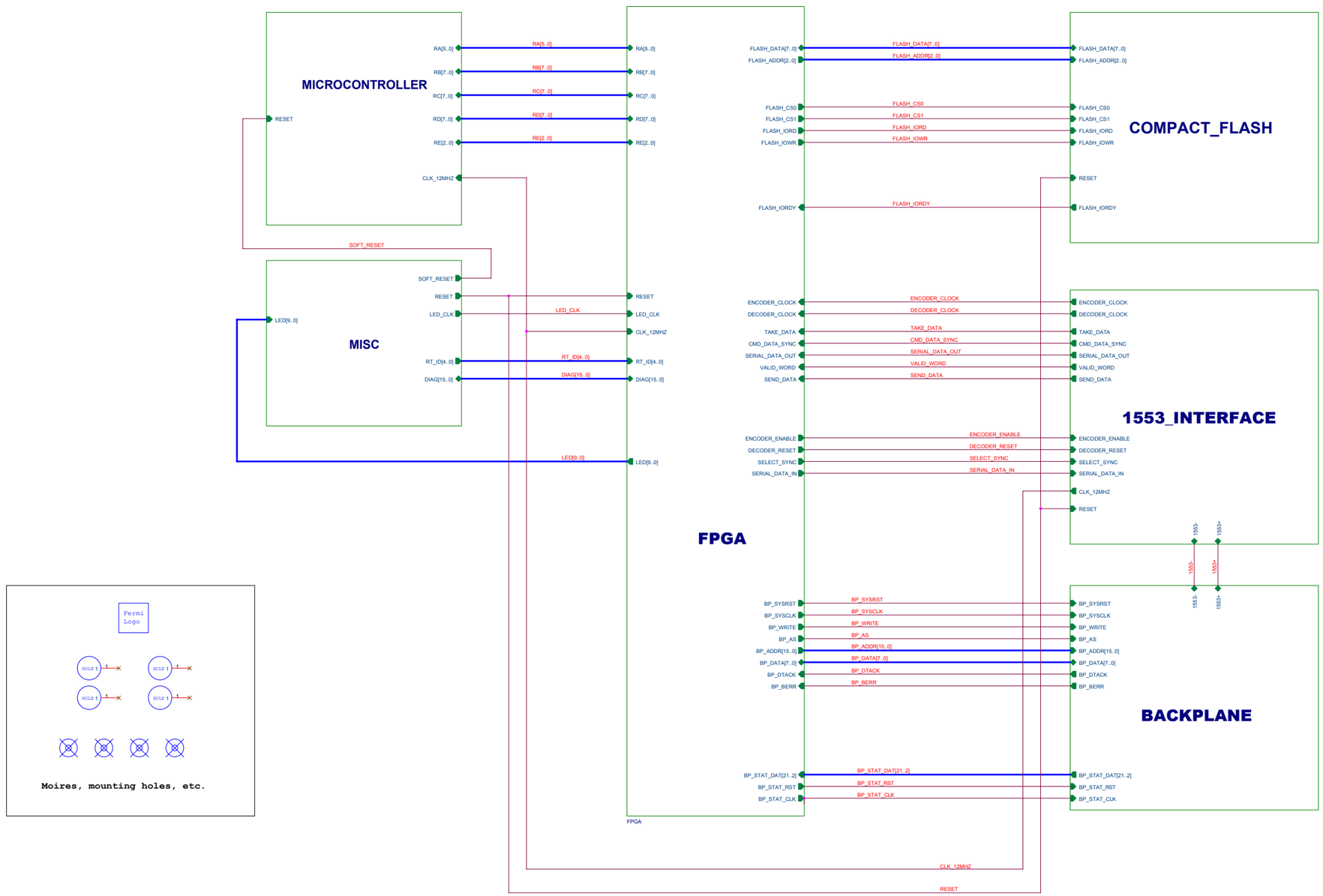
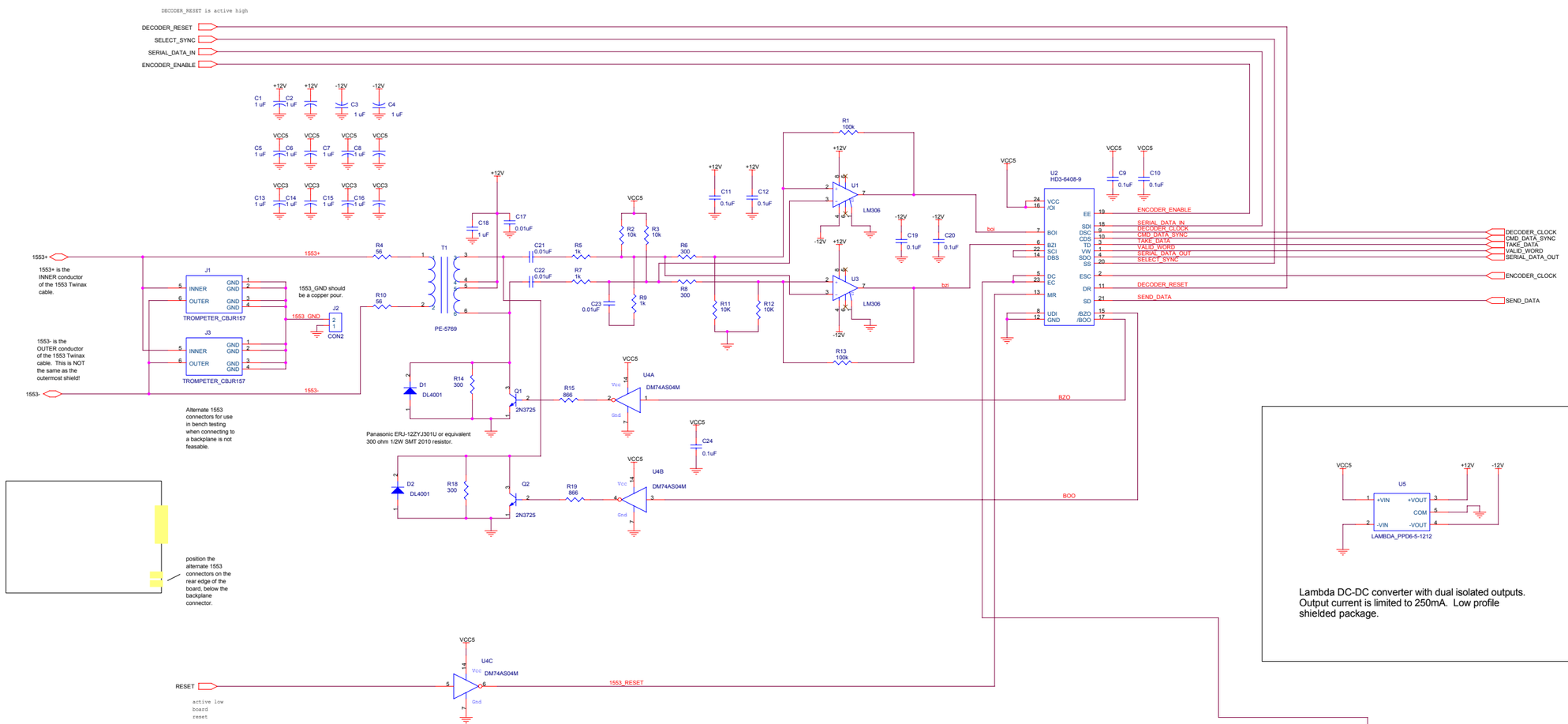
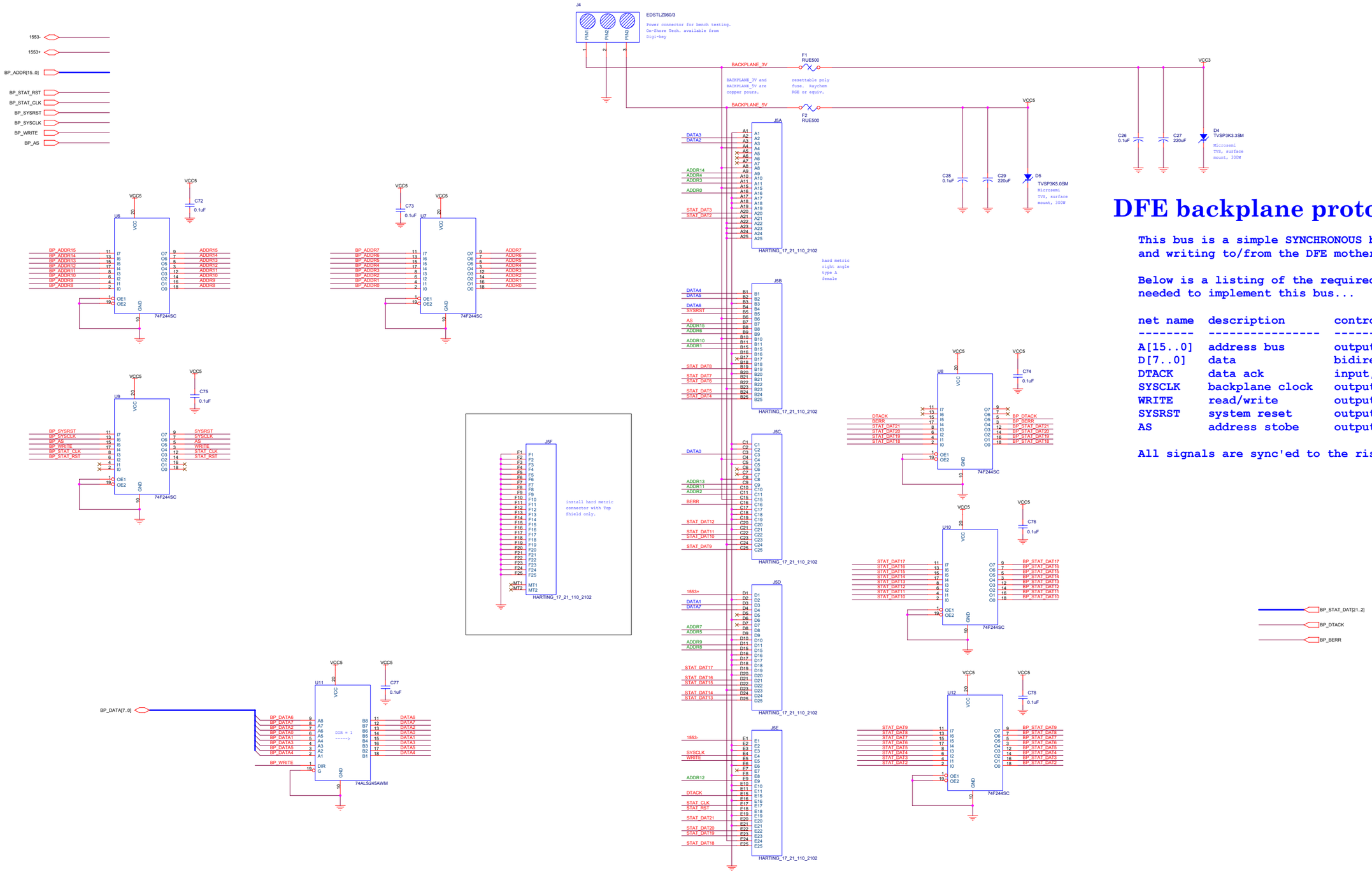


Fermi National Accelerator Laboratory PPD / E&TT / DZERO upgrade		
	design by:	J. Olsen
	drawn by:	J. Olsen
	drawing number	3823 113 ED 330318
name of board	Digital Front End Crate Controller	
size D	page name TOP LEVEL	revision A
Date: Wednesday, April 12, 2000	Sheet 1 of 7	



Fermi National Accelerator Laboratory PPD / E&TT / DZERO upgrade	
design by:	J. Olsen
drawn by:	J. Olsen
drawing number	3823 113 ED 330318
name of board	Digital Front End Crate Controller
size D	page name 1553 REMOTE TERMINAL INTERFACE
revision A	
Date: Friday, April 14, 2000	Sheet 2 of 7



DFE backplane protocol is not VME

This bus is a simple SYNCHRONOUS bus capable of reading and writing to/from the DFE motherboards.

Below is a listing of the required backplane signals needed to implement this bus...

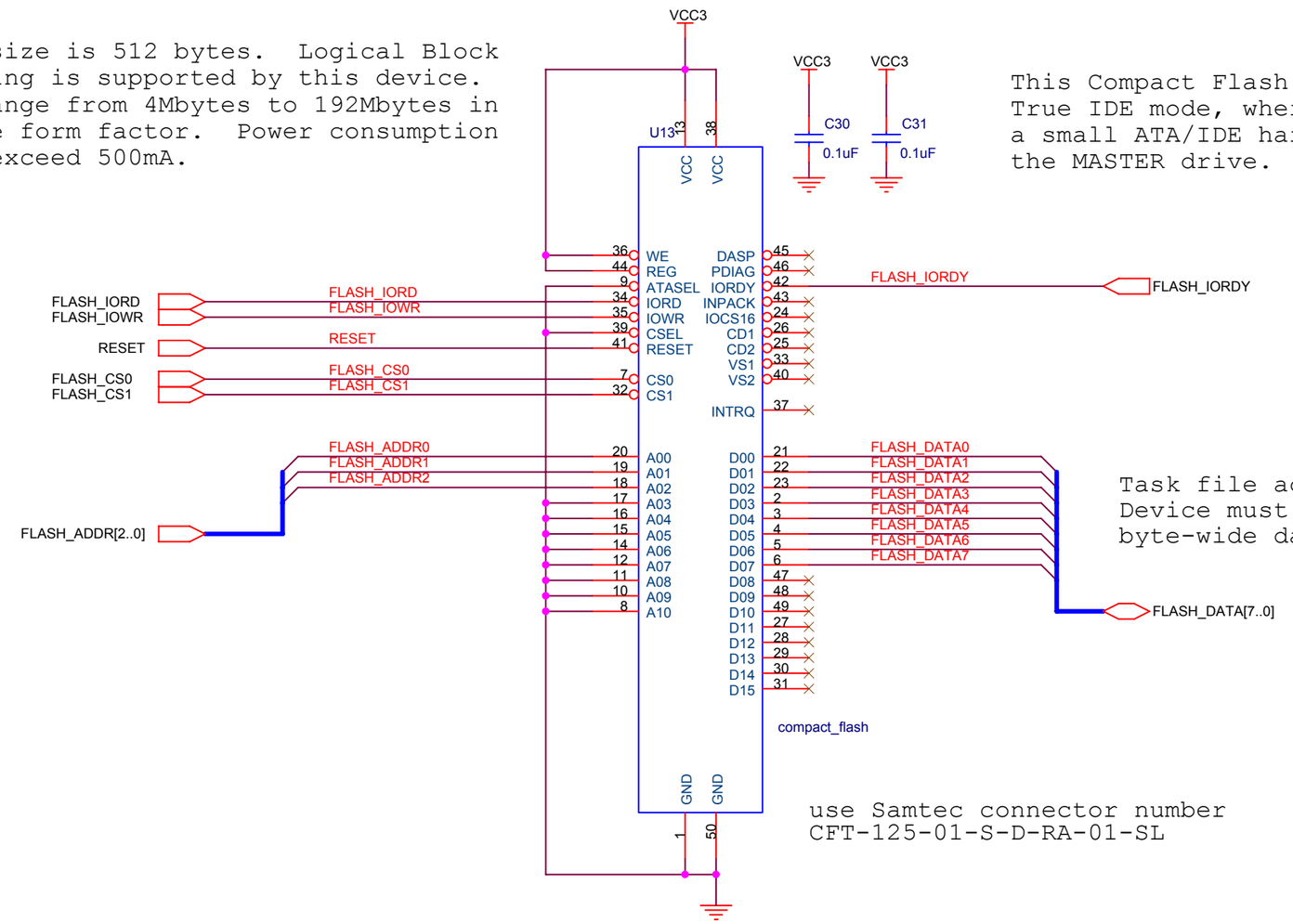
net name	description	controller board
A[15..0]	address bus	output
D[7..0]	data	bidirectional
DTACK	data ack	input, open drain, active low
SYSCLK	backplane clock	output, constant freq
WRITE	read/write	output, high to write
SYSRST	system reset	output, active low reset
AS	address stobe	output, valid address on the bus

All signals are sync'ed to the rising edge of sysclk.

Fermi National Accelerator Laboratory PPD / E&TT / DZERO upgrade	
design by:	J. Olsen
drawn by:	J. Olsen
drawing number	3823 113 ED 330318
name of board	Digital Front End Crate Controller
size D	page name: DFE BACKPLANE CONNECTOR
revision	A
Date:	Friday, April 14, 2000
Sheet	3 of 7

Sector size is 512 bytes. Logical Block Addressing is supported by this device. Sizes range from 4Mbytes to 192Mbytes in the same form factor. Power consumption not to exceed 500mA.

This Compact Flash device is hardwired in True IDE mode, where it will behave like a small ATA/IDE hard drive configured as the MASTER drive.

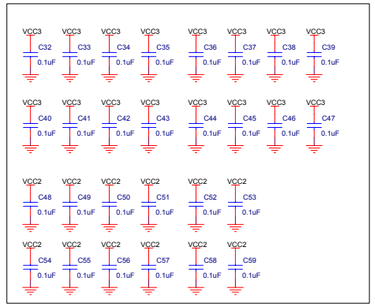


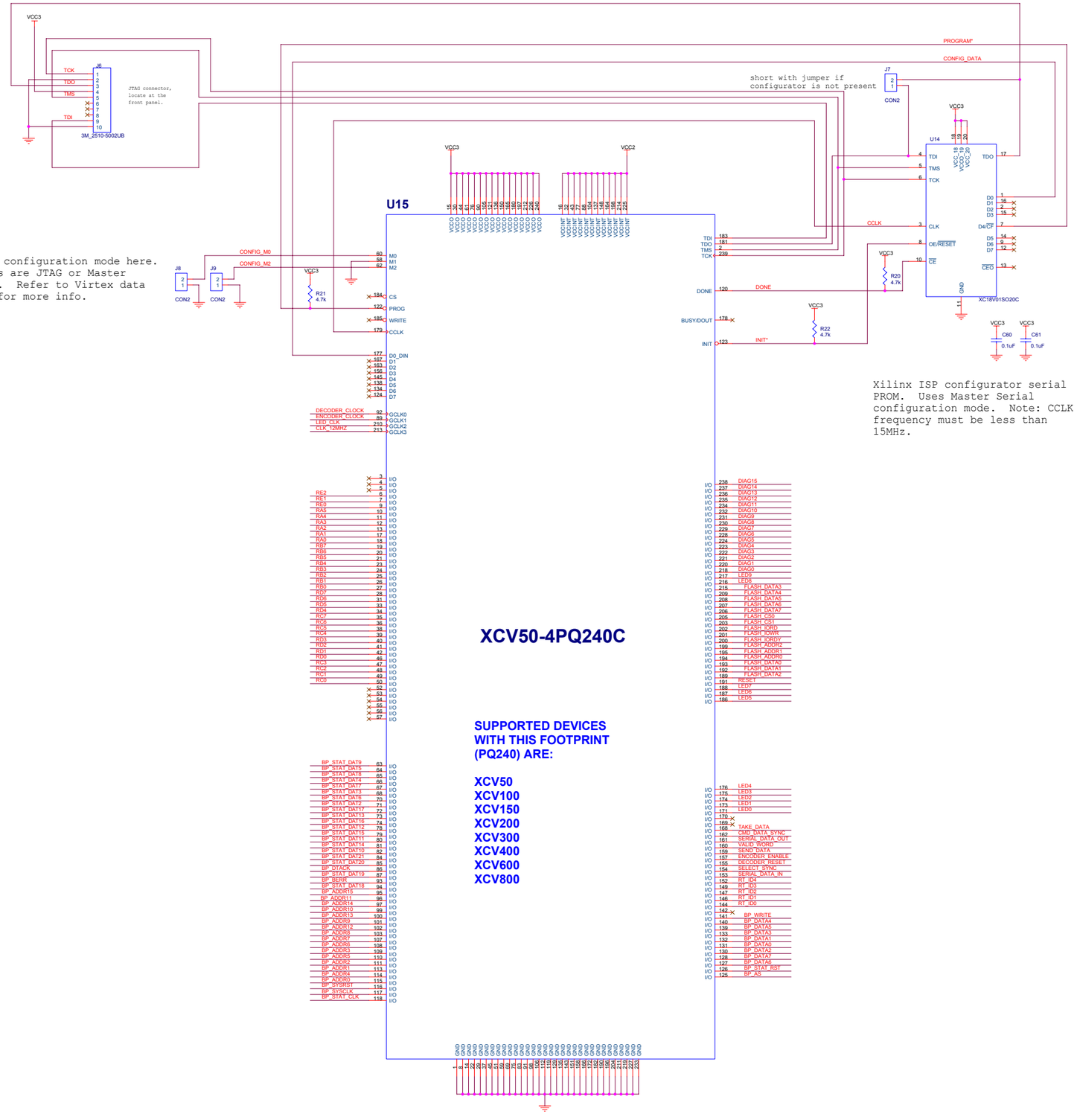
Task file access is always byte-wide. Device must be manually configured for byte-wide data transferrs, however.

use Samtec connector number CFT-125-01-S-D-RA-01-SL

Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

design by:	Jamieson Olsen
drawn by:	Jamieson Olsen
drawing number	3823 113 ED 330318
name of board	**Digital Front End Crate Controller**
size B	page name **COMPACT FLASH**
revision	A
Date:	Wednesday, April 12, 2000
Sheet	4 of 7





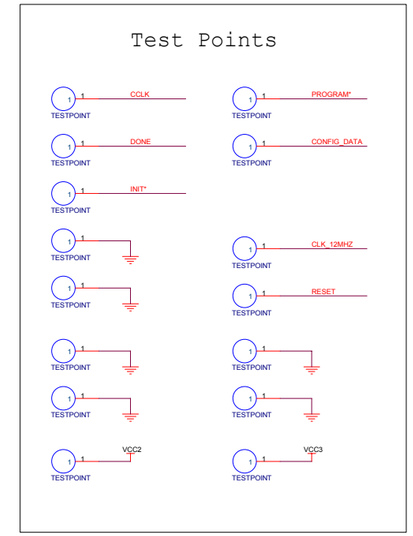
Select configuration mode here. Choices are JTAG or Master Serial. Refer to Virtex data sheet for more info.

Xilinx ISP configurator serial PROM. Uses Master Serial configuration mode. Note: CCLK frequency must be less than 15MHz.

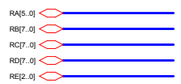
XCV50-4PQ240C

SUPPORTED DEVICES WITH THIS FOOTPRINT (PQ240) ARE:

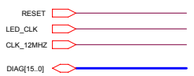
XCV50
XCV100
XCV150
XCV200
XCV300
XCV400
XCV600
XCV800



Bi-directional Communication with the MicroController

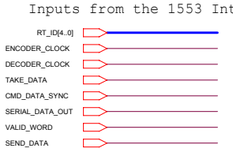


General board inputs

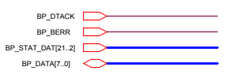


Inputs from the Compact Flash

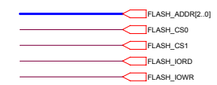
Inputs from the 1553 Interface



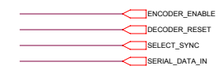
Inputs from the Backplane



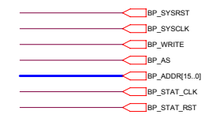
Outputs to the Compact Flash



Outputs to the 1553 Interface

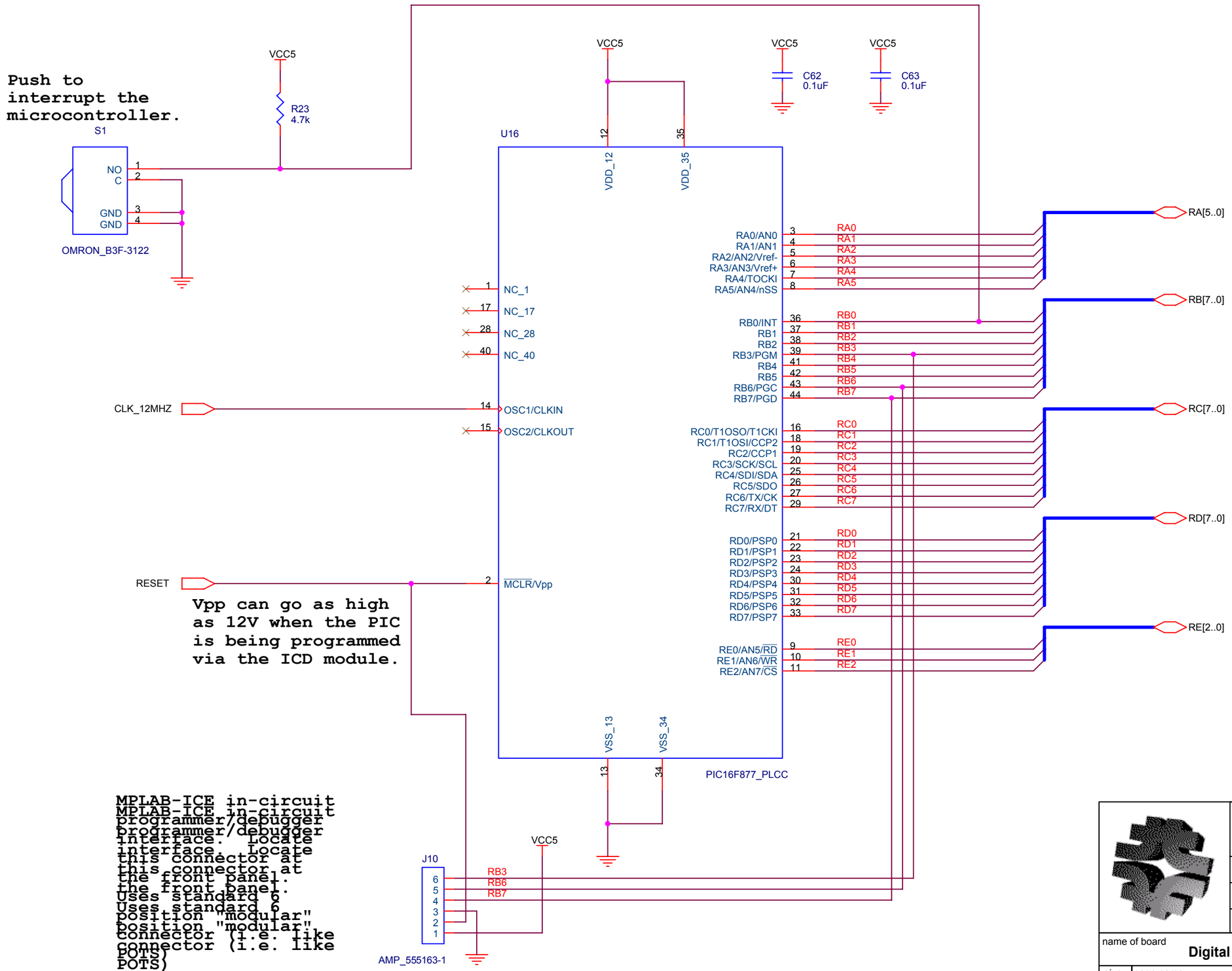


Outputs to the Backplane Drivers



Front Panel LEDs

Fermi National Accelerator Laboratory PPD / E&TT / DZERO upgrade	
design by:	Jamieson Olsen
drawn by:	Jamieson Olsen
drawing number	3823 113 ED 330318
name of board	Digital Front End Crate Controller
size D / page name	CONTROL LOGIC FPGA / revision A
Date: Friday, April 14, 2000	Sheet 5 of 7



Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

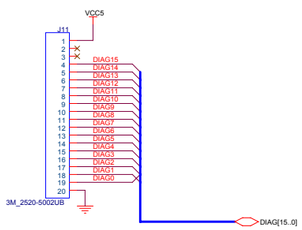
design by:	J. Olsen
drawn by:	J. Olsen
drawing number	3823 113 ED 330318

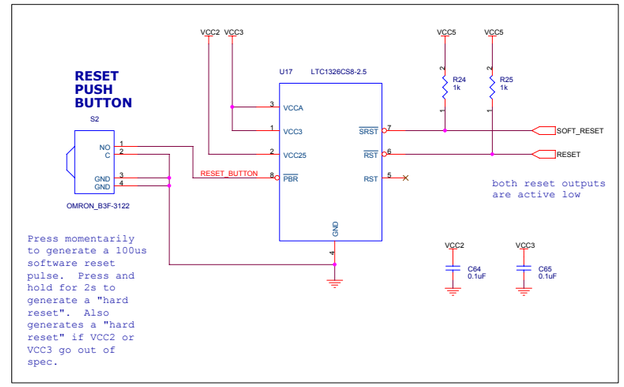
name of board: **Digital Front End Crate Controller**

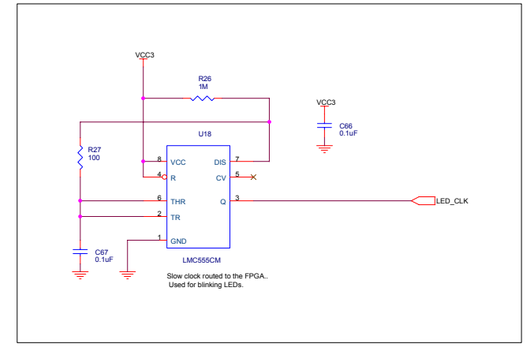
size	page name	revision
B	**PIC MICROCONTROLLER**	A

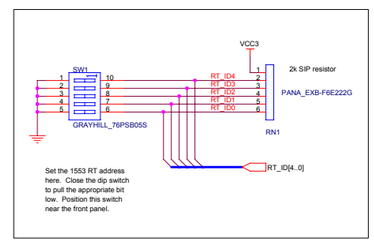
Date: Friday, May 19, 2000 Sheet 6 of 7

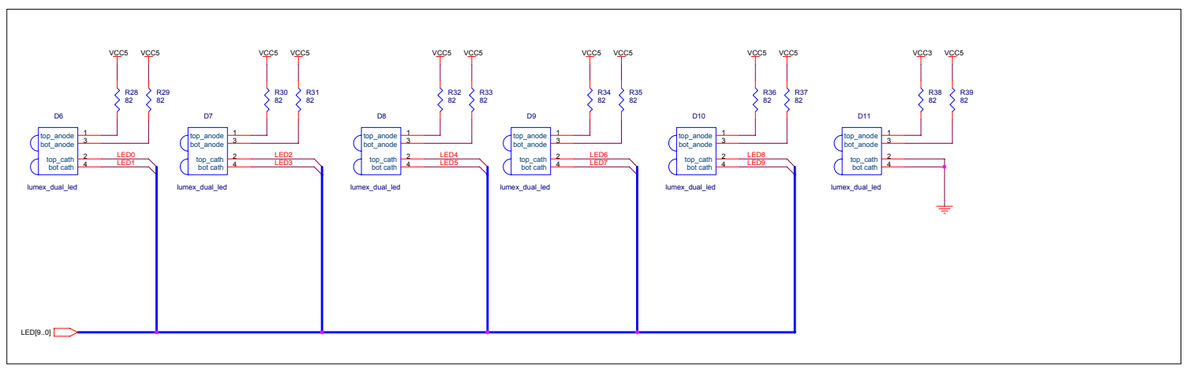
Logic Analyser Connector use right angle 4-wall version and mount near the front panel.

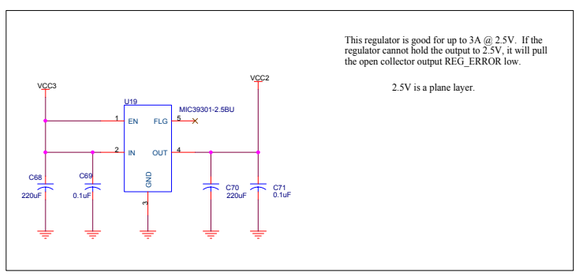












This regulator is good for up to 3A @ 2.5V. If the regulator cannot hold the output to 2.5V, it will pull the open collector output REG_ERROR low.

2.5V is a plane layer.

Fermi National Accelerator Laboratory PPD / E&TT / DZERO upgrade	
design by:	J. Olsen
drawn by:	J. Olsen
drawing number	3823 113 ED 330318
name of board	Digital Front End Crate Controller
size D	page name: Front Panel
revision	A
Date:	Thursday, April 13, 2000
Sheet	7 of 7