

# Digital Front End Motherboard

## Printed Circuit Board Fabrication

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### General Information

board revision: **C**  
board size: 233.25mm x 320mm (6U x 320mm)  
board thickness: **0.0845" final pressed thickness**  
board material: FR4  
layers: 6  
controlled impedance: Yes  
copper: **½ oz TOP and BOTTOM, 1oz all other layers**  
solder mask: BOTH sides, LPI, Black  
silk screen: BOTH sides, White  
traces: 7/7 on top, bottom; 8/8 inners  
finish: ENTEK (organic)

### Filenames

All gerbers are POSITIVE IMAGE. Gerber files are in RS254-X format.

TOP routing layer	dfem_top.gbx
GROUND plane	dfem_gnd.gbx
TOP INNER routing layer	dfem_in1.gbx
BOT INNER routing layer	dfem_in2.gbx
POWER plane	dfem_pwr.gbx
BOTTOM routing layer	dfem_bot.gbx
soldermask top	dfem_smt.gbx
soldermask bottom	dfem_smb.gbx
silkscreen top	dfem_sst.gbx
silkscreen bottom	dfem_ssb.gbx
solder paste top	dfem_spt.gbx
solder paste bot	dfem_spb.gbx
drill tape #1	thruhole.tap
drill tape #2	2_7.tap
fabrication drawing	dfem_drd.gbx
assembly drawing top	dfem_ast.gbx
assembly drawing bottom	dfem_asb.gbx

## Controlled Impedance

Table 1 shows a possible board layer stack-up to provide the microstrip and stripline characteristic impedance of  $90\Omega$  on the top and bottom routing layers. For the inner two routing layers impedance must be controlled to  $100\Omega$  differential (broadside coupled stripline). **The vendor has the liberty to adjust these dimensions to suit their manufacturing process in order to archive this goal.**

The characteristic impedance on the top and bottom layers should be  $90\Omega$  ( $\pm 10\%$ ) and  $100\Omega$  differential ( $\pm 10\%$ ) on the inner two layers. The characteristic impedance must not vary by more than 5% from board to board.

1. TOP ROUTING LAYER (“COMPONENT” SIDE)

**0.0165” core**

2. PLANE LAYER

**0.014” prepreg**

3. TOP INNER ROUTING LAYER

**0.0165” core**

4. BOTTOM INNER ROUTING LAYER

**0.014” prepreg**

5. PLANE LAYER

**0.0165” core**

6. BOTTOM ROUTING LAYER (“SOLDER” SIDE)

*Table 1. Possible layer arrangement used to give characteristic impedances mentioned above.  
Note the layer designations correspond to the layers given in the PCB design file.*

## Colors

- soldermask: black
- silkscreen: white

## Thruholes

- **9** different hole sizes
- **3312** holes total
- 0.330mm (13 mil) hole is smallest
- 2.794mm (110 mil) hole is largest
- no blind or buried vias
- refer to dfem\_drd.gbr for fabrication data and hole legend

## **Contact Prints**

The vendor will generate all necessary artwork and supply a full set of contact prints for each of the prototype and production runs as soon as they can be made available.

## **Board Testing**

Bare boards must be tested with either a flying head probe or a bed of nails fixture. Bare boards must pass a netlist connectivity test prior to stuffing. Defective boards shall not be modified using jumper wires, conductive paint, etc. in order to get them to pass the connectivity test. Each tested good board must be stamped or marked with paint.

## **Mechanical Considerations**

The overall board dimensions are 233.25mm x 320mm. The finished board shall be provided per the Digital Front End Motherboard Dimensions drawing to the indicated tolerances and be free of burrs and slivers and have smooth edges. The edges of the board must be milled to the dimensions specified in the assembly layer top gerber file.

## **Quantity**

125 boards will be fabricated. Ten initial boards plus 115 after Fermilab checkout.

## **Revision History**

B	12 Jan 2000	Original document/artwork released for quotation
C	18 Apr 2000	Modify hard metric connector footprints J1, J2, and J14 to accept Harting hard metric connectors. Push and shove traces on all routing layers to accept the new footprints.  Incorporate the approved Compunetics CORE and PREPREG thicknesses into this document. Change the final pressed thickness to match the approved Compunetics specification.  Removed the board warpage specification from the Mechanical Considerations section of this document.