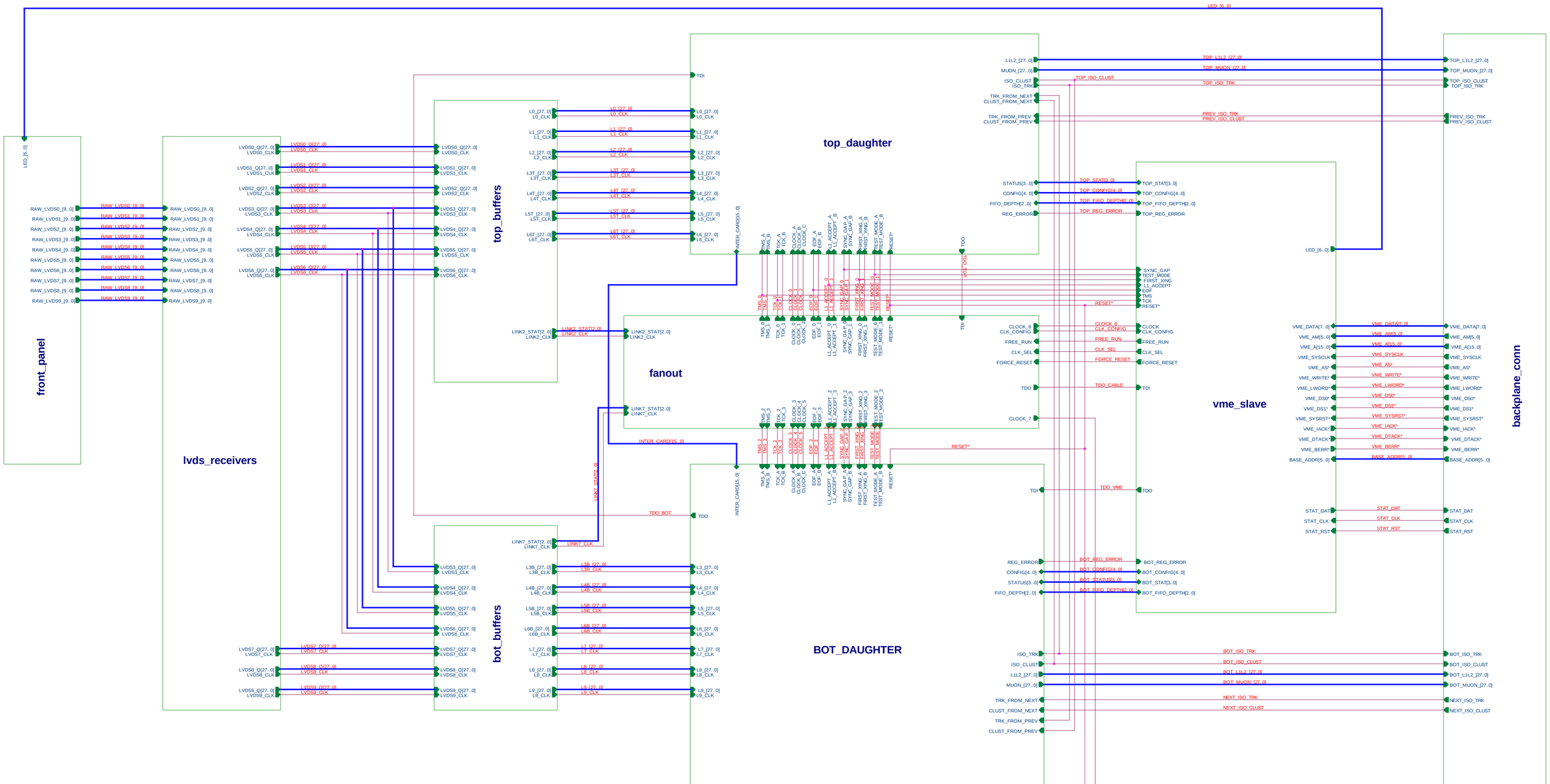
DIGITAL FRONT END MOTHERBOARD rev B -- TOP LEVEL



JTAG

JTAG CONNECTOR IS CONTAINED IN THE FANOUT BLOCK. THE DEVICE CHAIN IS AS FOLLOWS:

1. VME CLPD XC95288XL-10TC144C
2. BOTTOM DAUGHTERCARD*
3. TOP DAUGHTERCARD*
4. TIMING CPLD XC9572XL-10VQ64C

* DAUGHTERCARDS CAN BE BYPASSED WITH A JUMPER ON THE MOTHERBOARD. UP TO 8 JTAG DEVICES ARE SUPPORTED ON EACH OF THE DAUGHTERCARDS.

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design by Jamieson Olsen <jamieson@fnal.gov>

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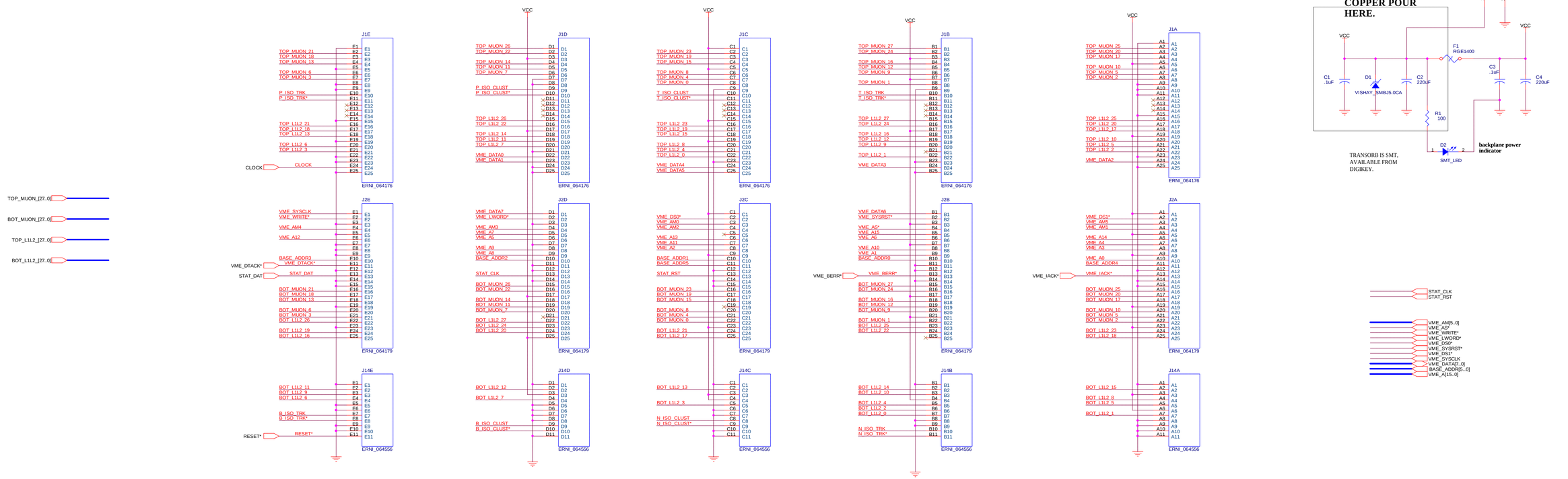
HORIZONTAL TERMINAL BLOCK FOR BENCH TESTING. POSITION NEAR THE BACK OF THE BOARD, POINTING TOWARDS THE EDGE OF THE BOARD. ON-SHORE TECH MODEL ED1865. REQUIRES A SECOND PIECE, MODEL ED1773.

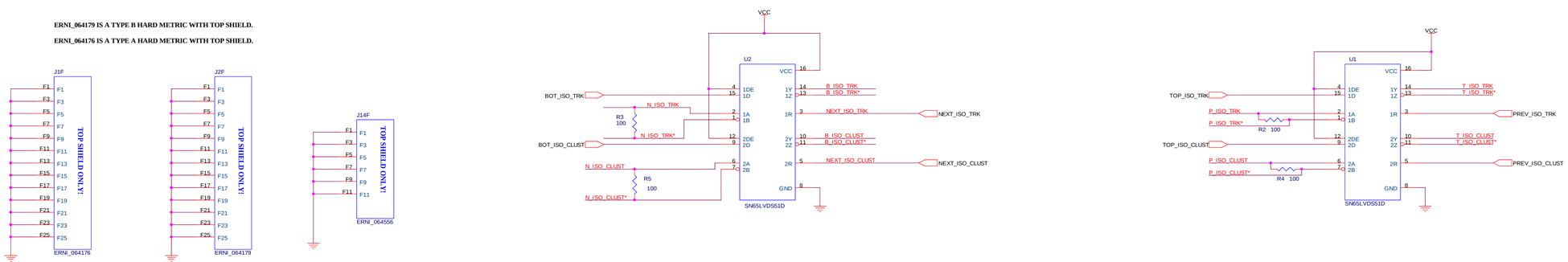
PANASONIC METAL CAN CAP, AVAILABLE FROM DIGIKEY. 220uF NOTE CASE OUTLINE IS LARGER THAN FOOTPRINT...



ROW "F" IS RESERVED FOR THE TOP SHIELD. THE FOOTPRINT DOES NOT ALLOW FOR A BOTTOM SHIELD TO BE FITTED, SINCE EVEN NUMBERED THROUGH HOLES IN ROW "F" ARE NOT PRESENT.

ERNI_064179 IS A TYPE B HARD METRIC WITH TOP SHIELD.

ERNI_064176 IS A TYPE A HARD METRIC WITH TOP SHIELD.



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Title	DIGITAL FRONT END BOARD -- J2 BACKPLANE CONN	
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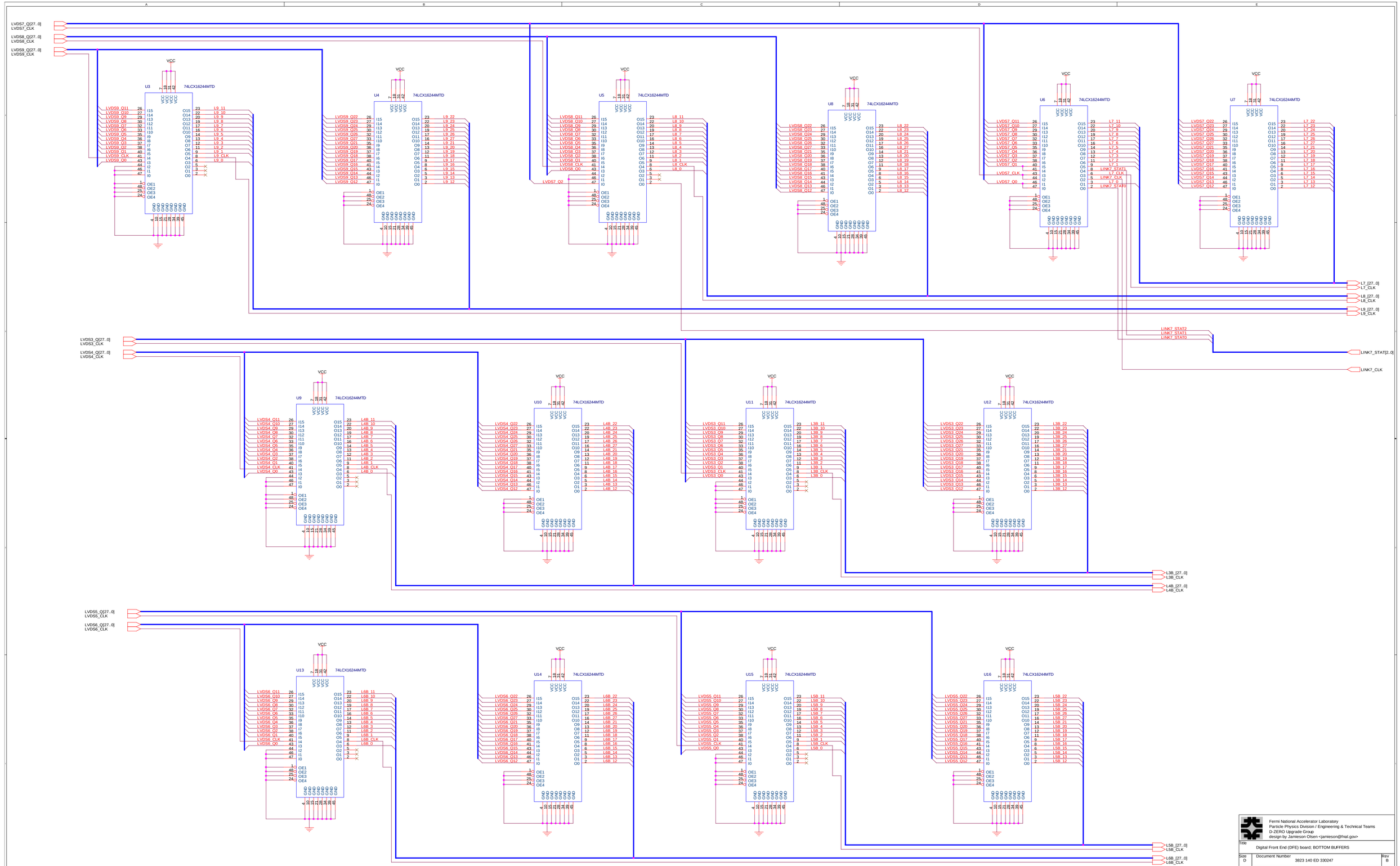

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Title: Digital Front End (DFE) board; BOTTOM BUFFERS

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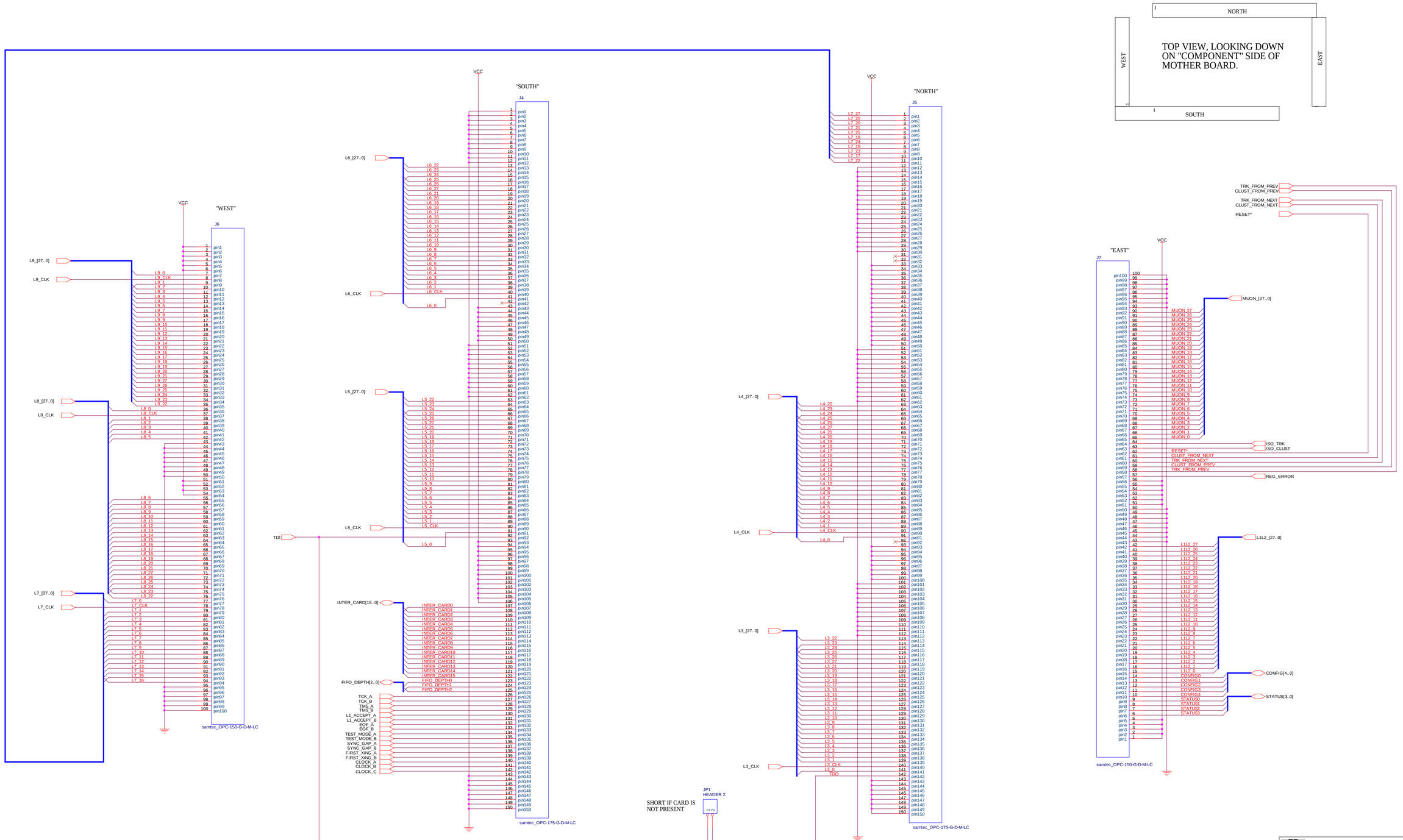

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Title	DFE: BOT DAUGHTERBOARD CONNECTORS	
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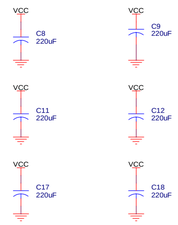
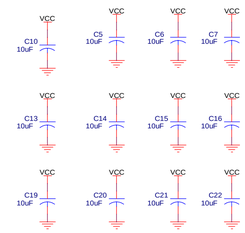
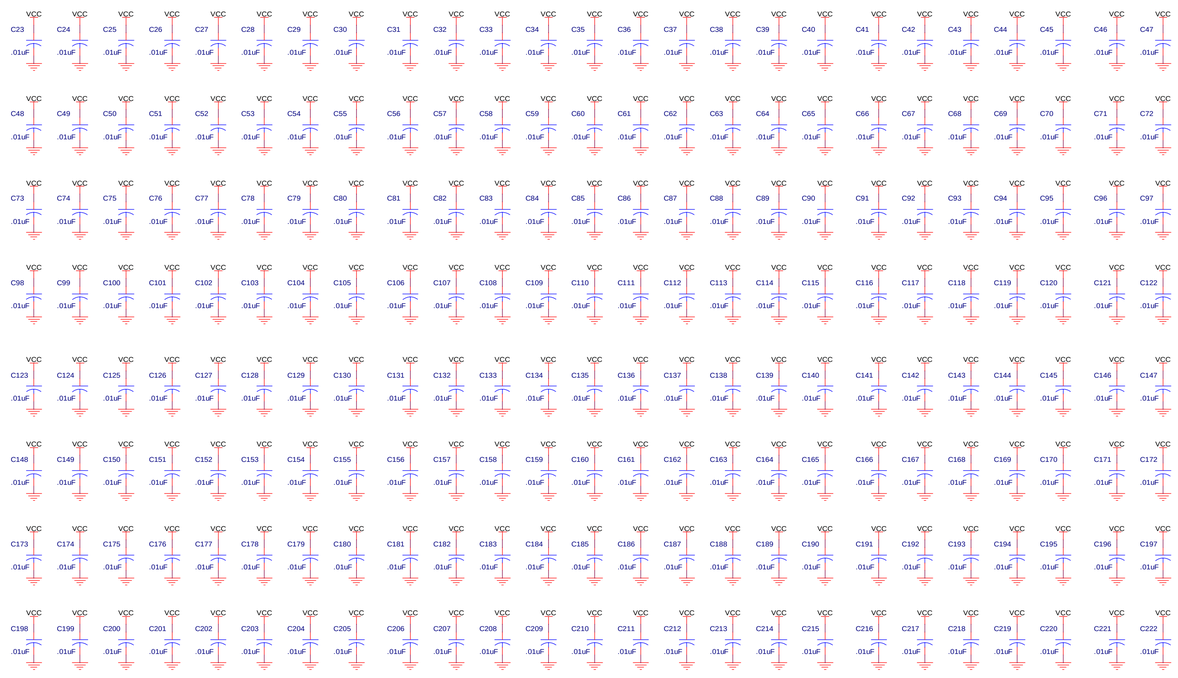
USE PANASONIC V0GA221P SMALL CAN SMT
DEVICES HERE (DIGIKEY)



USE PANASONIC ECS-T0JY106R SMT
DEVICES HERE. FOOTPRINT IS STANDARD
3216 STYLE. (DIGIKEY)





FOR THESE JUST USE 0805 .01 uF CAPS,
NPO, X7R, ETC.

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Title: **DIGITAL FRONT END BOARD -- BYPASS CAPS**

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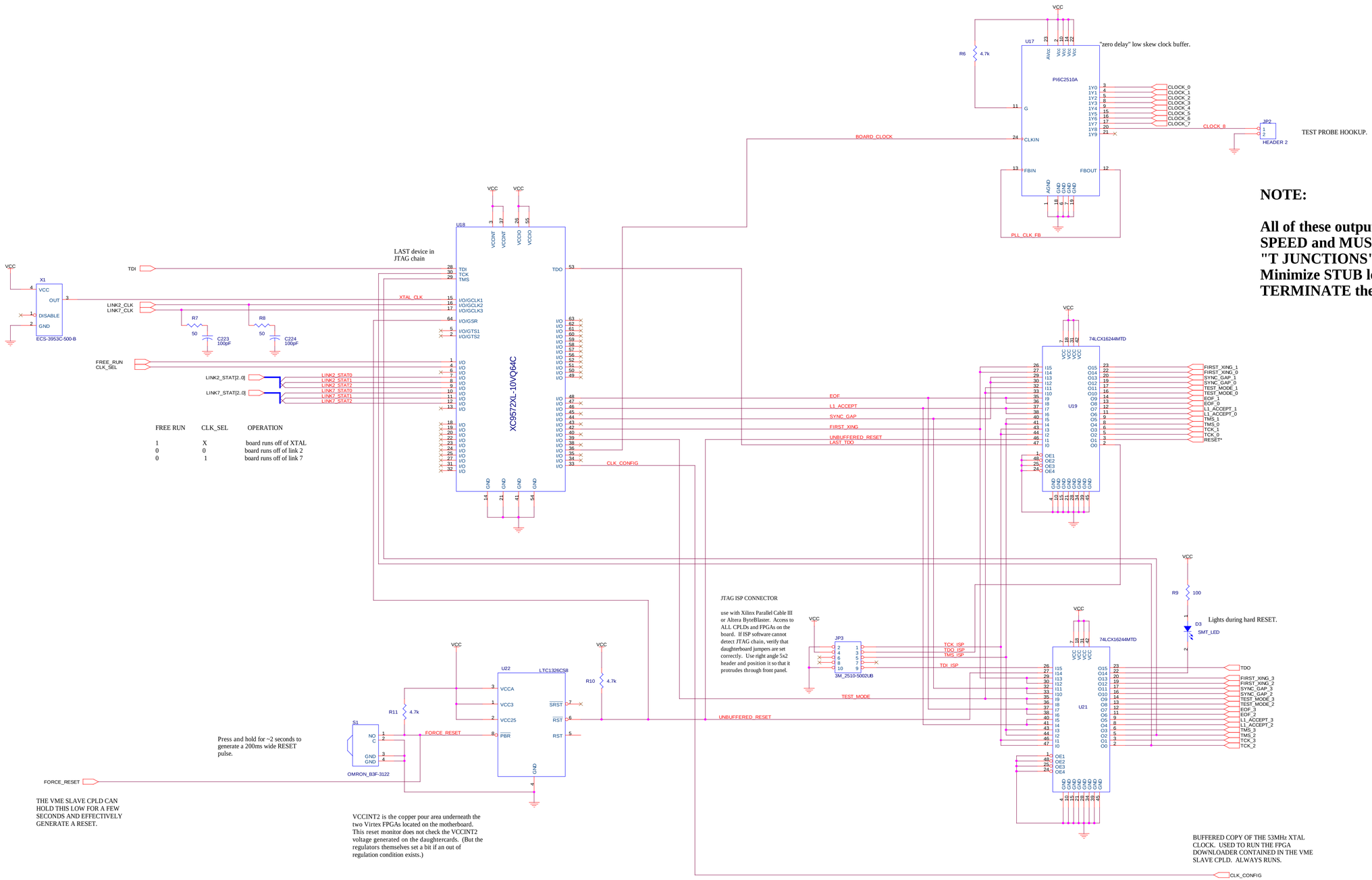

FREE RUN	CLK_SEL	OPERATION
1	X	board runs off of XTAL
0	0	board runs off of link 2
0	1	board runs off of link 7

NOTE:

All of these output nets are HIGH SPEED and MUST be routed without "T JUNCTIONS" and BRANCHES. Minimize STUB length and AC TERMINATE the end of the trace.

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Title: **DIGITAL FRONT END BOARD – FANOUT AND CONTROL**

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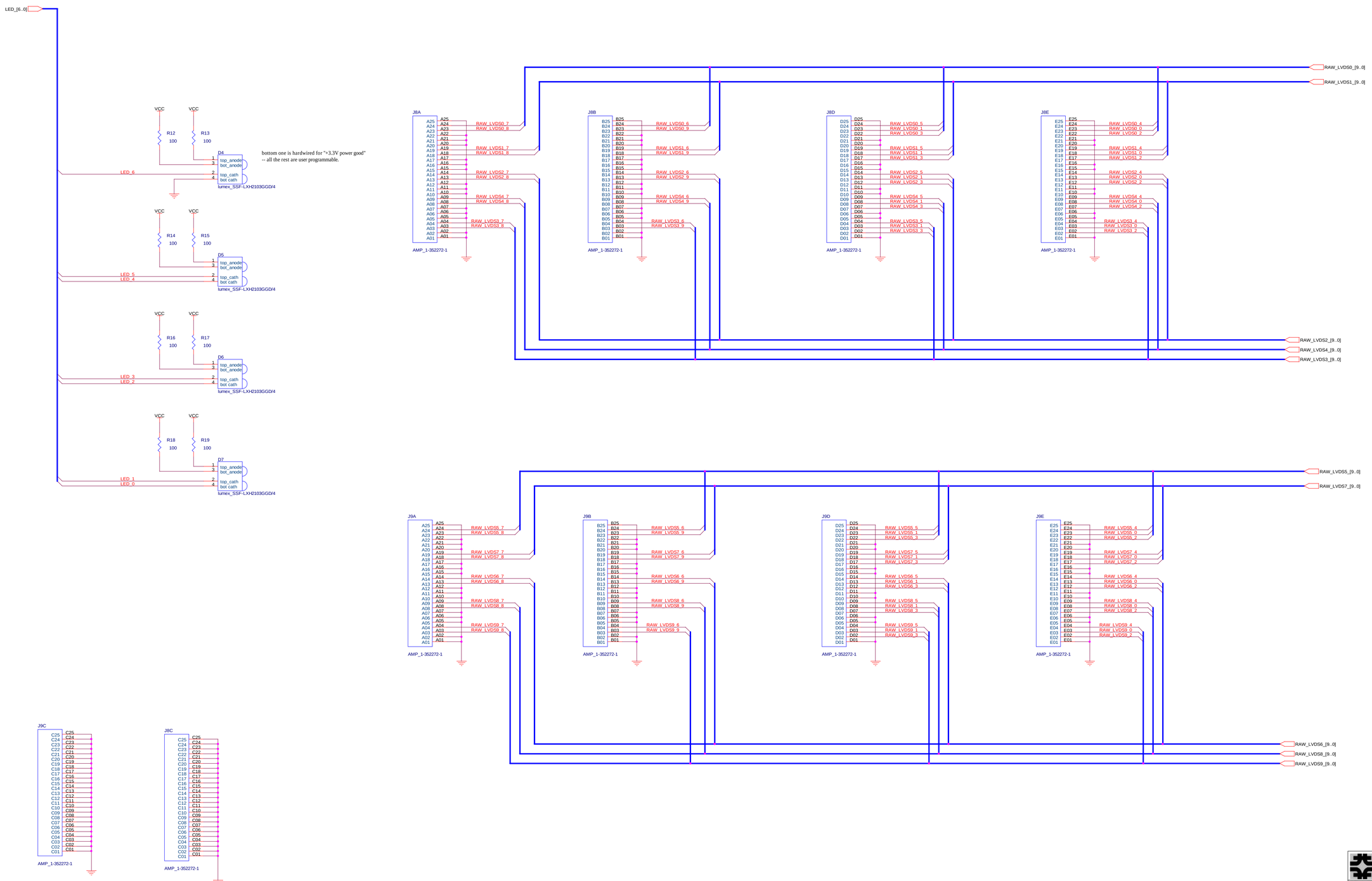

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Title: **DIGITAL FRONT END BOARD -- FRONT PANEL**

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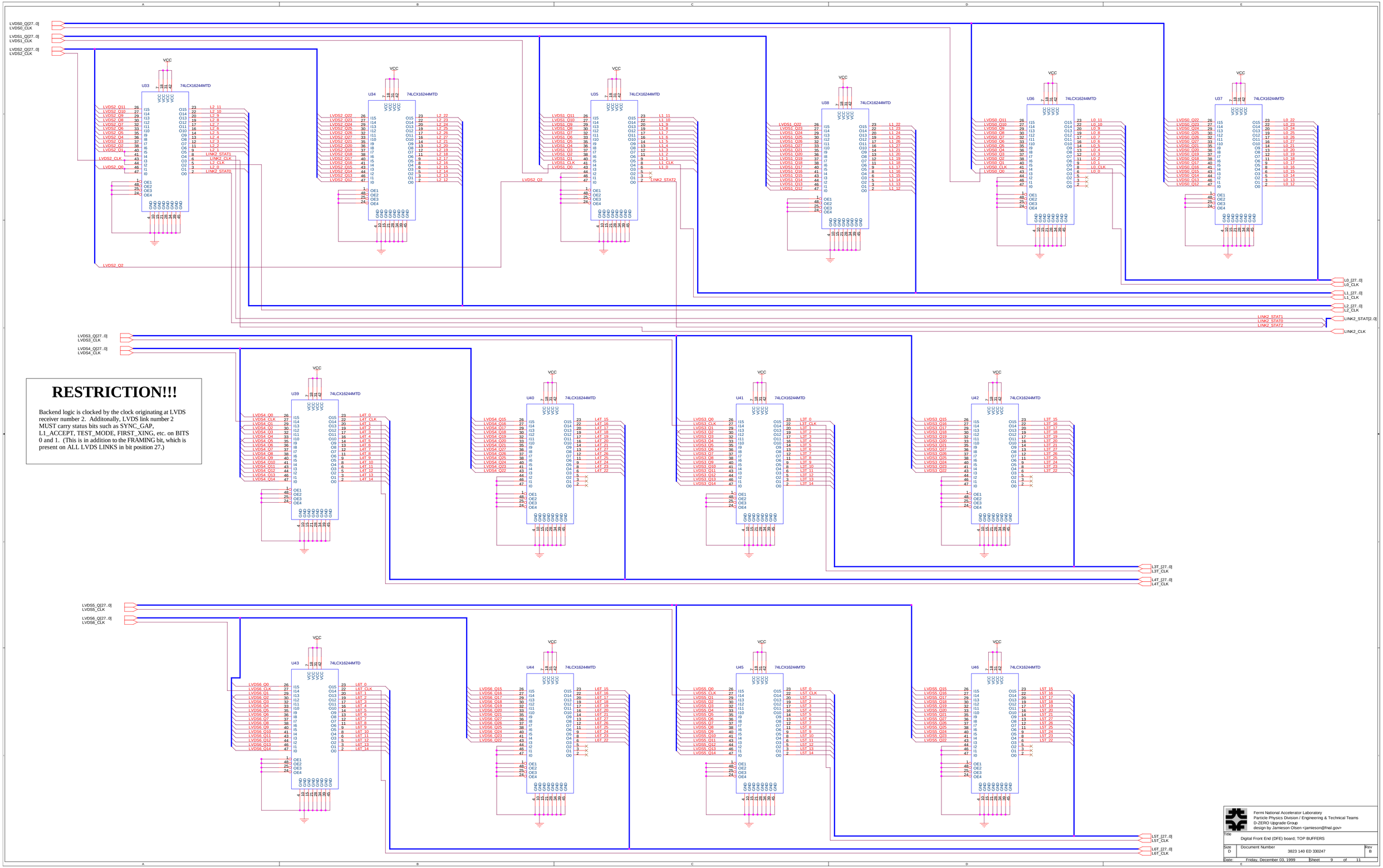

RESTRICTION!!!

Backend logic is clocked by the clock originating at LVDS receiver number 2. Additonally, LVDS link number 2 MUST carry status bits such as SYNC_GAP, L1_ACCEPT, TEST_MODE, FIRST_XING, etc. on BITS 0 and 1. (This is in addition to the FRAMING bit, which is present on ALL LVDS LINKS in bit position 27.)

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Title	Digital Front End (DFE) board; TOP BUFFERS	
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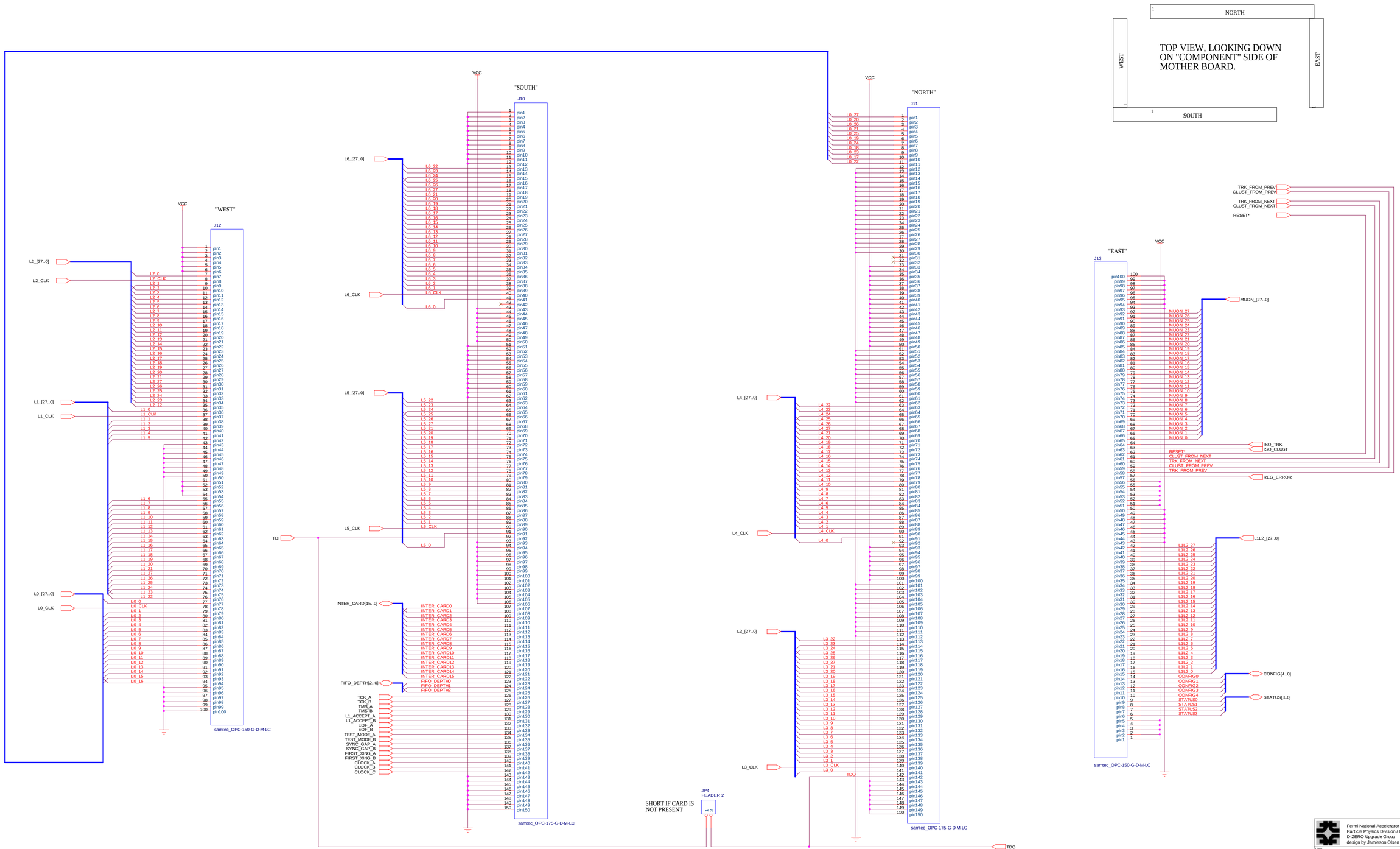

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Title: **DFE: TOP DAUGHTERBOARD CONNECTORS**

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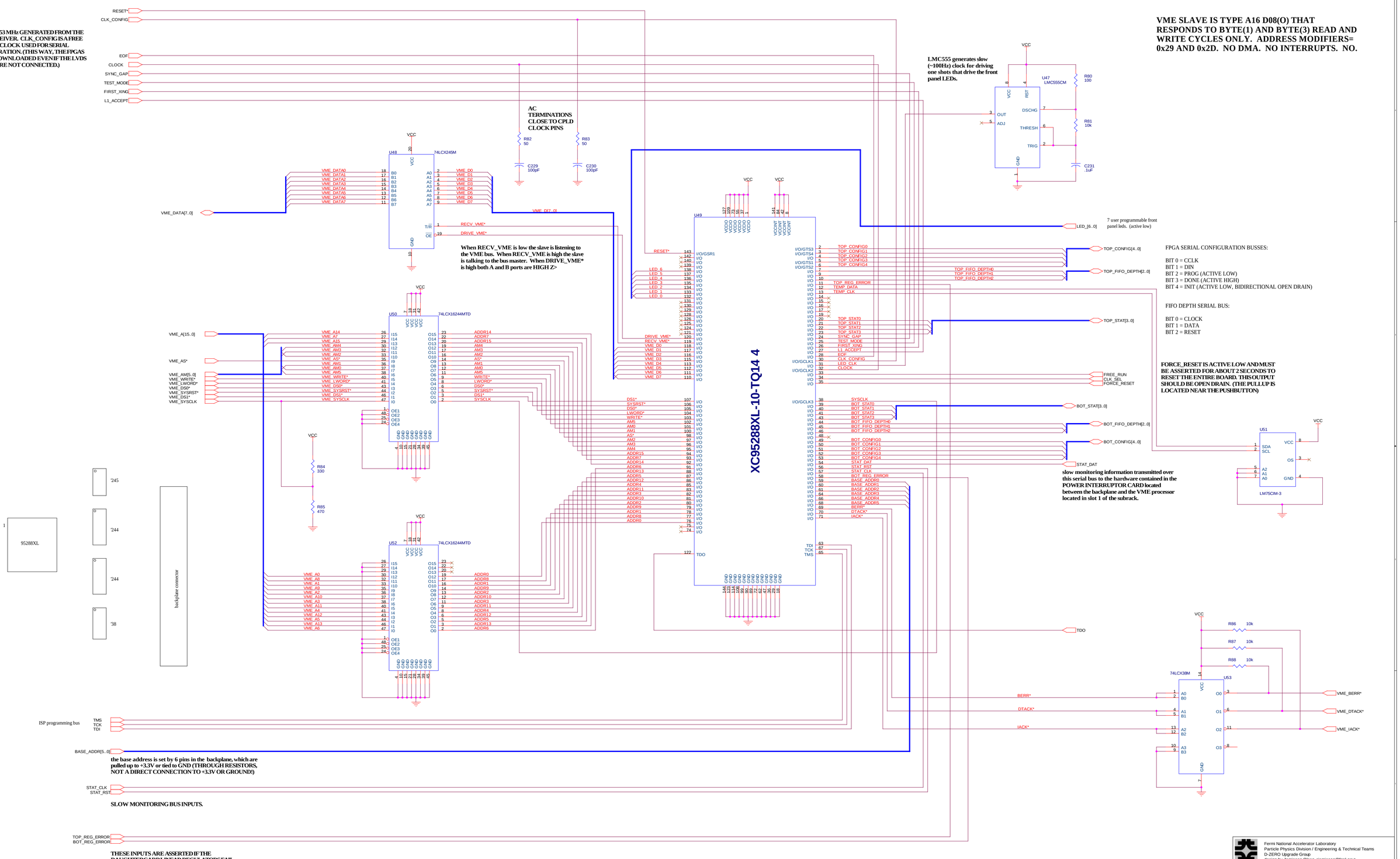
CLOCK IS 53 MHz GENERATED FROM THE LVDS RECEIVER. CLK_CONFIG IS A FREE RUNNING CLOCK USED FOR SERIAL CONFIGURATION. (THIS WAY, THE FPGAS CAN BE DOWNLOADED EVEN IF THE LVDS CABLES ARE NOT CONNECTED.)
VME SLAVE IS TYPE A16 D08(O) THAT RESPONDS TO BYTE(1) AND BYTE(3) READ AND WRITE CYCLES ONLY. ADDRESS MODIFIERS= 0x29 AND 0x2D. NO DMA. NO INTERRUPTS. NO.
RESET*
CLK_CONFIG
EOF
CLOCK
SYNC_GAP
TEST_MODE
FIRST_XING
L1_ACCEPT
AC TERMINATIONS CLOSE TO CPLD CLOCK PINS
R82 50
R83 50
C229 100pF
C230 100pF
LMC555 generates slow (~100Hz) clock for driving one shots that drive the front panel LEDs.
U47 LMC555CM
R80 100
R81 10k
C231 .1uF
U48 74LCX245M
VME_DATA[7..0]
VME_D0
VME_D1
VME_D2
VME_D3
VME_D4
VME_D5
VME_D6
VME_D7
RECV_VME*
DRIVE_VME*
When RECV_VME is low the slave is listening to the VME bus. When RECV_VME is high the slave is talking to the bus master. When DRIVE_VME* is high both A and B ports are HIGH />
U49
XC95288XL-10-TQ144 4
LED_[6..0]
7 user programmable front panel leds. (active low)
TOP_CONFIG[4..0]
TOP_FIFO_DEPTH[2..0]
TOP_STAT[3..0]
FREE_RUN
CLK_SEL
FORCE_RESET
BOT_STAT[3..0]
BOT_FIFO_DEPTH[2..0]
BOT_CONFIG[4..0]
STAT_DAT
TDO
FPGA SERIAL CONFIGURATION BUSSES:
BIT 0 = CCLK
BIT 1 = DIN
BIT 2 = PROG (ACTIVE LOW)
BIT 3 = DONE (ACTIVE HIGH)
BIT 4 = INIT (ACTIVE LOW, BIDIRECTIONAL OPEN DRAIN)
FIFO DEPTH SERIAL BUS:
BIT 0 = CLOCK
BIT 1 = DATA
BIT 2 = RESET
FORCE_RESET IS ACTIVE LOW AND MUST BE ASSERTED FOR ABOUT 2 SECONDS TO RESET THE ENTIRE BOARD. THIS OUTPUT SHOULD BE OPEN DRAIN. (THE PULLUP IS LOCATED NEAR THE PUSHBUTTON)
U51 LM75CIM-3
slow monitoring information transmitted over this serial bus to the hardware contained in the POWER INTERRUPTOR CARD located between the backplane and the VME processor located in slot 1 of the subrack.
U50 74LCX16244MTD
VME_A[15..0]
VME_AS*
VME_AM[5..0]
VME_WRITE*
VME_LWORD*
VME_DS0*
VME_SYSRST*
VME_DS1*
VME_SYSCLK
ADDR[15..0]
R84 330
R85 470
'245
'244
'244
'38
95288XL
backplane connector
U52 74LCX16244MTD
VME_A0
VME_A8
VME_A1
VME_A9
VME_A2
VME_A10
VME_A3
VME_A11
VME_A4
VME_A12
VME_A5
VME_A13
VME_A6
ISP programming bus
TMS
TCK
TDI
BASE_ADDR[5..0]
the base address is set by 6 pins in the backplane, which are pulled up to +3.3V or tied to GND (THROUGH RESISTORS, NOT A DIRECT CONNECTION TO +3.3V OR GROUND!)
STAT_CLK
STAT_RST
SLOW MONITORING BUS INPUTS.
TOP_REG_ERROR
BOT_REG_ERROR
THESE INPUTS ARE ASSERTED IF THE DAUGHTERCARD LINEAR REGULATORS FAIL.
R86 10k
R87 10k
R88 10k
74LCX38M U53
BERR*
DTACK*
IACK*
VME_BERR*
VME_DTACK*
VME_IACK*
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D-ZERO Upgrade Group
design by Jamieson Olsen <jamieson@fnal.gov>
Title
DIGITAL FRONT END BOARD -- VME SLAVE
Size D
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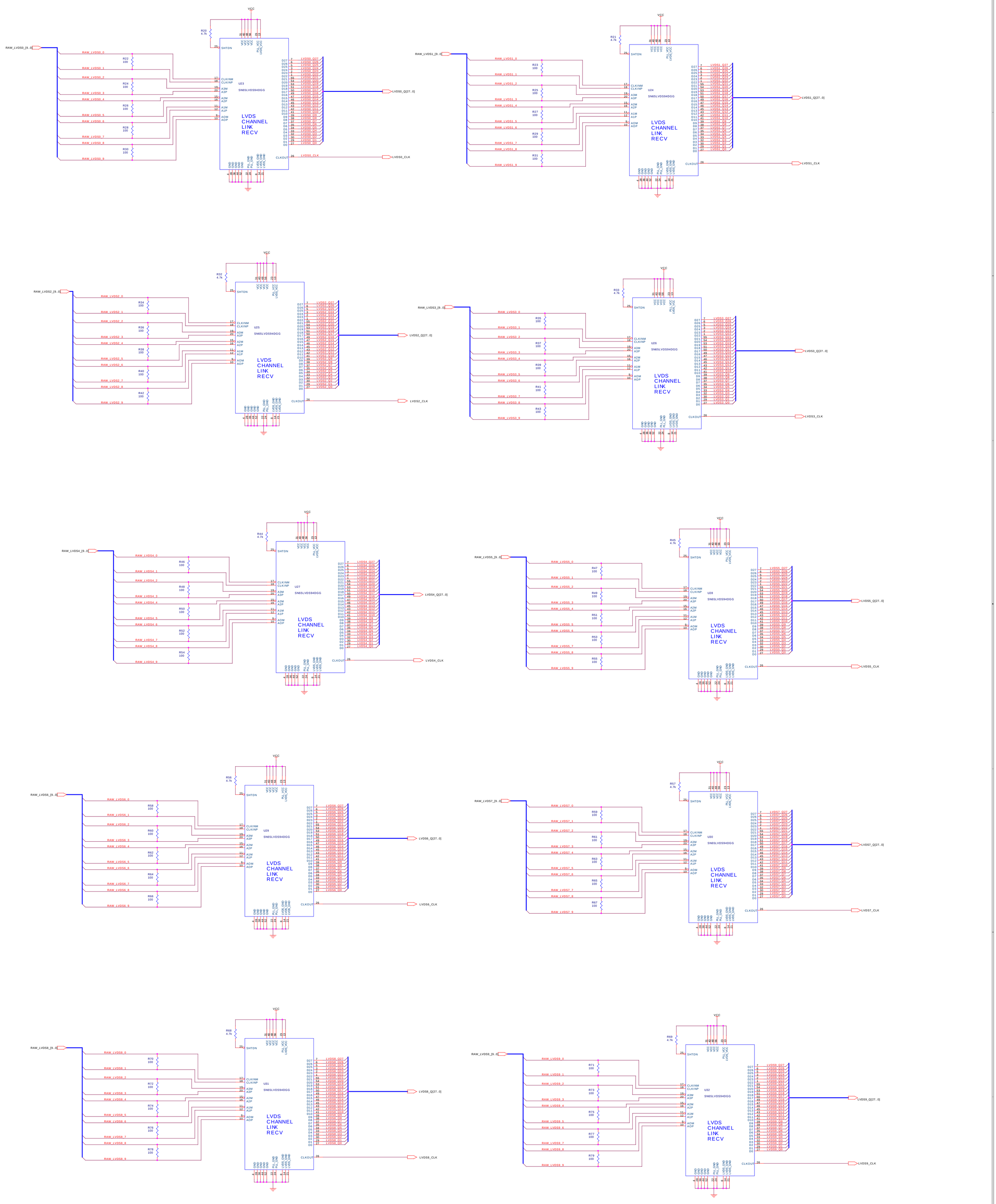

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Title: DIGITAL FRONT END BOARD / LVDS RECEIVERS

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