



Jamieson T. Olsen
Engineering Note

Date: 18 April 2000
Rev Date: 13 September 2000

Project: Collector Daughterboard
Doc. No: 2000-04-18a

Subject: PCB fabrication specifications for the Collector Daughterboard

General Board Specifications

size: 7.775" x 8.850"
revision: C
material: FR4
thickness: finished pressed thickness of 0.093" \pm 10%
copper: 1/2 oz TOP and BOTTOM; 1oz all other layers
soldermask: both sides LPI, BLACK
silkscreen: both sides, WHITE
layers: 10
finish: 3-7u" immersion Gold over 150-300 u" electroless Nickel

Thruholes

3798 total
8 unique sizes
0.013" is smallest
0.090" is largest
All holes are plated through. Refer to the drill drawing CDB_DRD.GBR for more information.
All hole dimensions are specified as finished sizes.

Stackup

Use your default 10-layer stackup. *In your quote please specify the core and pre-preg thicknesses that you intend to use.*
The layer order is as follows:

1) TOP "COMPONENT SIDE"	cdb_top.gbr
2) GROUND PLANE	cdb_gnd.gbr
3) INNER ROUTING 1	cdb_in1.gbr
4) VCC3 PLANE	cdb_vcc3.gbr
5) INNER ROUTING 2	cdb_in2.gbr
6) INNER ROUTING 3	cdb_in3.gbr
7) GROUND PLANE	cdb_gnd.gbr
8) INNER ROUTING 4	cdb_in4.gbr
9) VCC2 PLANE	cdb_vcc2.gbr
10) BOTTOM "SOLDER SIDE"	cdb_bot.gbr

Photoplots

The vendor must send to-scale photoplots of the above layers to Fermilab for approval prior to fabrication.

Board Finish

3-7 u" Immersion or Flash Gold over 150-300 u" electroless Nickel. Both sides.

Colors

Soldermask should be BLACK. Silkscreen legend should be WHITE.

Testing

All boards shall be fully electrically tested using a flying head probe (preferred) or bed of nails. Boards that pass the electrical test should be identified with a paint mark.

If possible, please send known bad boards to Fermilab along with the good boards.

Files

TOP routing layer	cdb_top.gbr
GROUND plane	cdb_gnd.gbr
inner routing layer 1	cdb_in1.gbr
inner routing layer 2	cdb_in2.gbr
inner routing layer 3	cdb_in3.gbr
inner routing layer 4	cdb_in4.gbr
VCC3 power plane	cdb_vcc3.gbr
VCC2 power plane	cdb_vcc2.gbr
BOTTOM routing layer	cdb_bot.gbr
soldermask top	cdb_smt.gbr
soldermask bottom	cdb_smb.gbr
silkscreen top	cdb_sst.gbr
silkscreen bottom	cdb_ssb.gbr
solder paste top	cdb_spt.gbr
solder paste bottom	cdb_spb.gbr
drill tape	thruhole.tap
drill drawing	cdb_drd.gbr
assembly drawing top	cdb_ast.gbr
assembly drawing bottom	cdb_asb.gbr

Contact Information

Jamieson Olsen
Fermilab
PO BOX 500 / MS352
Batavia, IL 60510-0500
630.840.2779 (voice)
630.840.8886 (fax)
jamieson@fnal.gov