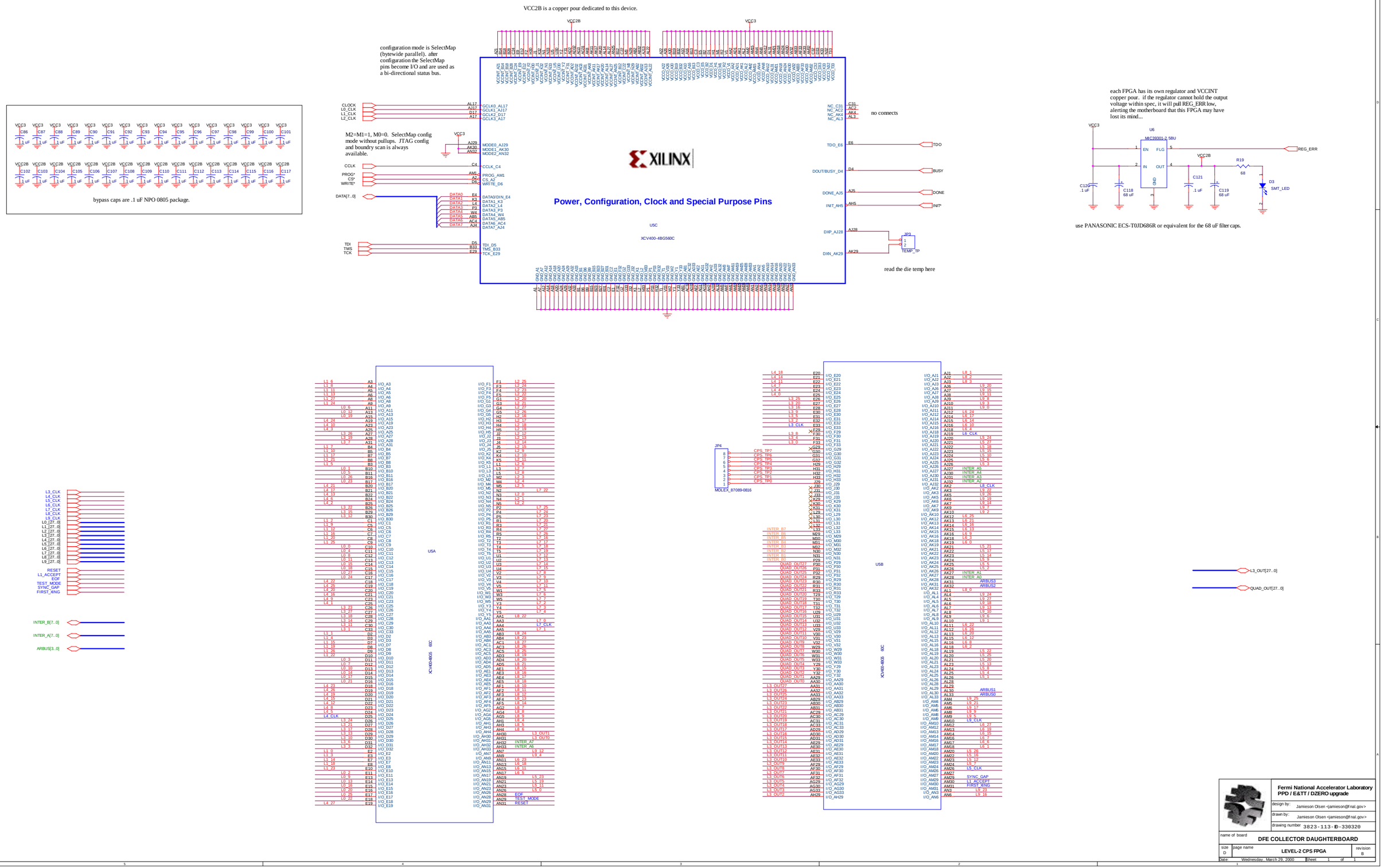
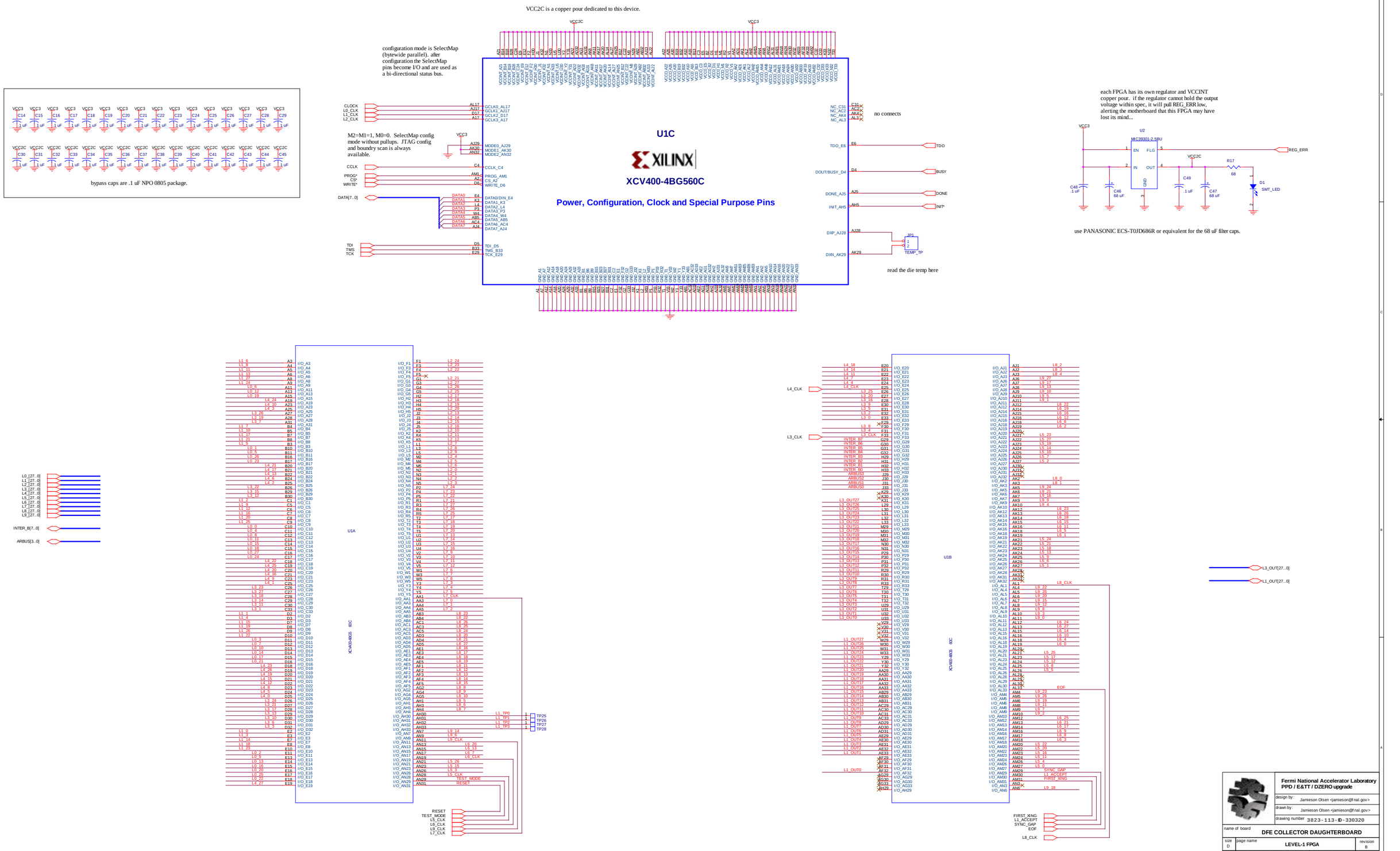
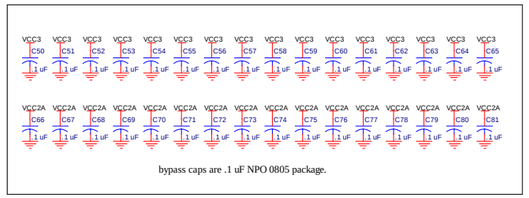

VCC2B is a copper pour dedicated to this device.
VCC2B
VCC3
configuration mode is SelectMap (bytewide parallel). after configuration the SelectMap pins become I/O and are used as a bi-directional status bus.
CLOCK
L0_CLK
L1_CLK
L2_CLK
GCLK0_AL17
GCLK1_AJ17
GCLK2_D17
GCLK3_A17
M2=M1=1, M0=0. SelectMap config mode without pullups. JTAG config and boundry scan is always available.
MODE0_AJ29
MODE1_AK30
MODE2_AN32
CCLK
PROG*
CS*
WRITE*
CCLK_C4
PROG_AM1
CS_A2
WRITE_D6
DATA[7..0]
DATA0/DIN_E4
DATA1_K3
DATA2_L4
DATA3_P3
DATA4_W4
DATA5_AB5
DATA6_AC4
DATA7_AJ4
TDI
TMS
TCK
TDI_D5
TMS_B33
TCK_E29
XILINX
Power, Configuration, Clock and Special Purpose Pins
U5C
XCV400-4BG560C
NC_C31
NC_AC2
NC_AK4
NC_AL3
no connects
TDO_E6
TDO
DOUT/BUSY_D4
BUSY
DONE_AJ5
DONE
INIT_AH5
INIT*
DXP_AJ28
DXN_AK29
JP3
TEMP_TP
read the die temp here
VCC3
C86 C87 C88 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99 C100 C101
C102 C103 C104 C105 C106 C107 C108 C109 C110 C111 C112 C113 C114 C115 C116 C117
.1 uF
bypass caps are .1 uF NPO 0805 package.
each FPGA has its own regulator and VCCINT copper pour. if the regulator cannot hold the output voltage within spec, it will pull REG_ERR low, alerting the motherboard that this FPGA may have lost its mind...
U6
MIC39301-2.5BU
EN
FLG
IN
OUT
GND
REG_ERR
VCC2B
R19
68
C120
.1 uF
C118
68 uF
C121
.1 uF
C119
68 uF
D3
SMT_LED
use PANASONIC ECS-T0JD686R or equivalent for the 68 uF filter caps.
USA
XCV400-4BG560C
USB
XCV400-4BG560C
JP4
MOLEX_87089-0816
CPS_TP7
CPS_TP6
CPS_TP5
CPS_TP4
CPS_TP3
CPS_TP2
CPS_TP1
CPS_TP0
L3_CLK
L4_CLK
L5_CLK
L6_CLK
L7_CLK
L8_CLK
L9_CLK
L0_[27..0]
L1_[27..0]
L2_[27..0]
L3_[27..0]
L4_[27..0]
L5_[27..0]
L6_[27..0]
L7_[27..0]
L8_[27..0]
L9_[27..0]
RESET
L1_ACCEPT
EOF
TEST_MODE
SYNC_GAP
FIRST_XNG
INTER_B[7..0]
INTER_A[7..0]
ARBUS[3..0]
L3_OUT[27..0]
QUAD_OUT[27..0]
Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade
design by: Jamieson Olsen <jamieson@fnal.gov>
drawn by: Jamieson Olsen <jamieson@fnal.gov>
drawing number 3823-113-ID-330320
name of board DFE COLLECTOR DAUGHTERBOARD
size D
page name LEVEL-2 CPS FPGA
revision B
Date: Wednesday, March 29, 2000
Sheet 1 of 1

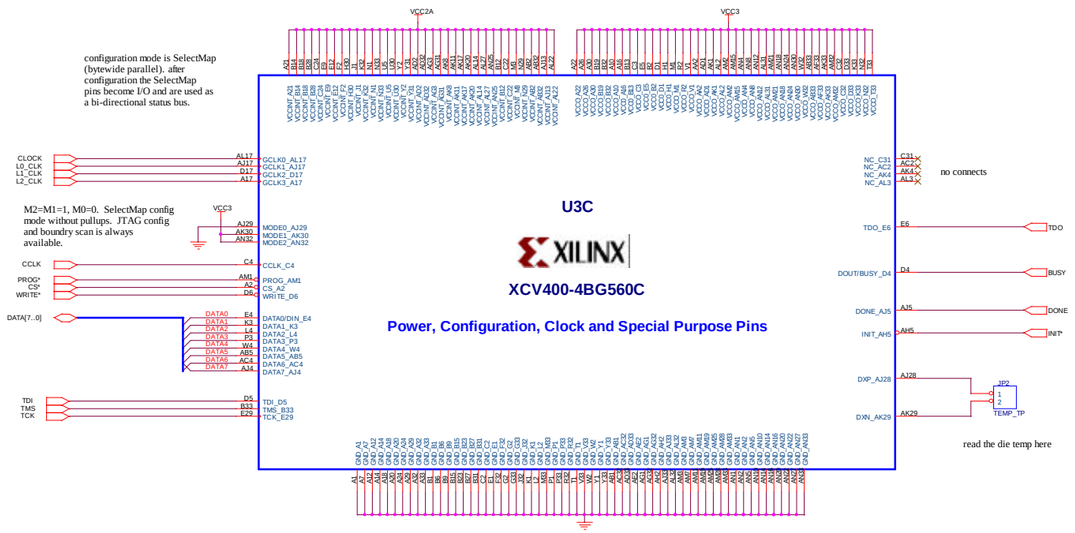

VCC2C is a copper pour dedicated to this device.
VCC2C
VCC3
configuration mode is SelectMap (bytewide parallel). after configuration the SelectMap pins become I/O and are used as a bi-directional status bus.
bypass caps are .1 uF NPO 0805 package.
M2=M1=1, M0=0. SelectMap config mode without pullups. JTAG config and boundry scan is always available.
U1C
XILINX
XCV400-4BG560C
Power, Configuration, Clock and Special Purpose Pins
CLOCK
L0_CLK
L1_CLK
L2_CLK
CCLK
PROG*
CS*
WRITE*
DATA[7..0]
TDI
TMS
TCK
GCLK0_AL17
GCLK1_A17
GCLK2_D17
GCLK3_A17
MODE0_AJ29
MODE1_AK30
MODE2_AN32
CCLK_C4
PROG_AM1
CS_A2
WRITE_D6
DATA0/DIN_E4
DATA1_K3
DATA2_L4
DATA3_P3
DATA4_W4
DATA5_AB5
DATA6_AC4
DATA7_AJ4
TDI_D5
TMS_B33
TCK_E29
NC_C31
NC_AC2
NC_AK4
NC_AL3
no connects
TDO_E6
TDO
DOUT/BUSY_D4
BUSY
DONE_AJ5
DONE
INIT_AH5
INIT*
DXP_AJ28
DXN_AK29
JP1
TEMP_TP
read the die temp here
each FPGA has its own regulator and VCCINT copper pour. if the regulator cannot hold the output voltage within spec, it will pull REG_ERR low, alerting the motherboard that this FPGA may have lost its mind...
U2
MIC39301-2.5BU
EN
FLG
IN
OUT
GND
REG_ERR
R17
68
D1
SMT_LED
C48
.1 uF
C46
68 uF
C49
.1 uF
C47
68 uF
use PANASONIC ECS-T0JD686R or equivalent for the 68 uF filter caps.
U1A
XCV400-4BG560C
U1B
XCV400-4BG560C
L4_CLK
L3_CLK
L0_[27..0]
L1_[27..0]
L2_[27..0]
L3_[27..0]
L4_[27..0]
L5_[27..0]
L6_[27..0]
L7_[27..0]
L8_[27..0]
L9_[27..0]
INTER_B[7..0]
ARBUS[3..0]
L3_OUT[27..0]
L1_OUT[27..0]
L1_TP0
L1_TP1
L1_TP2
L1_TP3
TP25
TP26
TP27
TP28
RESET
TEST_MODE
L5_CLK
L6_CLK
L9_CLK
L7_CLK
FIRST_XING
L1_ACCEPT
SYNC_GAP
EOF
L8_CLK
Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade
design by: Jamieson Olsen <jamieson@fnal.gov>
drawn by: Jamieson Olsen <jamieson@fnal.gov>
drawing number 3823-113-ID-330320
name of board DFE COLLECTOR DAUGHTERBOARD
size D
page name LEVEL-1 FPGA
revision B
Date: Wednesday, March 29, 2000
Sheet 1 of 1



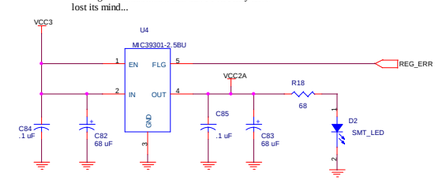
VCC2A is a copper pour dedicated to this device.

configuration mode is SelectMap (bytewide parallel). after configuration the SelectMap pins become I/O and are used as a bi-directional status bus.

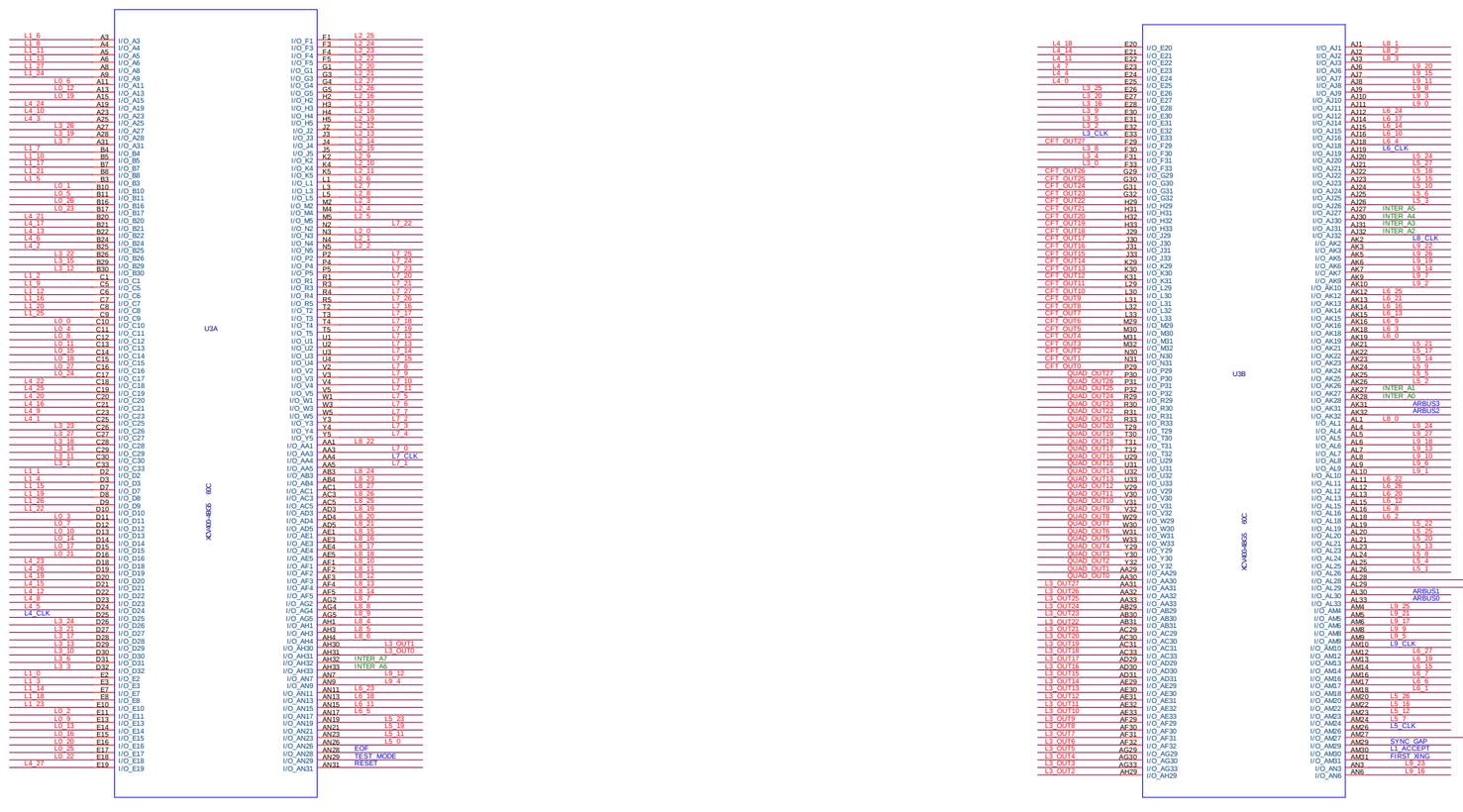
M2=M1=1, M0=0. SelectMap config mode without pullups. JTAG config and boundry scan is always available.



each FPGA has its own regulator and VCCINT copper pour. if the regulator cannot hold the output voltage within spec, it will pull REG_ERR low, alerting the motherboard that this FPGA may have lost its mind...



use PANASONIC ECS-T0JD686R or equivalent for the 68 uF filter caps.



Fermi National Accelerator Laboratory PPD / E&TT / DZERO upgrade	
design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-113-ID-330320
name of board	DFE COLLECTOR DAUGHTERBOARD
size D / page name	LEVEL-2 CFT FPGA / revision B
Date:	Wednesday, March 29, 2000 / Sheet 1 of 1

DFE COLLECTOR DAUGHTERBOARD

COLLECTOR DAUGHTERBOARD REVISON HISTORY:		
REV	DATE	CHANGES
A	04 NOV 1999	Original drawing.
B	29 MAR 2000	Switch OUT_A[27..0] and OUT_B[27..0] to insure proper connectivity to G-LINK and LVDS drivers based on Manuel Martin's D0 Note XXXX.

CONTROL SIGNALS:

EOF = end of frame marker, sync to CLOCK

CLOCK = 53.104MHz constant

RESET = active LOW reset from motherboard

L1_ACCEPT = framework now wants L2 data

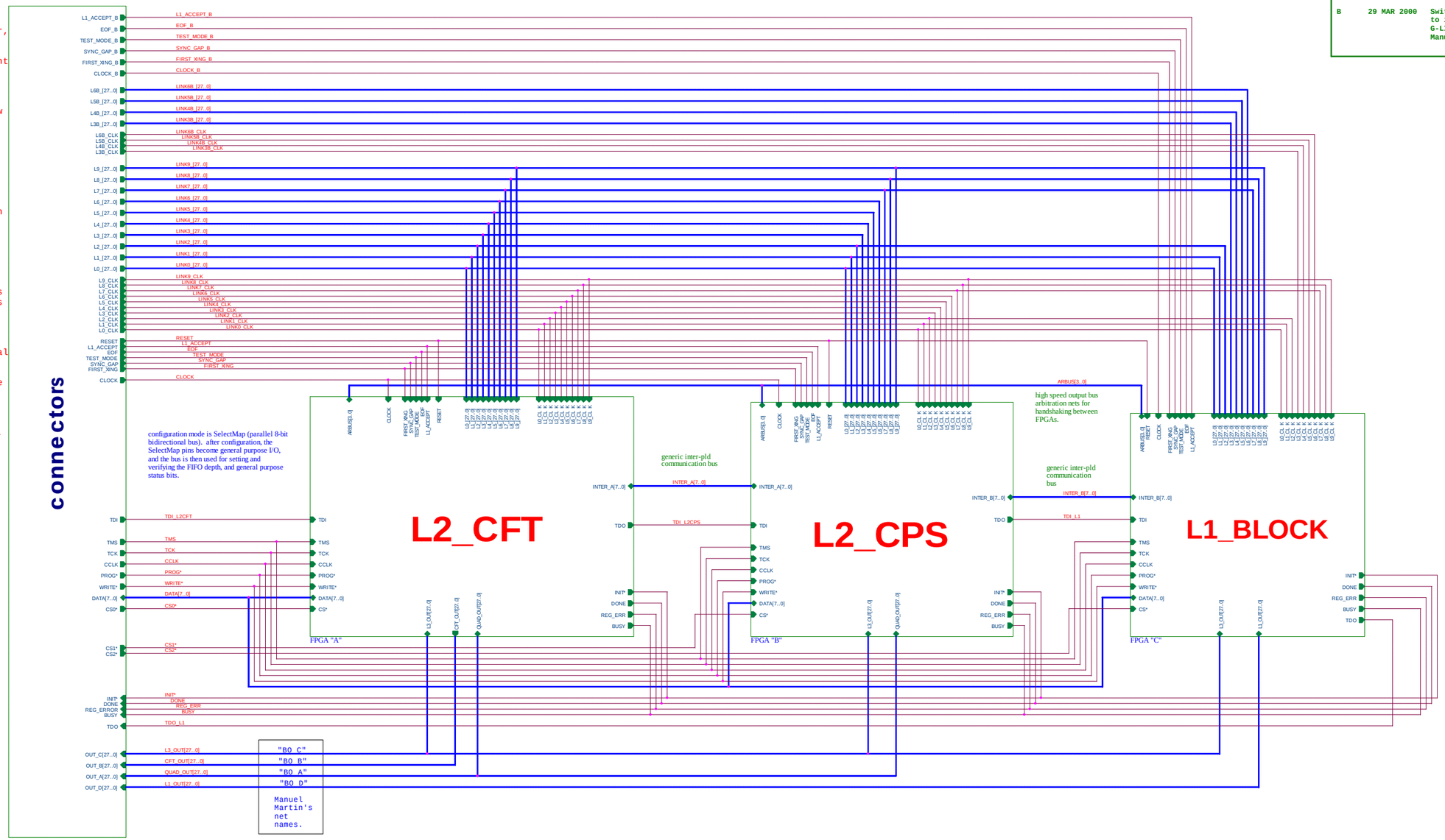
TEST_MODE = upstream module is sending test pattern data

SYNC_GAP = currently in beam sync gap, watch for test patterns and diagnostic data coming in

FIRST_XING = this is the first crossing after a beam gap -- reset the crossing counters.

NOTE: the control signals ending in "_B" are copies of the regular control signals brought in from the motherboard.

NOTE: these control signal names were defined by requirements for the DFE CFT/CPS AXIAL setup. The functions of these lines may change slightly to accomedate the requirements for this particular daughterboard.



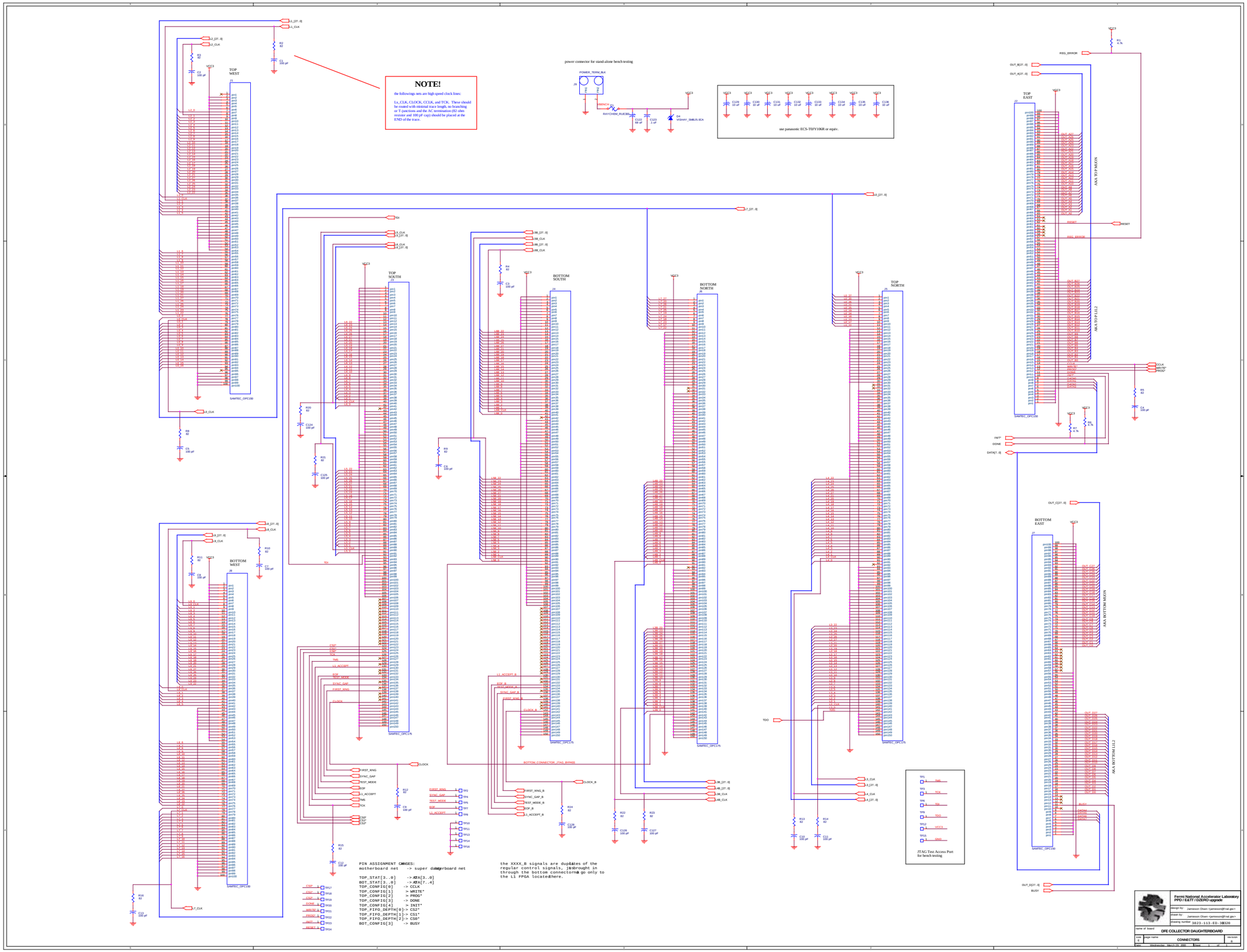
OUTPUT BUSSES ARE DEFINED AS FOLLOWS:

OUT_B = TOP L1L2 = 2 LVDS
OUT_A = TOP MUON = LVDS and G-LINK
OUT_D = BOT L1L2 = 2 LVDS
OUT_C = BOT MUON = LVDS and G-LINK

THIS IS USING "TRANSITION MODULE 1.0" DESIGNED BY P. SHEAHAN.

Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-113-ID-330320
name of board	DFE COLLECTOR DAUGHTERBOARD
size D	page name TOP LEVEL	revision B
Date: Wednesday, March 29, 2000	Sheet 1 of 1


NOTE!
the followings nets are high speed clock lines:
Lx_CLK, CLOCK, CCLK, and TCK. These should be routed with minimal trace length, no branching or T-junctions and the AC termination (82 ohm resistor and 100 pF cap) should be placed at the END of the trace.
power connector for stand-alone bench testing
use panasonic ECS-T0JY106R or equiv.
TOP WEST
BOTTOM WEST
TOP SOUTH
BOTTOM SOUTH
BOTTOM NORTH
TOP NORTH
TOP EAST
BOTTOM EAST
AKA TOP MUON
AKA TOP LL2
AKA BOTTOM MUON
AKA BOTTOM LL2
JTAG Test Access Port for bench testing
PIN ASSIGNMENT CHANGES:
motherboard net -> super daughterboard net
TOP_STAT[3..0] -> ATA[3..0]
BOT_STAT[3..0] -> ATA[7..4]
TOP_CONFIG[0] -> CCLK
TOP_CONFIG[1] -> WRITE*
TOP_CONFIG[2] -> PROG*
TOP_CONFIG[3] -> DONE
TOP_CONFIG[4] -> INIT*
TOP_FIFO_DEPTH[0]-> CS2*
TOP_FIFO_DEPTH[1]-> CS1*
TOP_FIFO_DEPTH[2]-> CS0*
BOT_CONFIG[3] -> BUSY
the XXXX_B signals are duplicates of the regular control signals, just brought in through the bottom connectors to go only to the L1 FPGA located here.
Fermi National Accelerator Laboratory
PPD / ELETT / D0ZERO upgrade
design by: Jamieson Olsen
drawn by: Jamieson Olsen
drawing number: 3823-113-ED-3B320
name of board
DFE COLLECTOR DAUGHTERBOARD
page name
CONNECTORS
revision
B
Date: Wednesday, March 29, 2006
Sheet 1 of 1