

Luminosity Monitor L3 Data Format

Version 1.2

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This document defines the format of the data sent by the Luminosity Monitor (LM) to the L3/DAQ.

Block Structure

The LM data is contained in a series of blocks. There are four different types of blocks: VBD Header, Crate Header, Module, and VBD Trailer. They are readout as illustrated below:

VBD Header
Crate Header
First Module Block
Second Module Block
...
Last Module Block
VBD Trailer

The sections below describe the content of these four block types.

VBD Header

A VBD header is attached by the DAQ. It has the same format for all crates:

Total Word Count	
Event Number	Crate ID
Reserved	

Total Word Count: Total number of words transferred for this crate, including the VBD header and trailer.

Event Number: Level 3 Transfer Number assigned by the DAQ system, stored in the upper 16 bits of the 2nd VBD header word.

Crate ID: Crate ID Number (0x11 for LM crate, 0x12 for the FPD Timing crate).

Crate Header

The first block readout by the DAQ is the Crate Header. It has the following format:

Crate Header Word Count	
Crate ID	Crate Status
Number of Modules Read	

Crate Header Word Count: Number of long words in the header not counting the word count (2).

Crate ID: The Crate ID is stored in the upper 16 bits of the second word in the crate header. It is set to 0x11 for the LM crate and 0x12 for the FPD Timing crate.

Crate Status: The Crate Status is stored in the lower 16 bits of the second word in the crate header. A value of 0xa indicates no errors, while a value of 0xe indicates the presence of an error condition.

Number of Modules Read: Depends on readout configuration. For the LM crate, this quantity will vary between 0-7, with full detector readout having 6 TDC modules and 1

VTX module. For the FPD Timing crate, this quantity will vary between 0 and 4, with full detector readout having 3 TDC modules and 1 VTX module.

Module Block

Each module block has a module header followed by the data from the module as illustrated below:

Module Header
Module Data

The LM employs two types of modules: TDC and VTX. The FPD Timing readout also uses the same modules, and will initially have the same data format. The FPD data format could potentially change in the future if the FPD group needs to customize the TDC and/or VTX firmware. The format of the module header and the TDC and VTX module data are described below.

Module Header

The module header has the same format for all data blocks:

0	Module Word Count
Version	Module ID
Crossing Number	Turn
Status 1	Status 2

Module Word Count: Number of long words that follow in the module block (15 for TDC modules, 11 for VTX modules).

Version: The module version number is stored in the upper 16 bits of the 2nd module header word. The TDC and VTX modules described by this document have a module version number of 0.

Module ID: The module ID is stored in the lower 16 bits of the 2nd module header word. The module ID identifies which module is being readout. For the LM system, the VTX board has module ID 0 and the TDC boards have module ID 1-6. The mapping of counters to modules is defined below.

Crossing Number: The crossing number is stored in the upper 16 bits of the 3rd module header word. The crossing number ranges from 1 – 159 and specifies which beam crossing (or tick) the data is from. The crossing number calculated on the TDC and VTX boards is compared with the crossing number supplied by the Trigger Framework, and an error is set if they do not match.

Turn: The turn number is stored in the lower 16 bits of the 3rd module header word. The turn number is reset by an SCL init and incremented by 1 on each occurrence of crossing number 1.

Status 1: The status 1 register is stored in the upper 16 bits of the 4th module header word. The following bits are currently defined:

Bit 2: Set if the L2 buffer is full

Bit 3: Set if the L1 crossing number differs from the local crossing number

Bit 4: Set if the readout buffer is full

Bit 5: Set if the L2 crossing number differs from the local crossing number

All other bits are reserved for future use.

Status 2: The status 2 register is stored in the lower 16 bits of the 4th module header word. This word is reserved for future use.

TDC Module Data

The TDC module data is contained in 12 long words as follows:

TC1	TC0
TC3	TC2
TC5	TC4
TC7	TC6
T0	Q0
T1	Q1
T2	Q2
T3	Q3
T4	Q4
T5	Q5
T6	Q6
T7	Q7

TCn: Corrected time for channel n.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Corrected Time							

The corrected time provides the measured time for this channel, including charge slewing corrections. It has a 50 ps lsb and is calibrated so that an interaction taking place at z=0 will have an average corrected time of 0x80. The corrected time is obtained by summing

the time measurement in bits 0-11 of Tn and the charge slewing correction in bits 0-6 of Qn. If a valid time measurement has been made, the lowest 8 bits of this sum are the corrected time. For a time measurement to be valid, the valid time (bit 12 of Tn) must be set, the slewing correction must be non-zero, and the corrected time must lie within programmable limits. Valid corrected times range from 0x01-0xff, with a corrected time of 0x00 indicating there was not a valid time measurement for the counter. The corrected times are stored in the lower 8-bits of the indicated 16-bit word; the upper 8 bits are reserved for future use as shown below:

Tn: Time measurement for channel n.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			Vld	TDC Time Measurement											

The TDC time measurement is contained in bits 0-11 of Tn, the valid time flag is in bit 12, and bits 13-15 are reserved for future use. The TDC time measurement is calibrated to have a 50 ps lsb and an average time of 0x880 for hits where the slewing correction is 0 and the interaction takes place at z=0.

Qn: Charge measurement and slewing correction for channel n.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Q Range		Q Data						Slewing Correction							

The charge slewing correction to the time measurement is contained in bits 0-6 of Qn, with a 50 ps lsb. A slewing correction of 0 indicates an invalid charge measurement. The charge measurement is stored using four different ranges:

Q Range Bits	Used When	Q Data Contents	Q Data lsb
0	$0 \leq Q(\text{pC}) < 12.8$	Q	0.1 pC
1	$12.8 \leq Q(\text{pC}) < 38.4$	Q-12.8 pC	0.2 pC
2	$38.4 \leq Q(\text{pC}) < 89.6$	Q-38.4 pC	0.4 pC
3	$89.6 \leq Q(\text{pC}) < 192$	Q-89.6 pC	0.8 pC
3	$192 \leq Q(\text{pC})$	0x1ff	-

The above table can also be represented by the following formula:

$$Q(\text{pC}) = 0.1 \times \left[(128 + Q \text{ Data}) \times 2^{(Q \text{ Range})} - 128 \right].$$

VTX Module Data

The VTX module data is contained in 8 long words as follows:

T_L2N	T_H3N	T_H2N	T_H1N
SUMN		NHITN	T_L1N
T_L2S	T_H3S	T_H2S	T_H1S
SUMS		NHITS	T_L1S
MI_FLAG		TDIFN	TDIFS
AVERAGEN			
AVERAGES			
ZVTX		TFW_ANDOR	

Word 1:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
T_L2N								T_H3N							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_H2N								T_H1N							

Word 2:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	SUMN												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	NHITN					T_L1N							

Word 3:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
T_L2S								T_H3S							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_H2S								T_H1S							

Word 4:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
0	0	0	SUMS													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	NHITS					T_L1S								

Word 5:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											MI_FLAG				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDIFN								TDIFS							

Word 6:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								AVERAGEN							

Word 7:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								AVERAGES							

Word 8:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	ZVTX								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFW_ANDOR															

T_H1N(S), T_H2N(S), T_H3N(S): The largest, 2nd largest, and 3rd largest corrected time for the north (south) LM counters, respectively.

T_L1N(S), T_L2N(S): The smallest and 2nd smallest corrected times for the north (south) LM counters, respectively.

NHITN(S): The number of valid hits in the north (south) LM counters. A valid hit is one that has a non-zero corrected time. NHITN(S) ranges from 0-24.

SUMN(S): The sum of the corrected times for the north (south) LM counters. SUMN(S) can range from 0-0x17e8.

TDIFN(S): The spread in arrival times for the north (south) LM counters used in the multiple interaction determination. The VTX board can be programmed to throw away the latest, 2nd latest, and/or earliest times in determining the spread in arrival times. For example, using the 2nd latest and earliest times to determine the north time difference would lead to $TDIFN=T_H3N-T_L1N$.

MI_FLAG: The multiple interaction flags indicate the likelihood that the beam crossing has a single/multiple interaction. The four multiple interaction flags are stored in bits 16-19 of the 5th data word, with MIFLAG[0] (bit 16) indicating a single interaction is likely, MIFLAG[1] (bit 17) indicating a single interaction is favored, MIFLAG[2] (bit 18) indicating a multiple interaction is favored, and MIFLAG[3] (bit 19) indicating a multiple interaction is likely.

AVERAGEN(S): Average value of the valid corrected times for the north (south) LM counters. For example, $AVERAGEN=SUMN/NHITN$. AVERAGEN(S) has a 50 ps lsb.

ZVTX: Interaction vertex position measured by the LM counters. The vertex position is obtained by calculating $ZVTX=AVERAGEN-AVERAGES$. The vertex position has a 0.75 cm lsb.

TFW_ANDOR: Trigger Framework and-or input bits provided by the VTX board. For the LM VTX board, the trigger framework bits are defined as follows:

bit 0: Valid hits in both north and south LM counters

bit 1: Valid hit in the south LM counters and no valid hits in the north LM counters

bit 2: Valid hit in the north LM counters and no valid hits in the south LM counters

bit 3: No valid hits in the LM counters

bit 4: Anti-proton halo detected using loose time cuts

bit 5: Anti-proton halo detected using tight time cuts

bit 6: Proton halo detected using loose time cuts

bit 7: Proton halo detected using tight time cuts

bit 8: MIFLAG[0]

bit 9: MIFLAG[1]

bit 10: MIFLAG[2]

bit 11: MIFLAG[3]

bit 12: Valid hits in north and south counters and $|ZVTX|<ZCUT0$ (programmable)

bit 13: Valid hits in north and south counters and $|ZVTX|<ZCUT1$ (programmable)

bit 14: Valid hits in north and south counters and $|ZVTX|<ZCUT2$ (programmable)

bit 15: Valid hits in north and south counters and $|ZVTX|<ZCUT3$ (programmable)

Luminosity Monitor Channel Map

Module ID	Channel No.	LM Counter No.	LM Counter Label
1	0	1	NW1
1	1	2	NW2
1	2	3	NW3
1	3	4	NW4
1	4	5	NW5
1	5	6	NW6
1	6	7	NW7
1	7	8	NW8
2	0	9	NW9
2	1	10	NW10
2	2	11	NW11
2	3	12	NW12
2	4	13	NE1
2	5	14	NE2
2	6	15	NE3
2	7	16	NE4
3	0	17	NE5
3	1	18	NE6
3	2	19	NE7
3	3	20	NE8
3	4	21	NE9
3	5	22	NE10
3	6	23	NE11
3	7	24	NE12
4	0	25	SW1
4	1	26	SW2
4	2	27	SW3
4	3	28	SW4
4	4	29	SW5
4	5	30	SW6
4	6	31	SW7
4	7	32	SW8
5	0	33	SW9
5	1	34	SW10
5	2	35	SW11
5	3	36	SW12
5	4	37	SE1
5	5	38	SE2
5	6	39	SE3
5	7	40	SE4
6	0	41	SE5
6	1	42	SE6
6	2	43	SE7
6	3	44	SE8
6	4	45	SE9
6	5	46	SE10
6	6	47	SE11
6	7	48	SE12

VBD Trailer

A VBD trailer is attached by the DAQ. It has the same format for all crates:

Total Word Count	
Event Number	Crate ID
Reserved	
DAQ Token	
Checksum	

Total Word Count: Total number of words transferred for this crate, including the VBD header and trailer.

Event Number: Level 3 Transfer Number assigned by the DAQ system, stored in the upper 16 bits of the 2nd VBD header word.

Crate ID: Crate ID Number (0x11 for LM crate, 0x12 for the FPD Timing crate).

DAQ Token: Token that enabled readout of this crate.

Checksum: Checksum of all words transferred for this crate, excluding the checksum.