



The DØ Run IIb L1Cal (past, present & future)

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Why Give This Talk?

1. **Introduce/Attract New Participants**
2. **Review Where We Are**
3. **Remember Constraints: Cost & Schedule**
4. **Start Discussion on Where We're Going**



Outline

1. Overview & Review

- ◆ Physics Goals
- ◆ System Architecture
- ◆ The Current Team

2. Current Status

- ◆ Boards in the System
- ◆ Prototype Integration Test

3. Where Do We Stand

- ◆ Cost & Schedule
- ◆ Where We Need Help

4. Getting to the End

- ◆ What Should We Do (start of discussion)

(5. Handy Glossary of Acronyms)



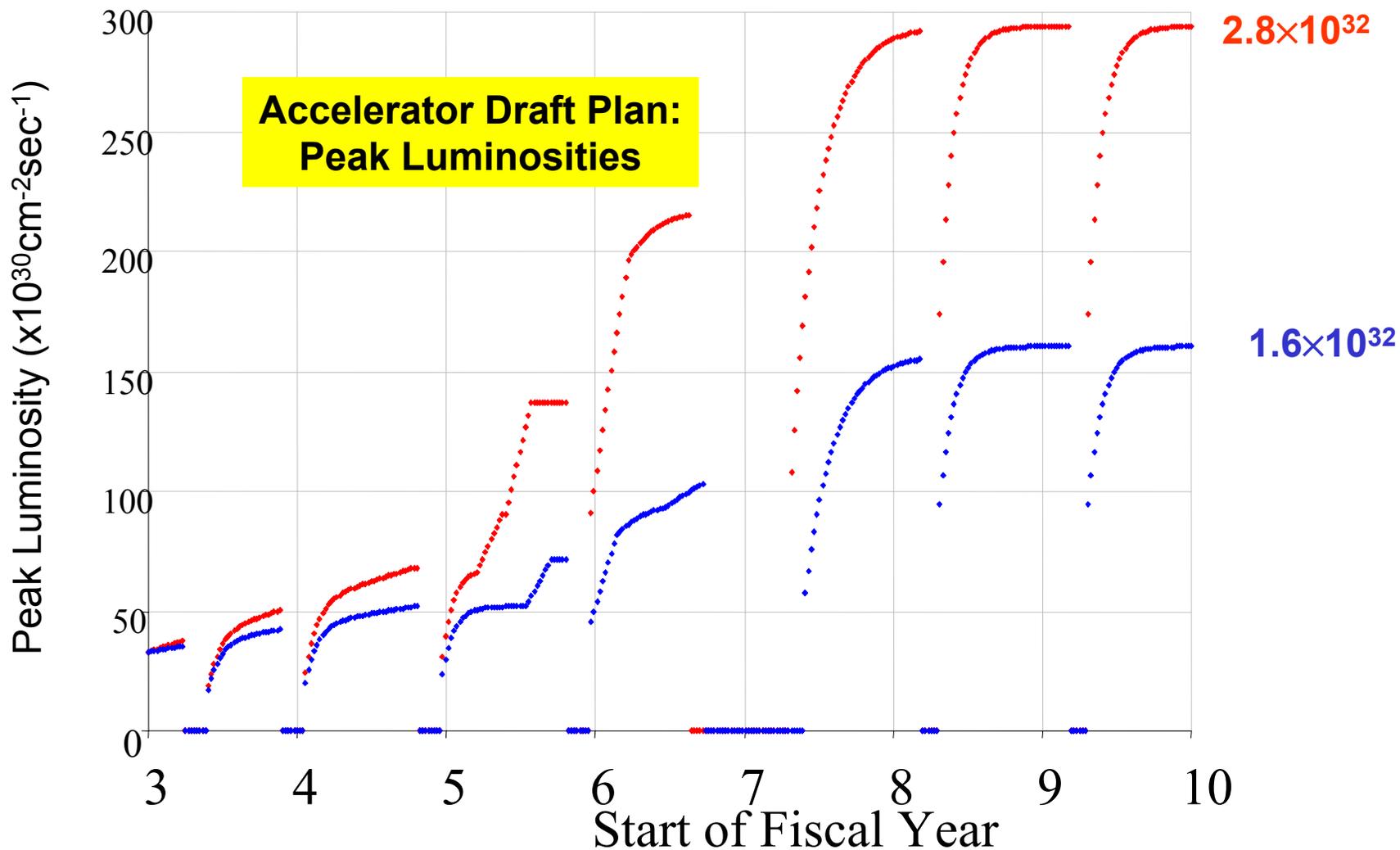
L1Cal is Key (Higgs or No)

L1 Calorimeter Trigger is the primary mechanism for collecting: e/γ , Jets, Invisible Particles (ME_T)

Physics	Sample Channels	Cal Triggers
Electro-Weak	$W \rightarrow l\nu / Z \rightarrow l^+l^-$	EM, ME_T
Top	$t\bar{t} \rightarrow l\nu + \text{jets, all jets}$ $Z \rightarrow b\bar{b}$	EM, Jet (calibrate E-scale)
B Physics	B_s Mixing (hadronic)	EM, Cal-Track
New Phenomena	$\tilde{\chi}_1^\pm \tilde{\chi}_2^0 \rightarrow \tilde{\chi}_1^0 l\nu \tilde{\chi}_1^0 l^+l^-$ $\tilde{t}_1 \rightarrow bW^+ \tilde{\chi}_1^0, G_{KK} \rightarrow \gamma\gamma$	EM, Jet, ME_T
Higgs	$W/ZH \rightarrow l\nu / \nu\nu b\bar{b}$ $H \rightarrow W^{(*)}W$	EM, Jet, ME_T



What Can We Expect





But Rate is a Problem

Trigger	Run IIa Definition	Example Channel	L1 Rate [kHz] (no upgrade)	L1 Rate [kHz] (w/ upgrade)
EM	1 EM TT > 10 GeV	W→eν WH→evjj	1.3	0.7
DiEM	1 EM TT > 7 GeV 2 EM TT > 5 GeV	Z→ee ZH→eejj	0.5	0.1
Muon	1 Mu Pt > 11 GeV CFT Track	W→μν WH→μνjj	6	1.1
Di-Mu	2 Mu Pt > 3 GeV CFT Tracks	Z/ψ→μμ ZH→μμjj	0.4	<0.1
e + Jets	1 EM TT > 7 GeV 2 Had TT > 5 GeV	WH→evjj tt→ev+jets	0.8	0.2
Mu + Jet	1 Mu Pt > 3 GeV 1 Had TT > 5 GeV	WH→μνjj tt→μν+jets	<0.1	<0.1
Jet+MEt	2 TT > 5 GeV MEt > 10 GeV	ZH→vvbb	2.1	0.8
Mu+EM	1 Mu Pt > 3 GeV + Trk 1 EM TT > 5 GeV	H→WW,ZZ	<0.1	<0.1
Iso Trk	1 Iso Trk Pt > 10 GeV	H→ττ, W→μν	17	1.0
Di-Trk	1 Iso Trk Pt > 10 GeV 2 Trk Pt > 5 GeV 1 Trk matched w/ EM	H→ττ	0.6	<0.1
Total Rate			~30	3.9
Cal Rate			4.7	1.8

Luminosity

$$2 \times 10^{32}$$

BC

396 ns

L1 Limit

~3 kHz

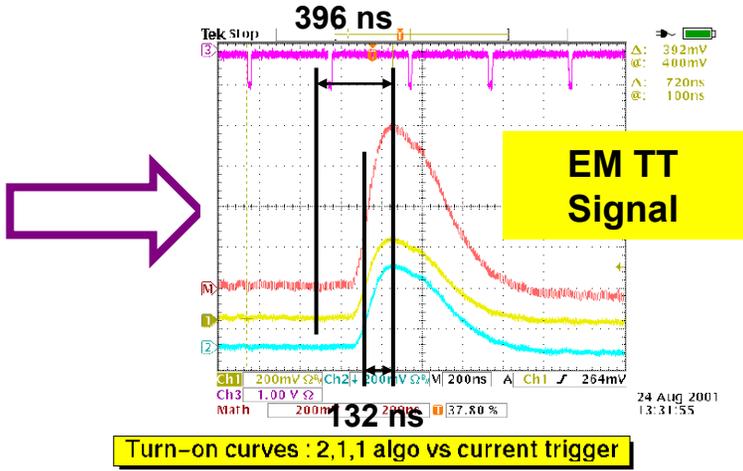


Run IIa Limitations

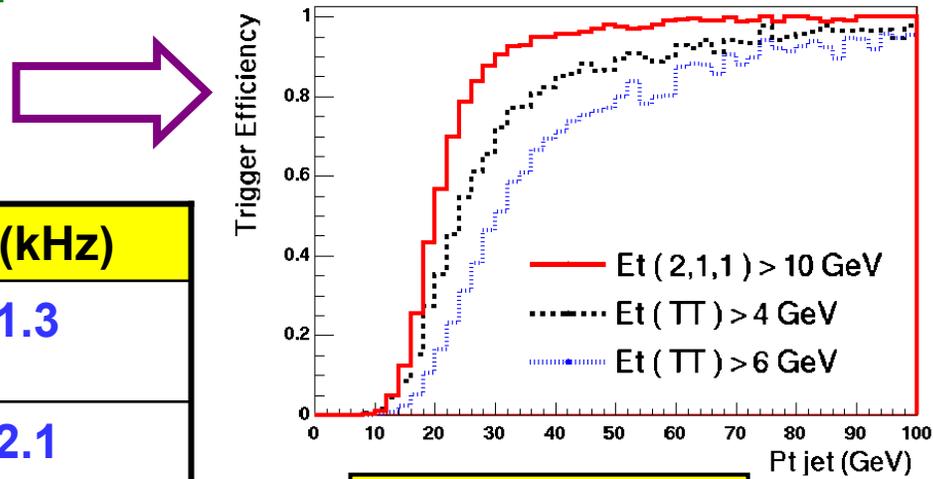
- Signal rise > 132 ns
 - cross thrsh before peak
⇒ trigger on wrong x'ing
 - affects high-Et events
 - prevents 132 ns running

- Poor Et-res. (Jet,EM,MEt)

- slow turn-on curves
 - 5 Gev TT thresh ⇒ 80% eff. for 40 GeV jets
- low thresholds ⇒ unacceptable rates at $L = 2 \times 10^{32}$



Trigger	Phys. Chan	Rate (kHz)
EM Trigger 1 TT > 10 GeV	$W \rightarrow ev$	1.3
Jet Trigger 2 TT > 5 GeV + MEt > 10 GeV	$ZH \rightarrow vvbb$	2.1 ($L = 2e32$)

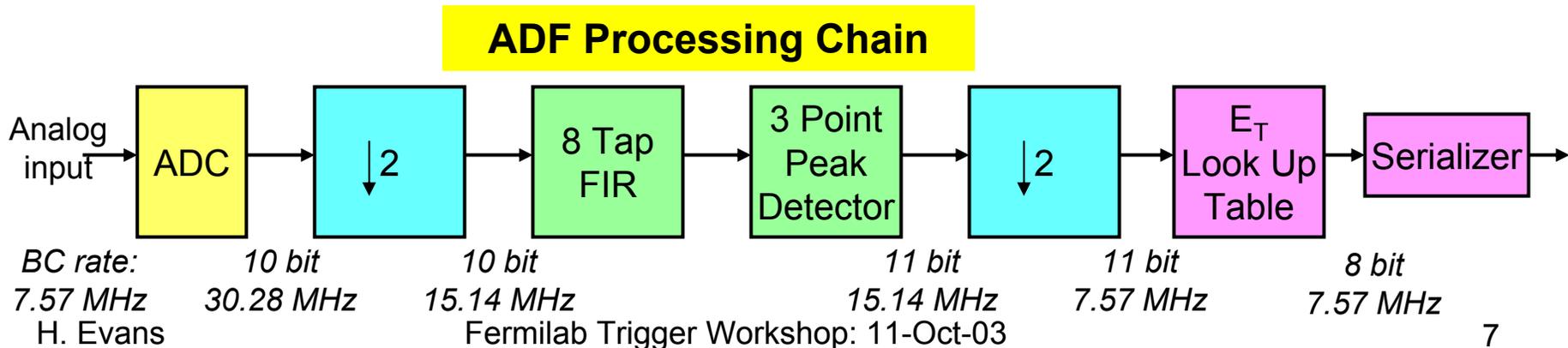


**L1 Rate Limit
~3 kHz**



Run IIb Solutions (1)

- **Solution to Signal Rise Time: Digital Filtering**
 - ◆ digitize Cal trigger signals
 - ◆ 8-tap FIR (6-bit coeff's) + Peak Detector run at $BC \times 2$
 - ◆ reformats output for transmission to physics algo stage
- **Benefits**
 - ◆ allows running at 132 ns (keeps this option open)
 - ◆ improvements in energy resolution (under study)
 - ◆ note: this stage is necessary as input to algo stage



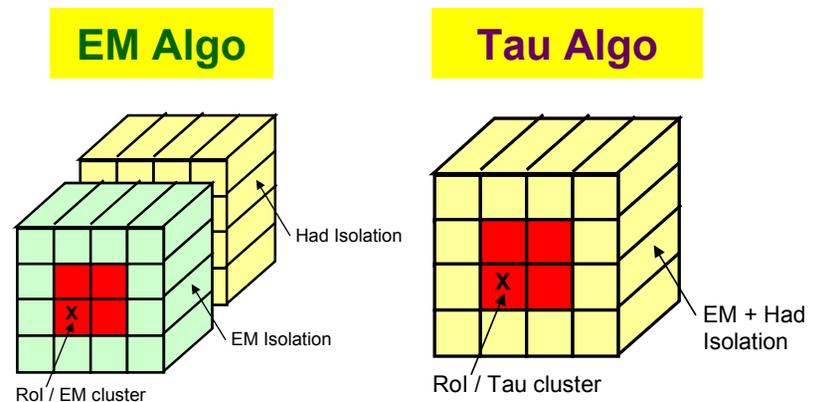
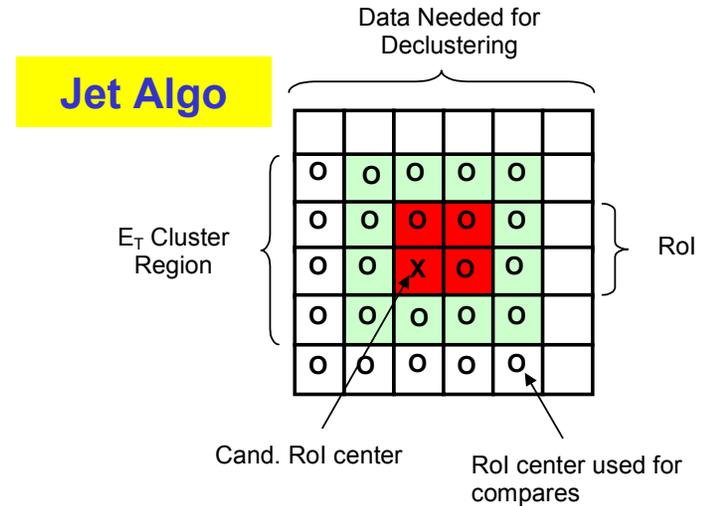


Run IIb Solutions (2)

- **Solution for Rates:**
Sliding Windows Algorithm
 - ◆ Et cluster local max. search on 40×32 ($\eta \times \phi$) TT grid
 - ◆ Jet, EM & Tau algo's
 - ◆ Better calc of missing Et
 - ◆ Topological Triggers
 - ◆ Jet, EM clust output for matching with L1 Tracks

- **Benefits**

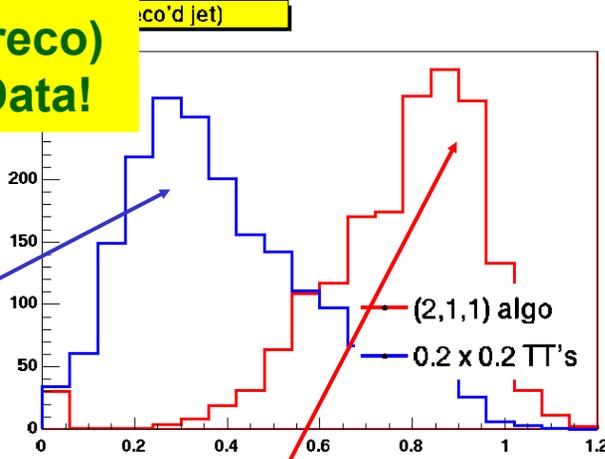
- ◆ $\times 2.5-3$ Jet Rate reduction at const. eff.
 - ▲ ZH \rightarrow $\nu\nu b\bar{b}$ Rate:
2.1 \rightarrow 0.8 kHz
- ◆ Similar gains for EM & Tau
- ◆ MEt, Topological Triggers under study





Algorithm Results

**Et(trig) / Et(reco)
w/ Run Ila Data!**

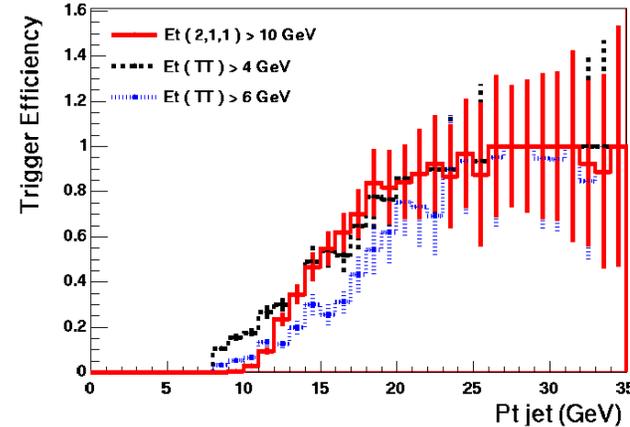


TTs
Ave = 0.4
RMS/Ave = 0.5

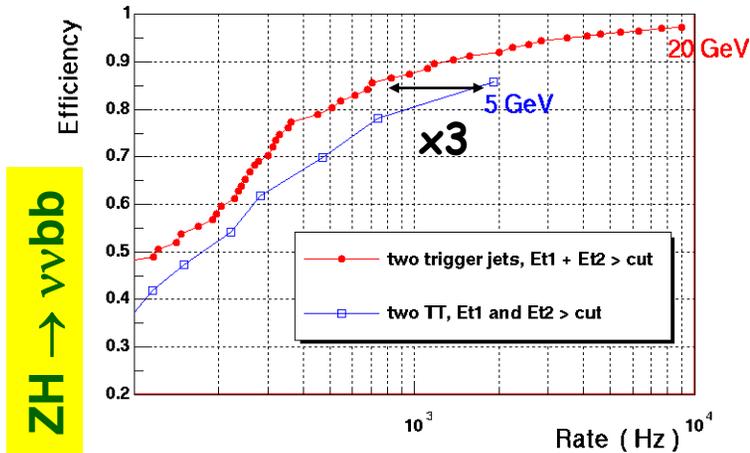
Sliding Windows
Ave = 0.8
RMS/Ave = 0.2

**Turn-on
Curves
from data**

(2,1,1) algo vs current trigger, J/ψ sample



Selectivity on ZH → νν + jets (mb=7.5)



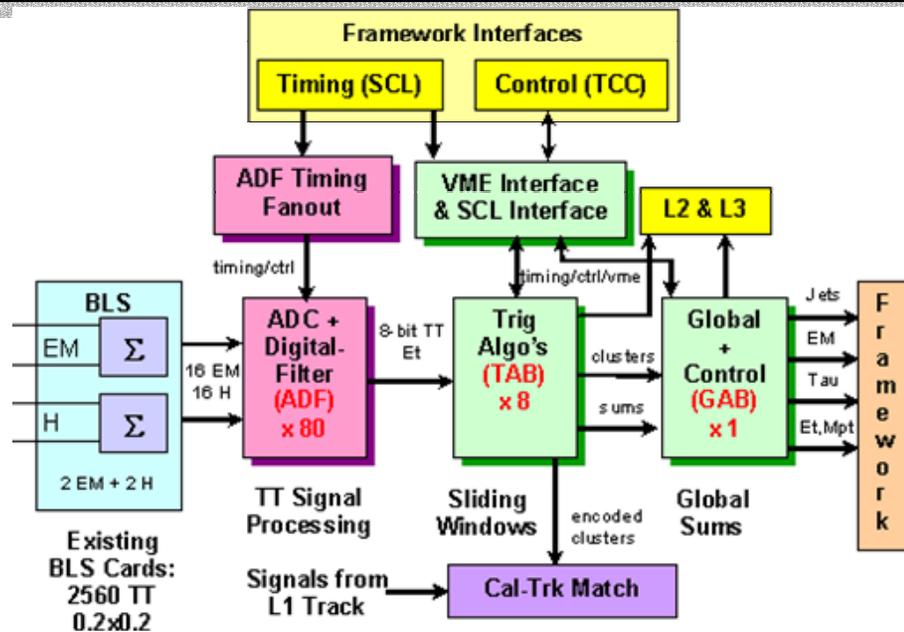
ZH → ννbb

Algorithm Study Status

Algo	Rate Red. @ const eff	Comments
Jet	2.5 – 3	most studied
EM	?	gains possible ???
Tau	O(2)	very preliminary
ICR	?	tools available



The Run IIb L1Cal System



Custom Board	No	Purpose
ADF: ACD/Dig. Filt.	80	digitize, filter, E-to-Et
ADF Timing F'out	4	ADF control/timing
TAB: Trig Algo Board	8	algo's, Cal-Trk out, sums
GAB: Global Algo Board	1	sums, trigs to FWK
VME/SCL Board	1	VME comm & timing f'out to TAB/GAB



The L1Cal Team

Saclay

- ◆ Physicists:
- ◆ Engineers:

J.Bystricky, P.LeDu*, E.Perez
D.Calvet, Saclay Staff

ADFs/ADF Timing/Splitters

Columbia/Nevis

- ◆ Physicists:
- ◆ Engineers:

H.Evans*, C.Johnson, J.Parsons, J.Mitrevski
J.Ban, B.Sippach, Nevis Staff

TABs/GABs/VME-SCL

Michigan State

- ◆ Physicists:
- ◆ Engineers:

M.Abolins*, C.Brock, H.Weerts
D.Edmunds, P.Laurens

Framework/Online Software

Northeastern

- ◆ Physicists:

D.Wood

Online Software

Fermilab

- ◆ Engineers:

G.Cancelo, V.Pavlicek, S.Rapisarda

Test Waveform Generator

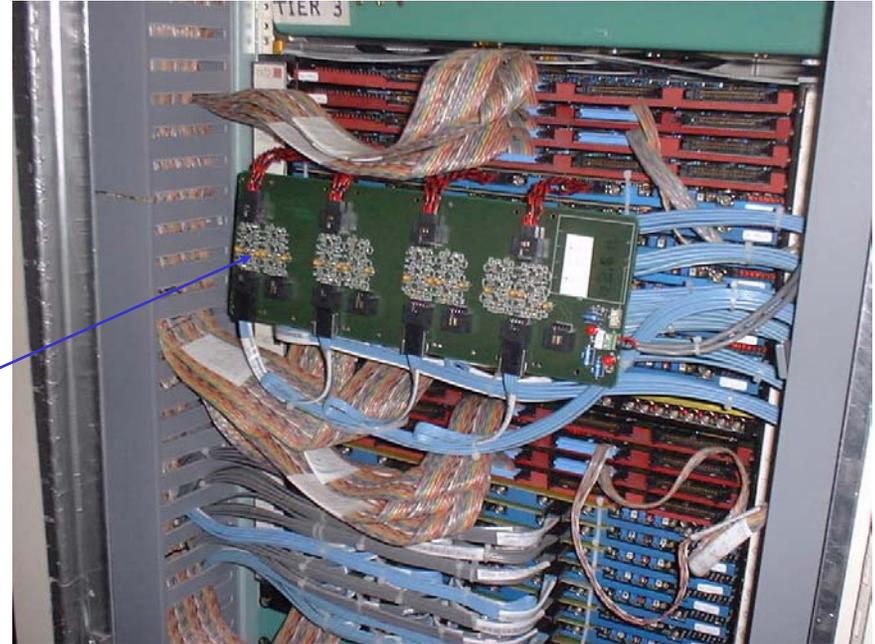
* L1Cal Project Leaders



Signal Splitter

- **Access to Real TT Data using “Splitter” Boards**

- ◆ designed/built by Saclay
- ◆ active split of analog signals at CTFE input
- ◆ 4 TTs per board
- ◆ installed: Jan. 2003



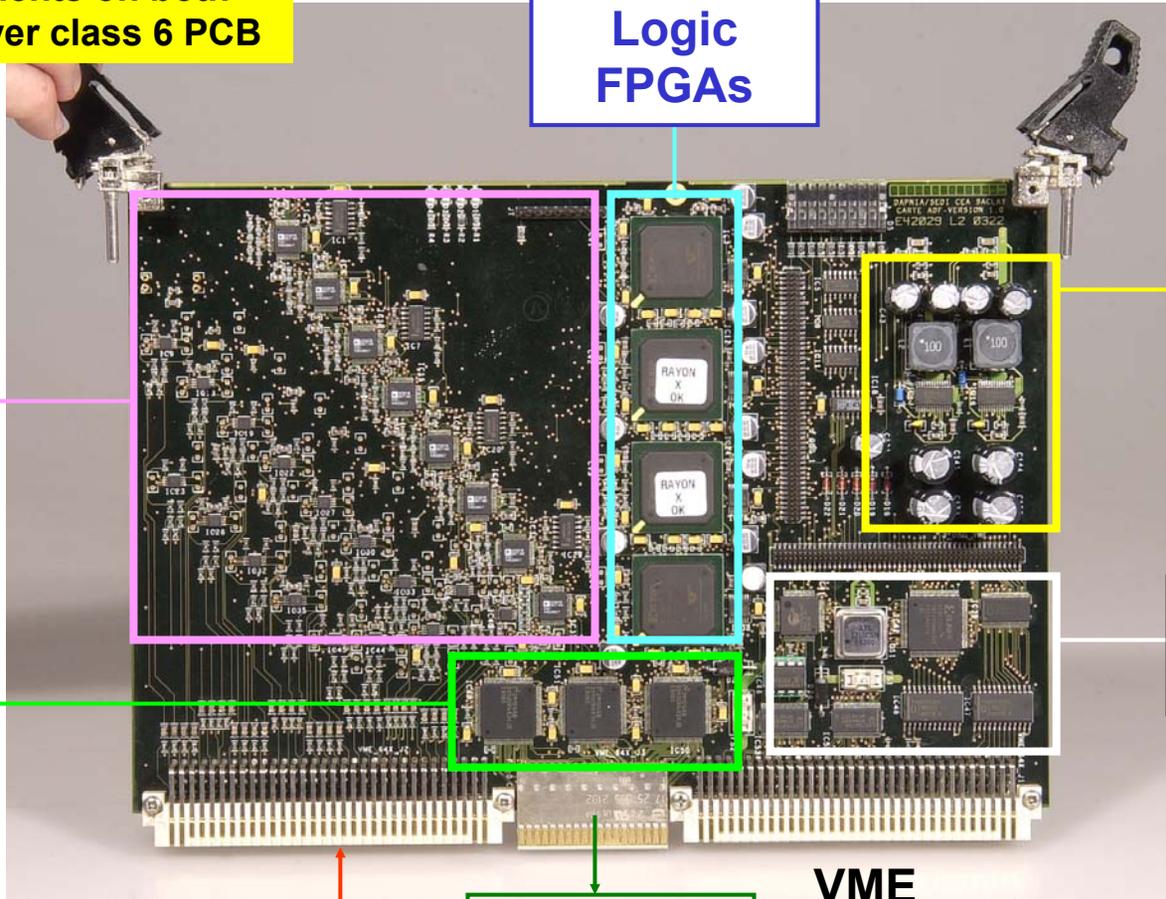
- **Splitter Data**

- ◆ no perturbation of Run IIa L1Cal signals
- ◆ allows tests of digital filter algorithm with real data



ADF Prototype

~1300 components on both sides of a 14-layer class 6 PCB



Logic FPGAs

Analog & ADCs

DC/DC Conv.

Channel Link Xmit

VME Interface

BLS Input (32 TTs)

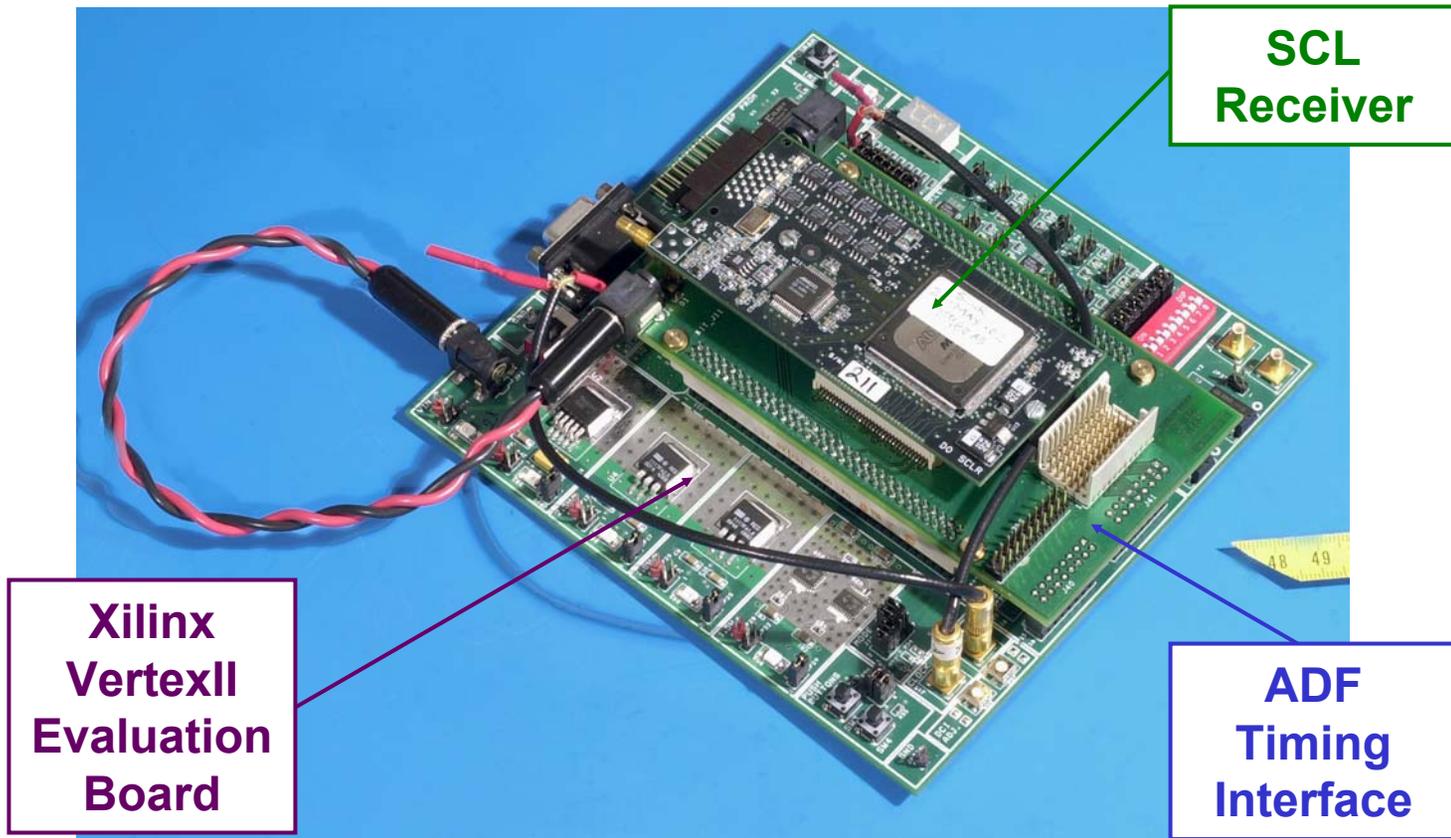
to TABs (3 cables)

VME

Internal Functionality mainly tested



ADF Timing Test Card





TAB Prototype

DC/DC conv

Channel Link Receivers (x30)

power

VME/SCL

L2/L3 Output (optical)

Output to GAB

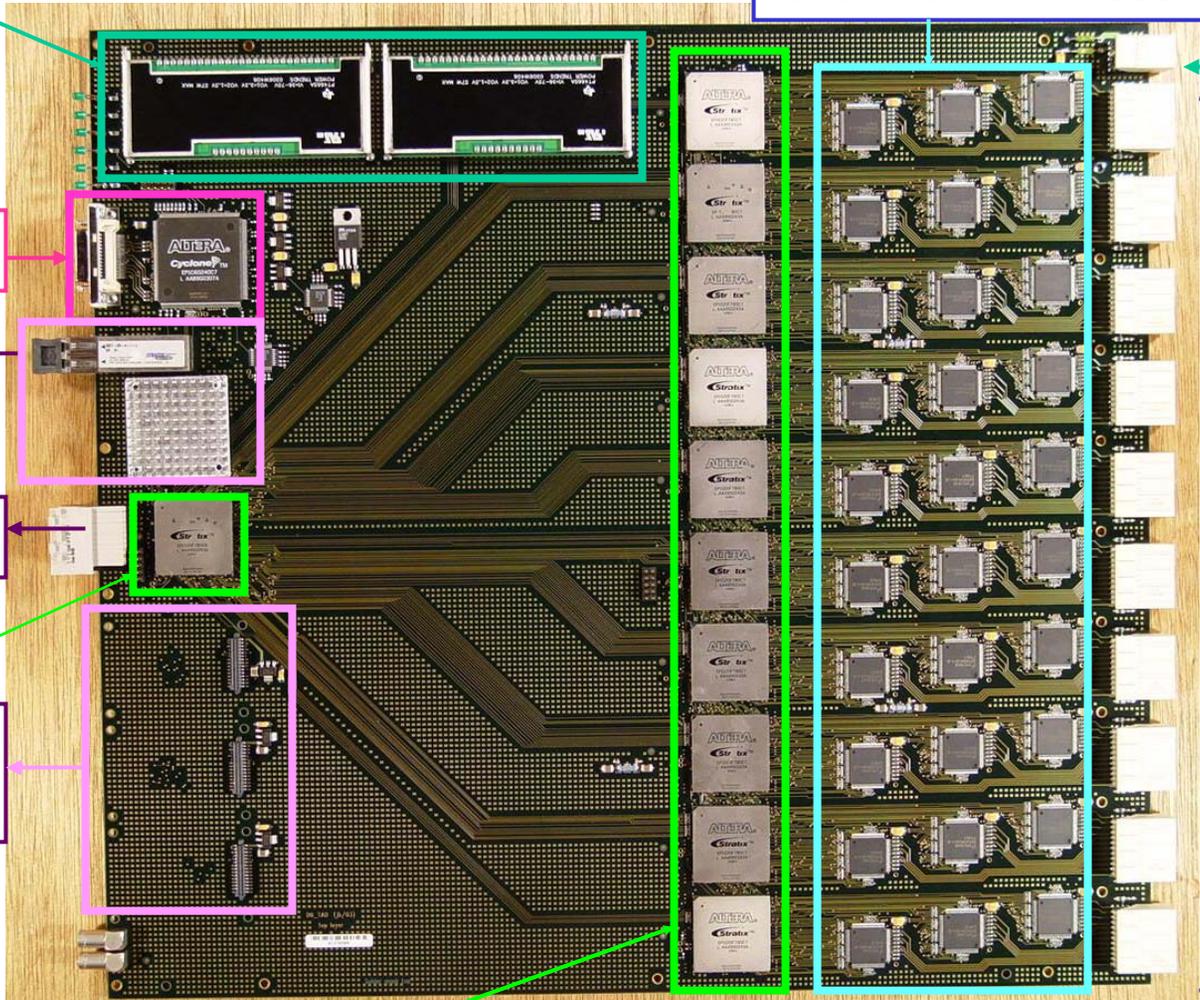
Global Chip

Output to Cal-Track (x3)

ADF Inputs (x30)

Sliding Windows Chips (x10)

Internal Functions ~Fully Tested





VME/SCL Board

- **New Comp. of TAB/GAB system**

- ◆ proposed: Feb 03
- ◆ change control: Mar 03

- **Interfaces to**

- ◆ **VME (custom protocol)**
 - ▲ not enough space on TAB for standard VME
- ◆ **D0 Trigger Timing (SCL)**
- ◆ **(previously part of GAB)**

- **Why Split off from GAB**

- ◆ **simplifies system design & maintenance**
- ◆ **allows speedy testing of prototype TAB**

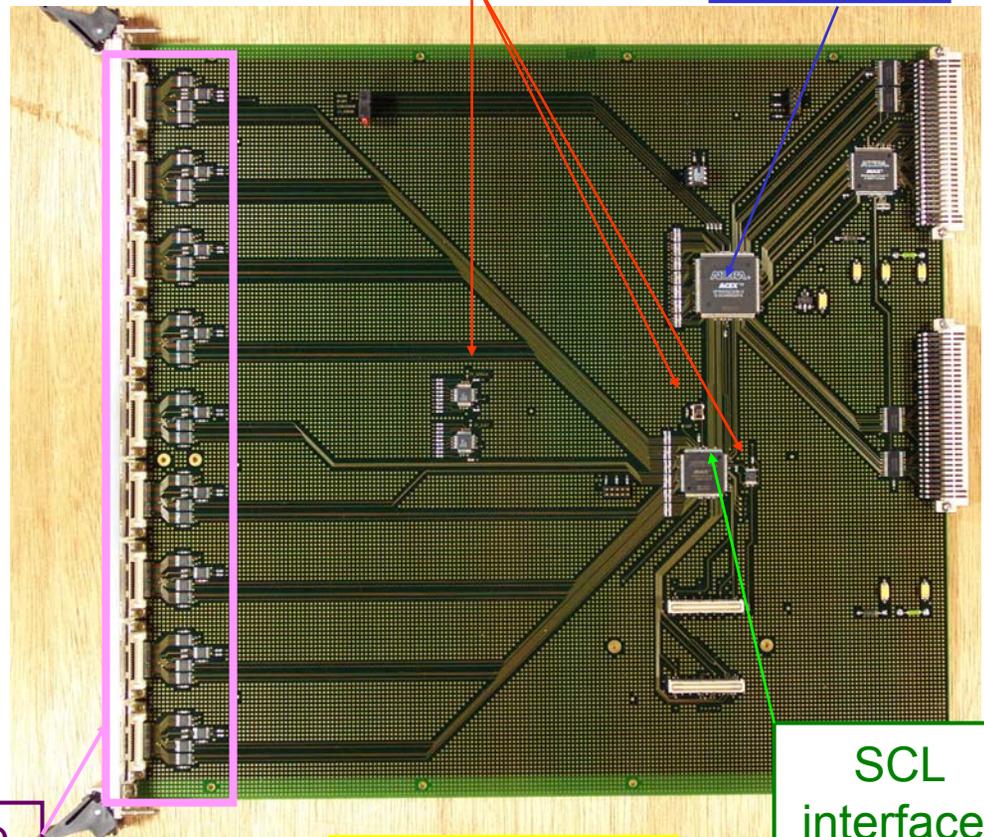
- **Fully Tested:**

Jun 12

serial out x9
(VME & SCL)

local osc's & f'out
(standalone runs)

VME
interface



Fully Tested

SCL
interface



TAB/GAB Test Card

TAB/GAB Data Rates

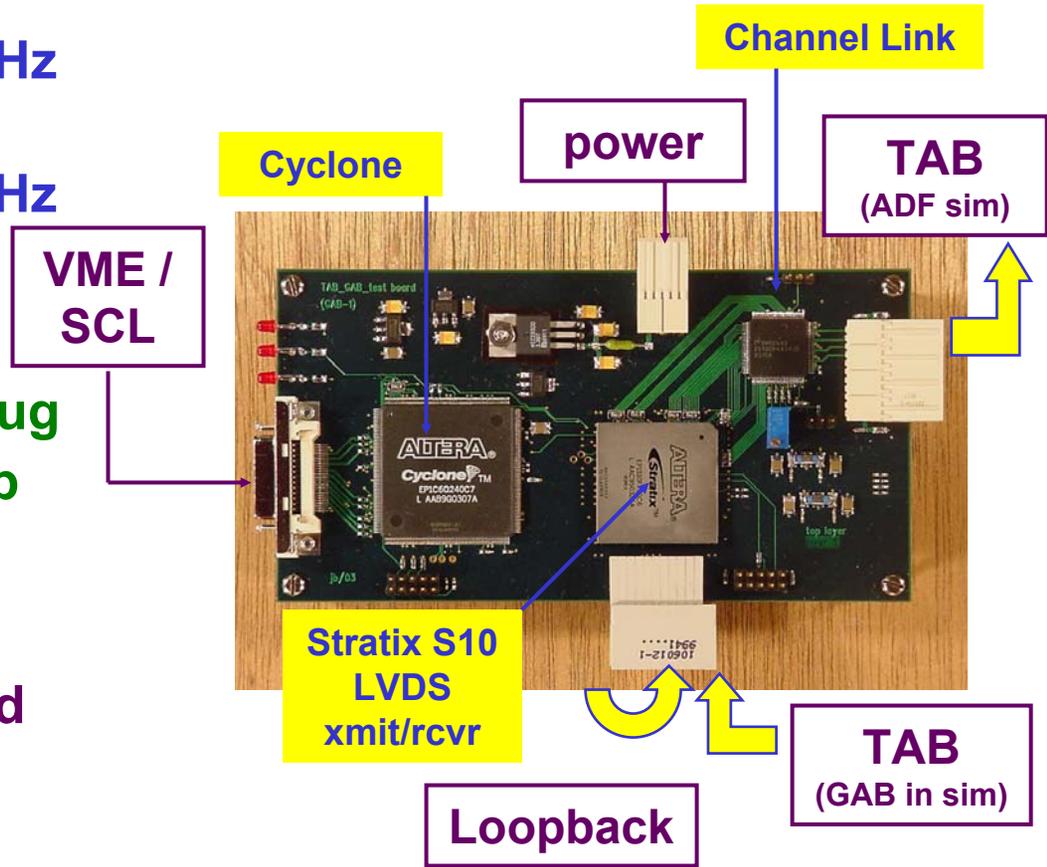
- ◆ TAB: LVDS 424 MHz
 - ▲ (channel link)
- ◆ GAB: LVDS 636 MHz
 - ▲ (stratix)

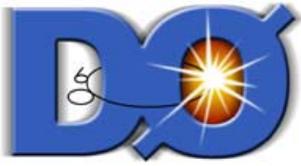
Test Card at Nevis

- ◆ Start Design mid-Aug
- ◆ Board at Nevis 29-Sep
- ◆ Cost \$790

● Status

- ◆ ADF-to-TAB xmit tested before integration
- ◆ Will test TAB-to-GAB before sending out GAB for fabrication





Prototype Integration Tests

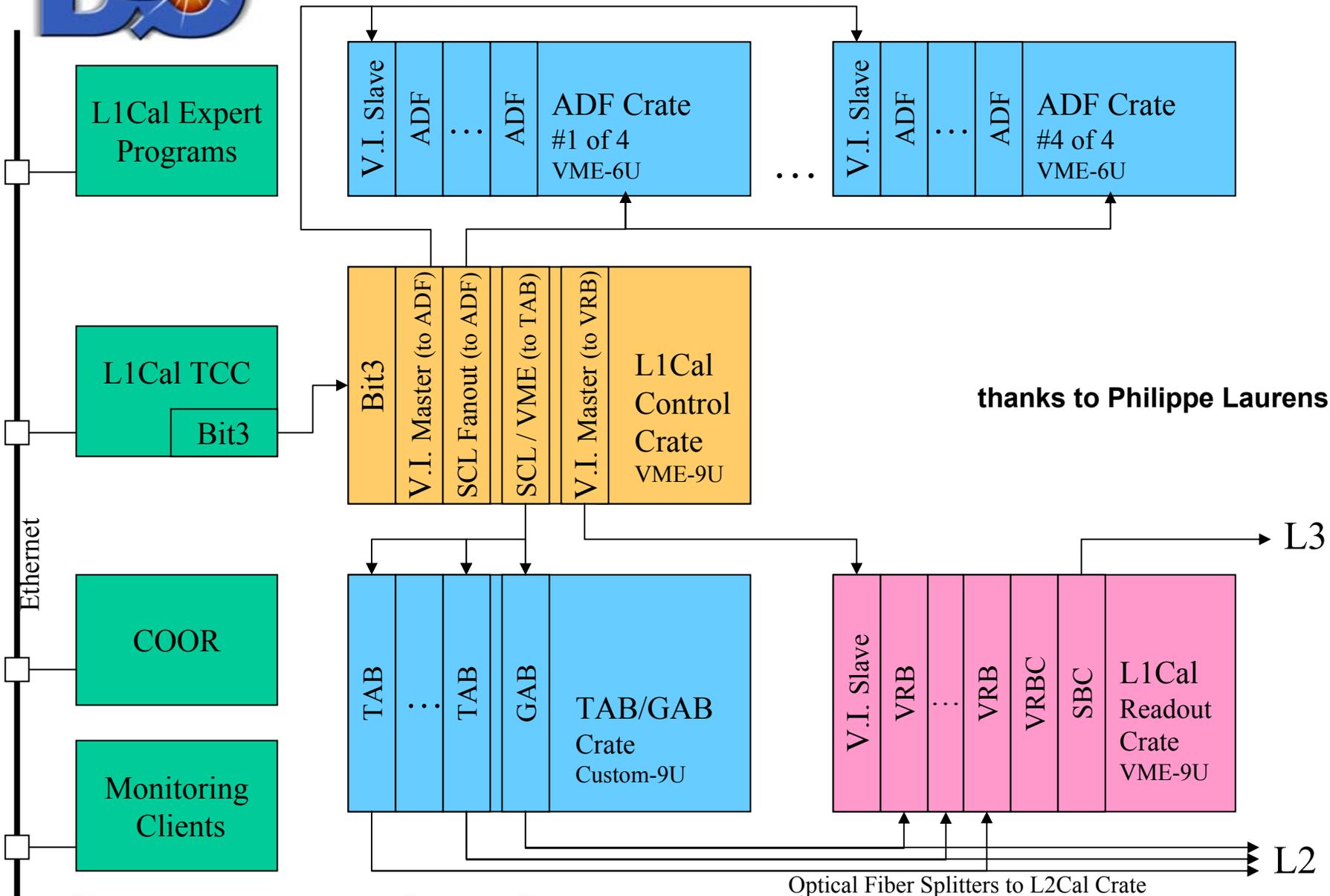
- **Stage I** **29-30 July**
 - ◆ Receive SCL trigger/timing information from SCL Hub to VME/SCL Card

- **Stage II** **8-17 October**
 - ◆ SCL → ADF Timing Card → ADF done
 - ◆ SCL → VME/SCL Card → TAB done
 - ◆ ADF → TAB Data transfer 1st data seen
 - ◆ TAB → Cal-Track timing & data checked

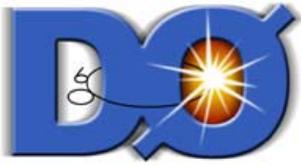
- **Future Stages**
 - ◆ ADF → TAB with full timing
 - ◆ BLS → ADF
 - ◆ TAB → L2
 - ◆ BLS → ADF → TAB → GAB
 - ◆ Test Area should operate ~DC at some point



Run IIb L1 Calorimeter Trigger Control Path



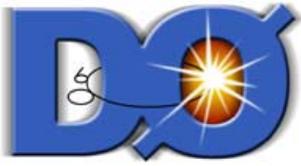
thanks to Philippe Laurens



Selected Schedule Milestones

Milestone	Curr. Sched End	Lehman End
TAB Prototype (bench tested)	8/29/03	5/16/03
ADF Prototype (bench tested)	10/7/03	5/2/03
VME/SCL (bench tested)	6/17/04	—
GAB Prototype (bench tested)	1/30/04	7/16/03
Prototype Integration Tests	1/26/04	10/9/03
Pre-Production Integration	10/1/04	5/5/04
Production Readiness Review	10/8/04	5/12/04
TAB Production (bench tested)	3/25/05	10/18/04
ADF Production (bench tested)	5/13/05	12/8/04
GAB Production (bench tested)	7/5/05	2/7/05
L1Cal Production Complete	7/5/05	2/7/05

- **Main Cause of Delays** **Complicated Design & Layout of ADF & TAB**
- **Integration Success** **More time at Prototype Stage Worth the Effort**



Costs (my interpretation)

Item (*)	Equipment	Labor	Main Source
ADF Prototype & Splitter	\$59K	\$360K	Saclay
SCL Interface	\$4K	\$53K	?
ADF Production	\$167K	\$118K	Project
ADF Crates	\$54K	\$69K	Project/Saclay
TAB Prototype	\$26K	\$132K	Nevis
TAB Production	\$83K	\$32K	Project
GAB & VME/SCL Prototype	\$17K	\$89K	Nevis
GAB & VME/SCL Production	\$11K	\$20K	Project
TAB Cables, Crate, Services	\$44K	\$23K	Project/Nevis
TOTAL(*)	\$464K	\$950K	\$1,414K

* Taken from Aug. 03 Schedule (to the best of my ability)

** Total includes some other misc. items



Costs (how are we doing?)

Item		Est. Unit Cost	Actual Unit Cost
TAB proto	components	\$7,900	\$4,700
	fabrication	\$2,000	\$310
	assembly	\$3,000	(incl. setup) \$3,500
VME/SCL	components	(GAB proto) \$7,500	\$350
	fab/assemb	\$4,500	\$440
Cables (full purchase)		\$17,780	\$19,700

- Note: enough TAB (13) & VME/SCL (5) pcb's for full production already procured
- No problems found with either prototype



The Future – Discussion

- **Saclay unable to continue in Project after Prototype Phase**
 - ◆ **BIG THANKS** for their **EXCELLENT** work
- **Migration of Saclay Responsibilities**
 - ◆ **ADF Production** **MSU**
 - ◆ **ADF Timing** interest expressed
 - ◆ **Digital Filtering** interest expressed
 - ◆ **Simulation Software** ???
- **Other Issues to Consider**
 - ◆ **Commissioning/Infrastructure** **UIC leads here**
 - ◆ **Calibration & Monitoring** **MSU + ???**
 - ◆ **Physics Studies** **???**
 - ▲ algo optimization, trigger terms, etc.
 - ◆ **Anything Else?**



More Discussion Points

1. Group Responsibilities

- ◆ any requests for rebaselining

2. Physics Studies Needed

3. Online Structure

4. Future Integration Plans

5. Anything I've Missed



Alphabet Soup

- **ADF: ADC & Digital Filter Card**
 - ♦ Run Ilb L1Cal card that digitizes and filters analog signals from BLS
- **ADF Timing (aka SCL Interface)**
 - ♦ Run Ilb L1Cal card that distributes SCL signals to ADFs
- **BLS: BaseLine Subtractor Card**
 - ♦ Run IlA/Ilb card that constructs analog TT signals from calorimeter cell signals (in collision hall)
- **CTFE: Calorimeter Trigger Front End Card**
 - ♦ Run IlA card that digitizes BLS signals, counts TTs over threshold and does first stage of Et summing (in MCH1)
- **GAB: Global Algorithm Board**
 - ♦ Run Ilb card that collects TAB outputs, constructs trigger terms and transmits them to the TFW
- **LVDS: Low Voltage Differential Signal**
 - ♦ Serial data transmission protocol used for communication between Run Ilb L1Cal components
- **MCH: Movable Counting House**
 - ♦ MCH-1 (1st floor) houses L1Cal. This is accessible during data taking.
- **SCL: Serial Command Link**
 - ♦ Means of communicating D0 TFW timing and control signals to all parts of D0 Trigger/DAQ
- **Splitter**
 - ♦ Splits analog signals from BLS (at CTFE) for Run Ilb L1Cal studies
- **TAB: Trigger Algorithm Board**
 - ♦ Run Ilb card that performs sliding windows and Et summing algorithms on ADF outputs
- **TFW: Trigger Framework**
 - ♦ System that collects trigger terms from all D0 trigger systems, makes final trigger decisions and distributes timing and control
- **TT: Trigger Tower**
 - ♦ 0.2x0.2 ($\eta \times \phi$) region of calorimeter cells (EM or Hadronic) used as input to L1Cal
- **VME/SCL Card**
 - ♦ Run Ilb card that interfaces TABs/GABs to VME using a custom serial protocol and distributes SCL signals to the TABs/GABs