



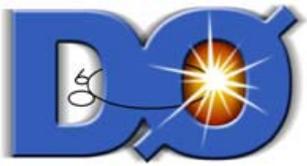
L1CalTrack Status

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Outline

- Overview
- L1MU Dark Corners
- Differences between L1MU and L1CalTrack
- L1CalTrack Status
- Commissioning Plans
- Simulation Status
- Concerns du Jour
- Conclusions



L1CalTrack Trigger

- Exploit L1Cal and L1CTT trigger upgrades to further reduce combinatoric contributions the L1 trigger rate
- Trigger algorithms match φ position of EM/jet objects from L1Cal with φ position of tracks from L1CTT
 - ◆ Isolation and CPS/FPS information is also available
 - ◆ Matching in E_T/P_T is also available
- Useful for any physics with high P_T electron or tau signatures
 - ◆ Electrons in WH and $H \rightarrow W^*W$ modes
 - ◆ Taus in $H \rightarrow \tau\tau$ and $H^+ \rightarrow \tau\nu$
- Old simulation results show
 - ◆ Fake EM rejection is improved by $\sim x2$
 - ◆ Fake τ rejection is improved by $\sim x10$



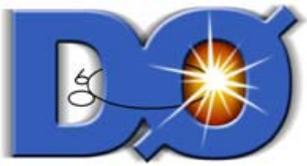
L1CalTrack Architecture

- Based on the existing L1MU trigger architecture
 - ◆ Trigger algorithms match φ position of hits in the muon scintillation counters with φ position of tracks from L1CTT
 - ◆ L1MU has been successfully running in DØ for close to two years
 - ◆ Synchronization, buffering, FPGA programming, output to L2 and L3, testing, debugging, monitoring, online/offline software and infrastructure have proven, working solutions



BOT

- BOT == Beginning of Turn trigger
- Formed at the beginning of each turn if data is available (Input Ready is there)
- Incredibly useful for monitoring the state of the trigger



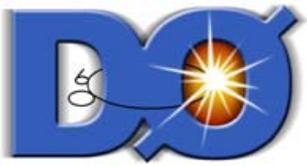
Dark Corners

- “Trigger dropout problem”
 - ◆ Trigger and BOT rate disappear after SCL INIT
 - ◆ Solution: Bad PECL clock driver replaced
- “CFT splitter problem”
 - ◆ Large number of parity errors (noise?) mainly on several channels on two splitters
 - ◆ Solution: Software problem now fixed
 - ◆ ~5 bad parity error channels / 300 total being tracked down



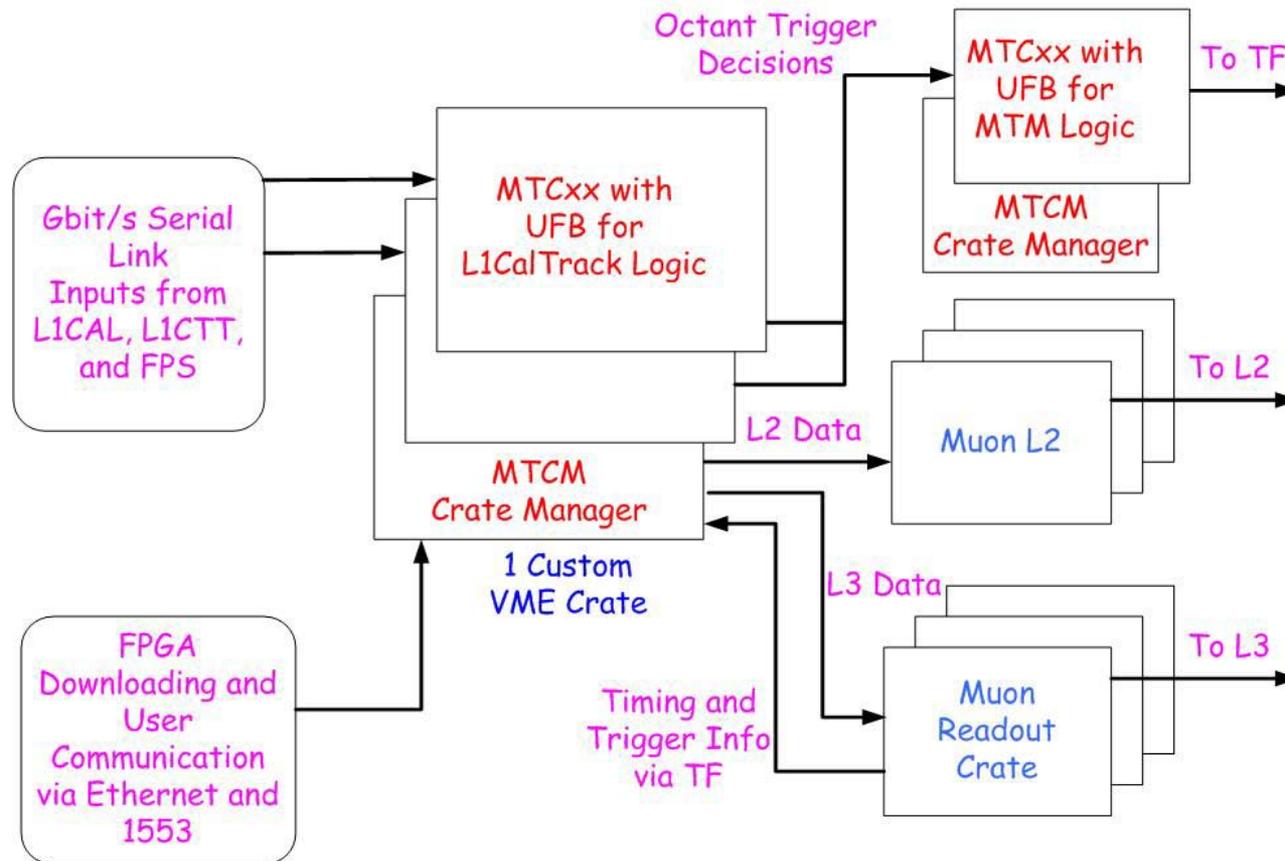
Dark Corners

- “MTCxx BC Number Problem”
 - ◆ 1% BC number disagreement from the MTCxx's
 - ◆ Solution: Firmware improvements seemed to have solved problem but need beam test to verify
- “Trigger Dropout During Readout Problem”
 - ◆ Trigger rate, not BOT rate, disappears when reading out particular MTCxx's
 - ◆ Solution: Firmware improvements seemed to have solved problem but need beam test to verify



L1CalTrack Trigger

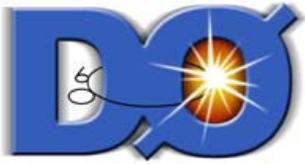
L1CalTrack Trigger System



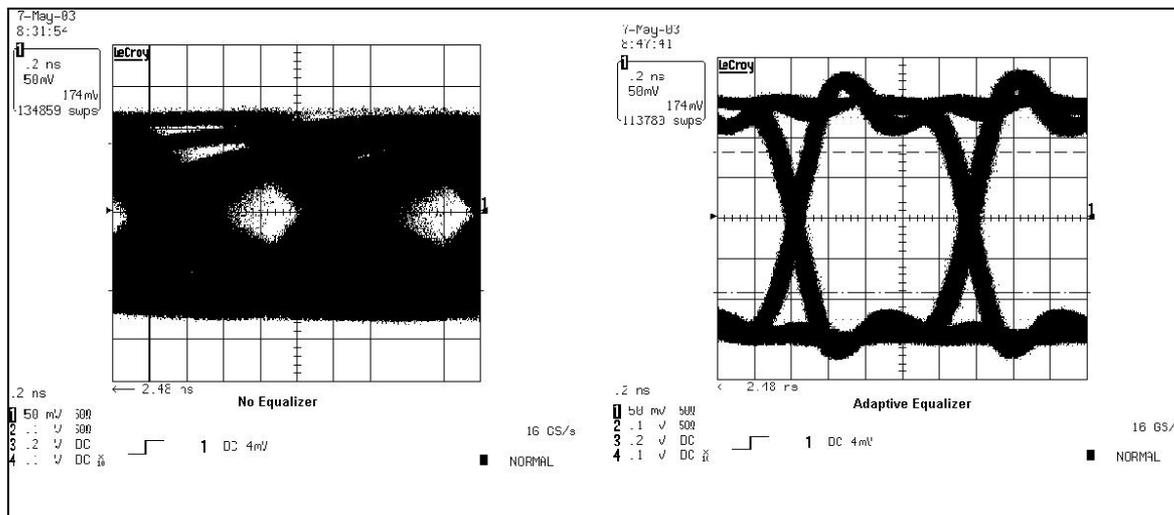
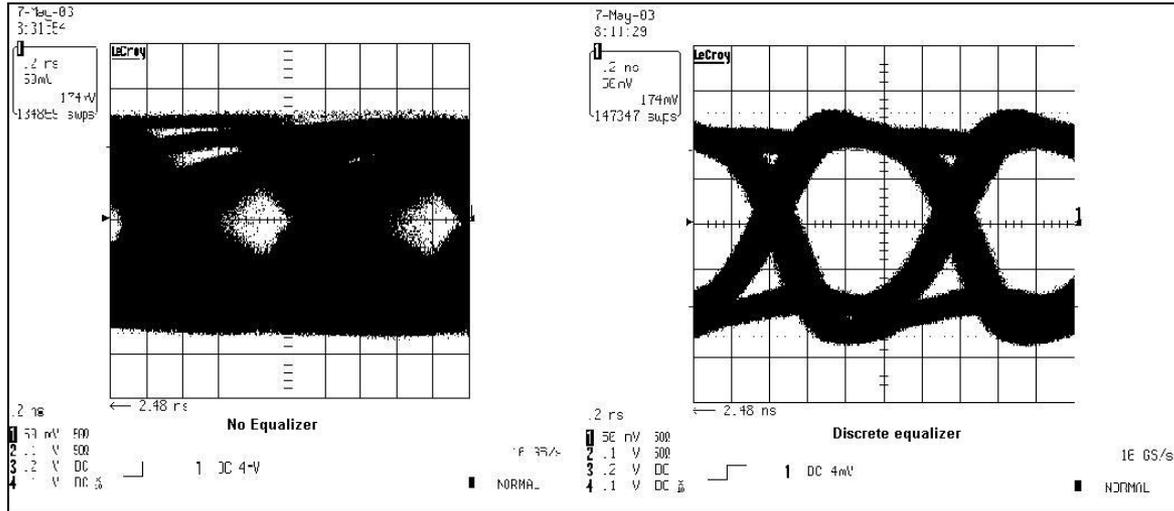


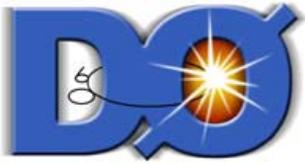
L1CalTrack/L1MU Differences

- **SLDB (Serial Link) Receivers**
 - ◆ Previous version used a discrete equalizer to compensate for cable attenuation
 - ◆ Limiting amplifier became obsolete and an adaptive equalizer (MAX...) became available
 - ◆ Improved performance over discrete equalizer!
 - ◆ But performance, though acceptable, was less than predicted so two more layouts are being tested before production
 - ◆ Update: Preferred layout reviewed and approved by Fermilab (no changes)



New SLDB RECV Equalizer





L1CalTrack/L1MU Differences

- MTCxx Trigger Card Changes
 - ◆ Two FPGA programming chains
 - ▲ Trigger and message building FPGA's were already remotely programmable
 - ◆ FPGA programming through front panel
 - ◆ Three JTAG chains introduced to allow boundary scan testing of almost all of the board's interconnections including the MTFB (aka UFB) and SLDB's
 - ◆ FIFO's and DPM's are now implemented on FPGA's
 - ◆ Flash memory is doubled in size to accommodate the larger Stratix devices



L1CalTrack/L1MU Differences

- Universal Flavor Board (UFB)
 - ◆ One MTFB daughterboard for L1CalTrack, MTC05, MTC10, and MTM logic
 - ▲ Previously needed three separate MTFB's
 - ◆ Allows for four additional serial inputs (16-→20)
 - ◆ Allows for four new serial outputs (0-→4)
 - ◆ Backwards compatible with V3 MTCxx's currently in use for L1MU if device smaller than EP1S30



L1CalTrack Status

- **MTCxx (Trigger Cards)**
 - ◆ Preproduction design complete
 - ◆ Layout and final checking in progress
 - ◆ Goal is to submit in November 03
- **UFB (Flavor Board)**
 - ◆ Prototypes in hand
 - ◆ JTAG boundary scan and program downloading OK
 - ◆ Receiver/transmitter testing in progress
 - ◆ L1MU "05" algorithm implemented in Stratix EP1S20F780C7 (simulated but not tested)
 - ◆ $H \rightarrow \tau\tau$ algorithm implementation in progress
- **MTCM (Crate Manger)**
 - ◆ Not started, but only minimal changes to the existing design



UFB FPGA Simulation

- Use L1MU EF MTC05 logic as a model for L1CalTrack UFB logic
- Quartus II with Stratix EP1S20F780C7
 - ◆ Demux logic block is universal
 - ◆ Remap/trigger logic block is application specific (MTC05 logic in this case)
- Results
 - ◆ Demux OK (flip-flop delay < RF clock)
 - ◆ Remap/trigger logic delay = 22.4 ns!
 - ◆ Total pin usage = 57%
 - ◆ Logic element usage = 39%



L1CalTrack Status

- **Infrastructure**

- ◆ VME crates, processors, power supplies, cables in hand
- ◆ L1CTT to L1CalTrack cables being installed this weekend (not terminated)
- ◆ Rack space in MCH1 identified (but not settled)

- **Commissioning**

- ◆ Plan is to use spare L1MU cards in L1CalTrack crates to establish communication with MRC and TF
- ◆ Replace these spares with L1CalTrack cards as they become available

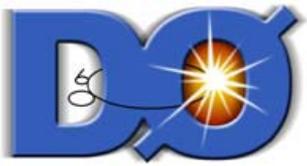
- **Simulator**

- ◆ Work has started writing the `tsim_l1caltrack` package and integrating it into the DO trigger simulator



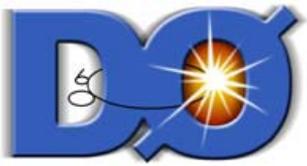
Commissioning

- Starting now
 - ◆ Bench test VME crates and power supplies
 - ◆ Safety review
 - ◆ Install in MCH1
 - ▲ May need management pressure here for our preferred rack
 - ▲ Rack infrastructure (blower, radiators, etc.)
 - ◆ Populate with spare L1MU trigger cards and managers
 - ▲ Replace with L1CalTrack cards as they become available
 - ◆ Install MRC in 3rd floor MCH (0x19)
 - ◆ Install 50c and Astro cables from MRC to MTCM



Commissioning

- ◆ Establish BOT trigger to TF using PDT or scintillator inputs
 - ▲ Need 16 TF A/O terms
- ◆ Establish RO to L3
 - ▲ Software changes?
 - ▲ Need software modifications to unpack expanded L1MU RDC
- ◆ Replace L1CTT transmitters with dual output transmitters and terminate LMR-200
 - ▲ Requires few day access
- ◆ Use L1Cal inputs as TAB's become available



Simulator Status

- Graduate student (Vernon Miller) working on $H \rightarrow \tau\tau$ algorithm
- Undergraduate student (Amy Dashiell) working on WH algorithm
 - ◆ Same student also working on FPGA implementation of $H \rightarrow \tau\tau$ algorithm
- Undergraduate student (Charles Armijo) with (industry) C++ experience working on writing and integrating tsim_l1caltrack



Monte Carlo Samples

- Signal == Pythia
 $H \rightarrow \tau\tau$ with $m(H) = 135 \text{ GeV}/c^2$
- Background == Pythia
QCD binned in p_T as shown in the table
 - ◆ No underlying minimum bias events for this study
- QCD with overlaid minimum bias events being generated by Erich Varnes

p_T (GeV)	σ (μb)
5 - 10	6894
10 - 20	570
20 - 40	34
40 - 80	1.4
80 - 160	0.04
160 - 320	$8 \text{ e-}4$
> 320	$4 \text{ e-}6$



Goal

- Develop an L1CalTrack algorithm for $H \rightarrow \tau\tau$ with an L1 rate < 1 kHz
 - ◆ Uses upgraded L1Cal information
 - ◆ Uses current L1CTT information
 - ◆ Uses algorithms implemented as Root macros



Trigger Algorithm

- For each event there must be at least one track that satisfies the following conditions for the trigger to fire:
- Phi matching
 - ◆ The phi information from the calorimeter and CFT must match
- Isolation
 - ◆ Tracks are defined to be isolated if the adjacent sectors contain no tracks
- E_T/p_T matching
- $p_T > 3 \text{ GeV}$ for $E_T > 20 \text{ GeV}$
- Counting
 - ◆ > 1 but not in adjacent calorimeter phi segments



Present Results

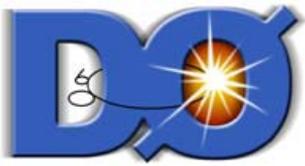
E_T/p_T Thresholds

E_T (GeV)	20	21	35	40
p_T (GeV)	1.5	3	5	11

← Chosen

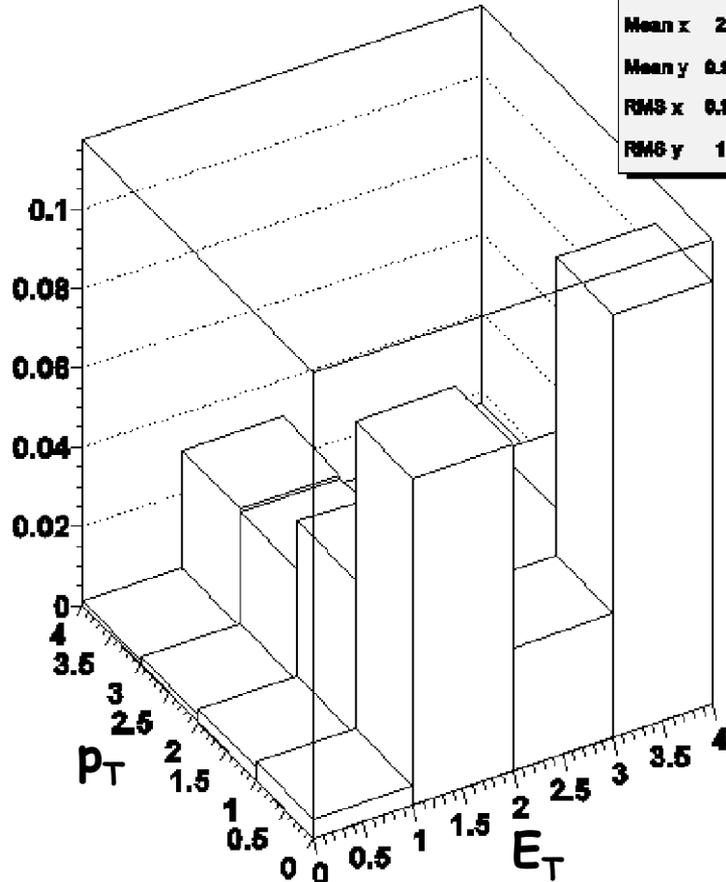
← Fixed

- Signal efficiency $\approx 30\%$
- Total background rate ≈ 125 Hz at $L=2e32$



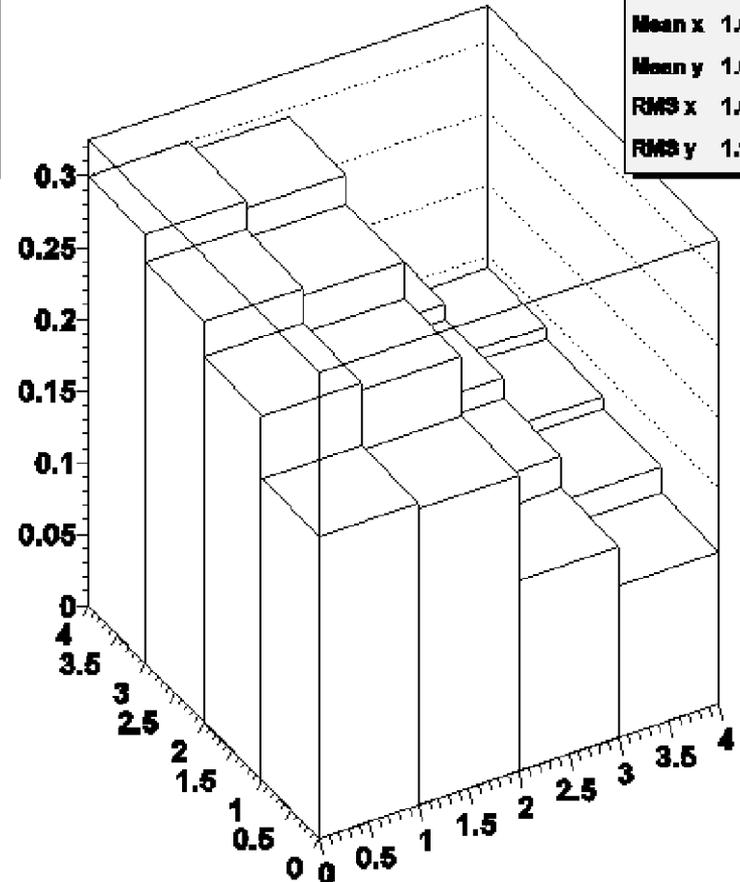
Signal Efficiency vs. E_T/p_T Thresholds

Individual Efficiencies



IndEff	
Entries	16
Mean x	2.481
Mean y	0.0066
RMS x	0.9819
RMS y	1.072

Inclusive Efficiencies



IncEff	
Entries	16
Mean x	1.699
Mean y	1.632
RMS x	1.067
RMS y	1.101



Concerns du Jour

- MCH1 rack space
- CPS info in L1CTT tracks
 - ◆ Need communication with Meena et al
- FPS inputs and info
 - ◆ Need communication with Jamieson et al
- Latency (always)
- Plan for mods to PDT electronics



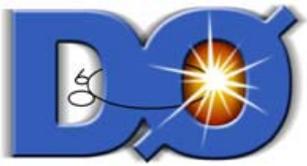
Trigger Study Todo

- Use QCD plus minimum bias events for background
- Compare simulator rates to Run 2 collider rates
- Study E_T/p_T matching
- Develop single electron algorithm

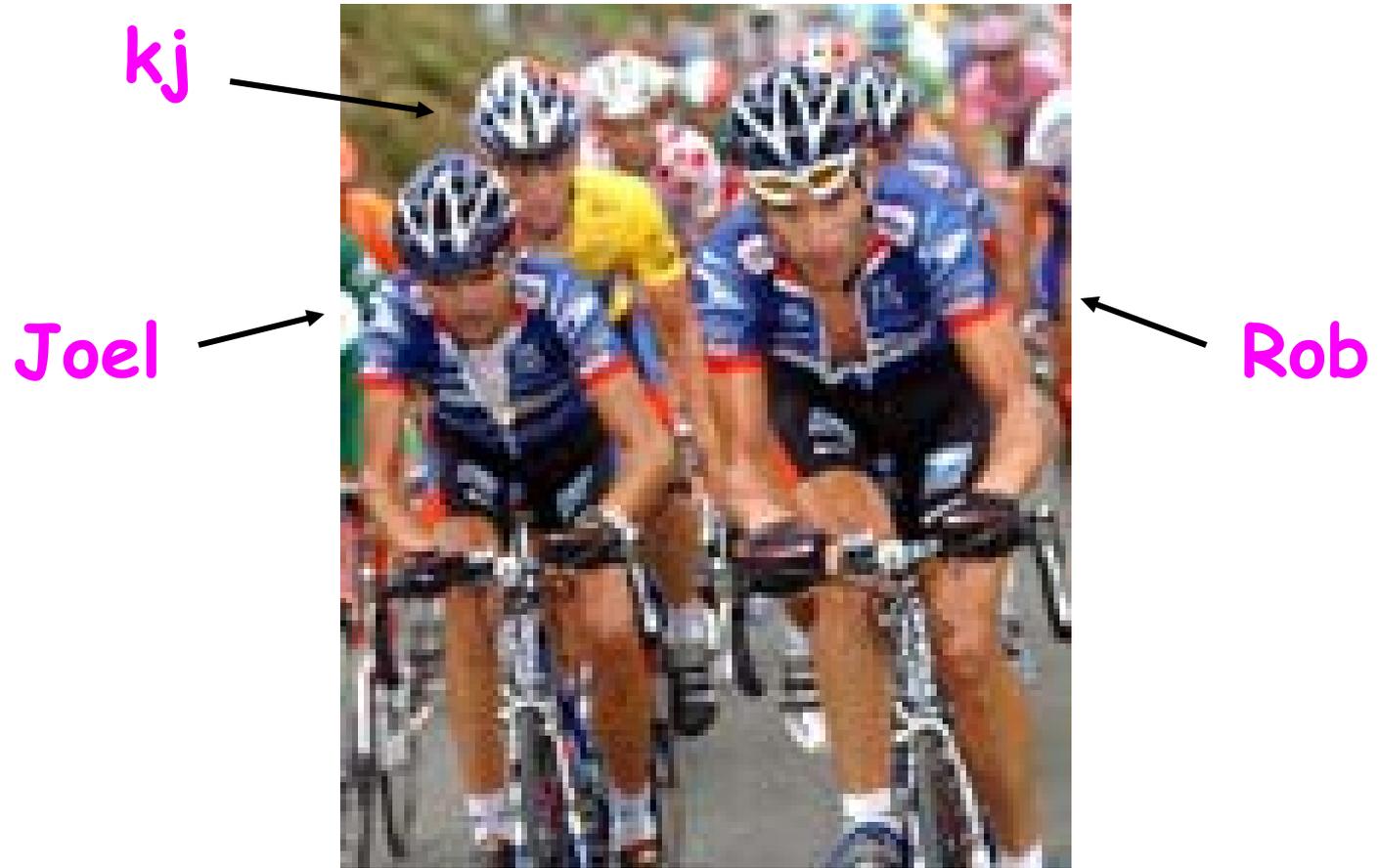


Conclusions

- L1CalTrack continues to make steady progress
- Latest schedule begins production of MTCxx and UFB cards in late spring 2004
- (Slowly) beginning commissioning now
- Active work in progress writing and integrating `tsim_l1caltrack` into `tsim_l1l2`



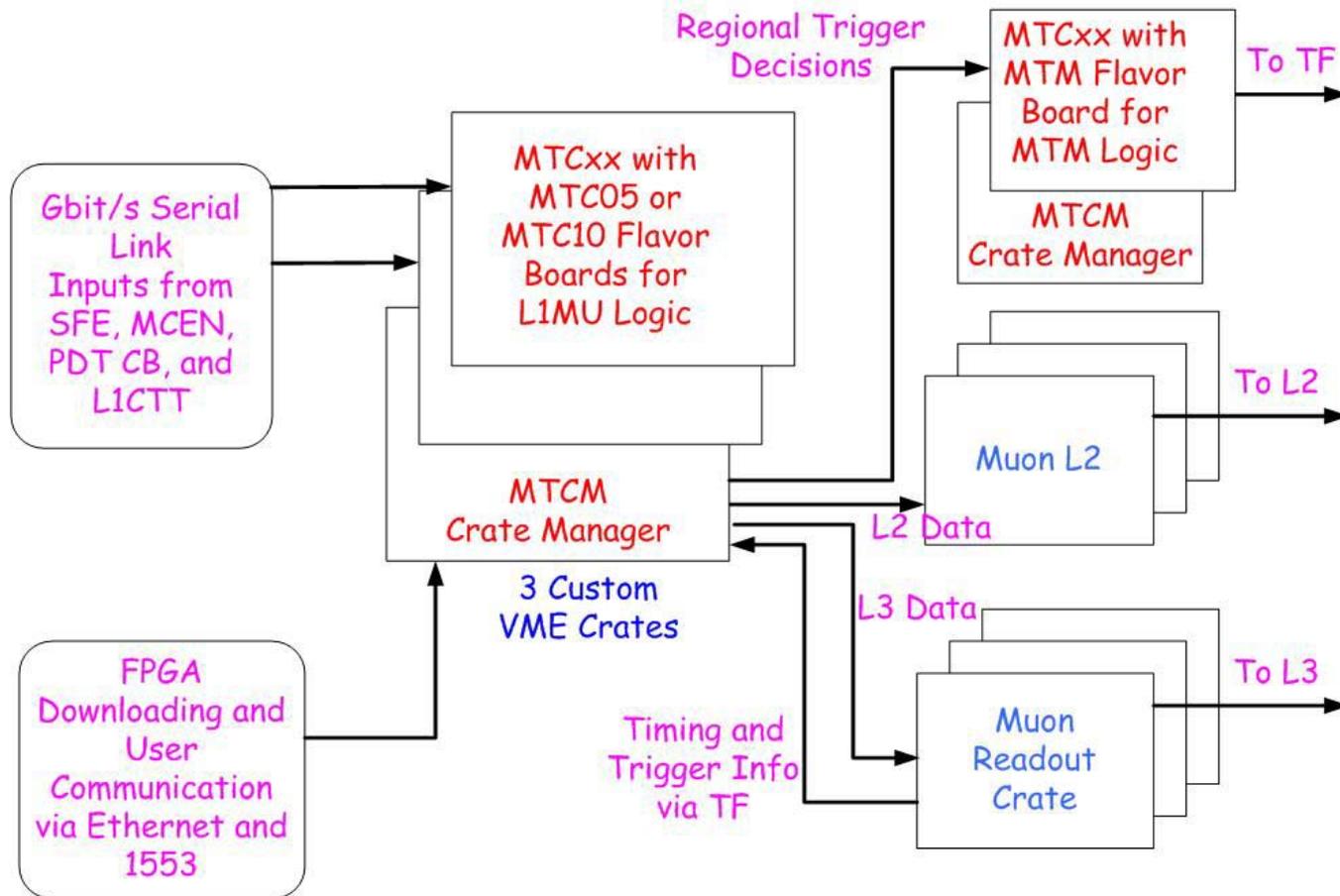
Missing Some Key Teammates





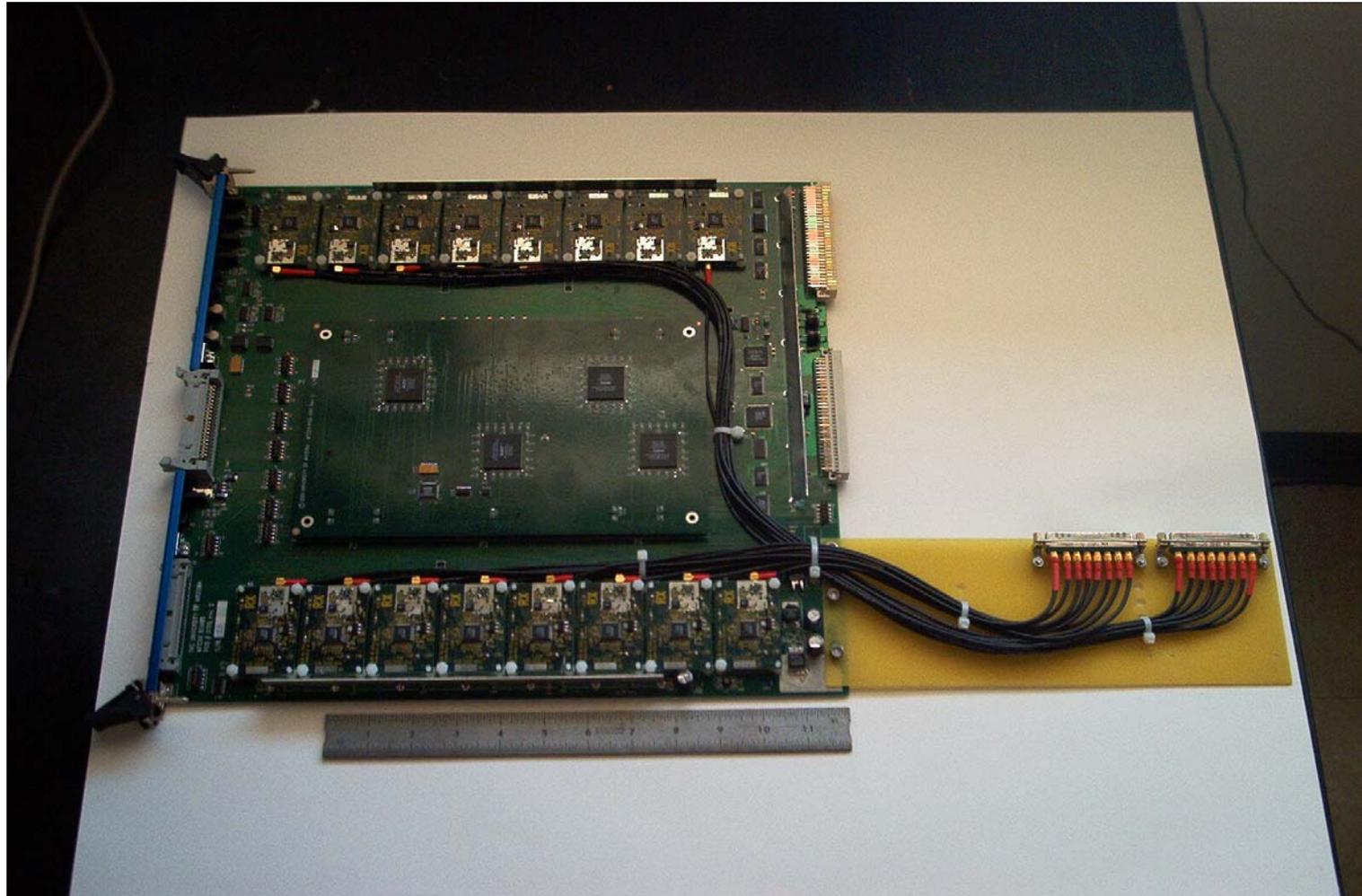
L1MU Trigger

L1MU Trigger System





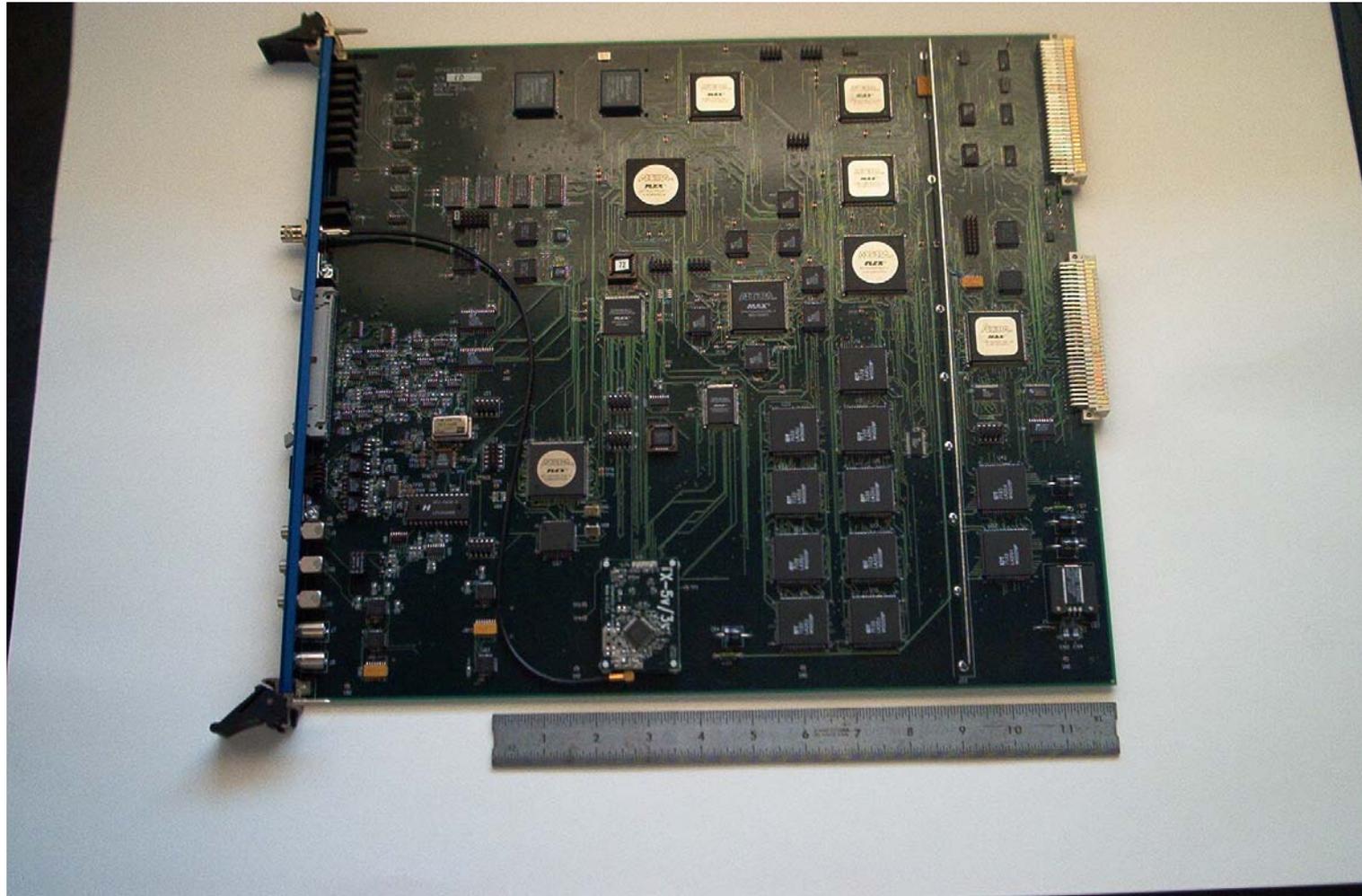
MTCxx (Trigger Card) with MTFB (Flavor Board)



Some DO Meeting
October 2003



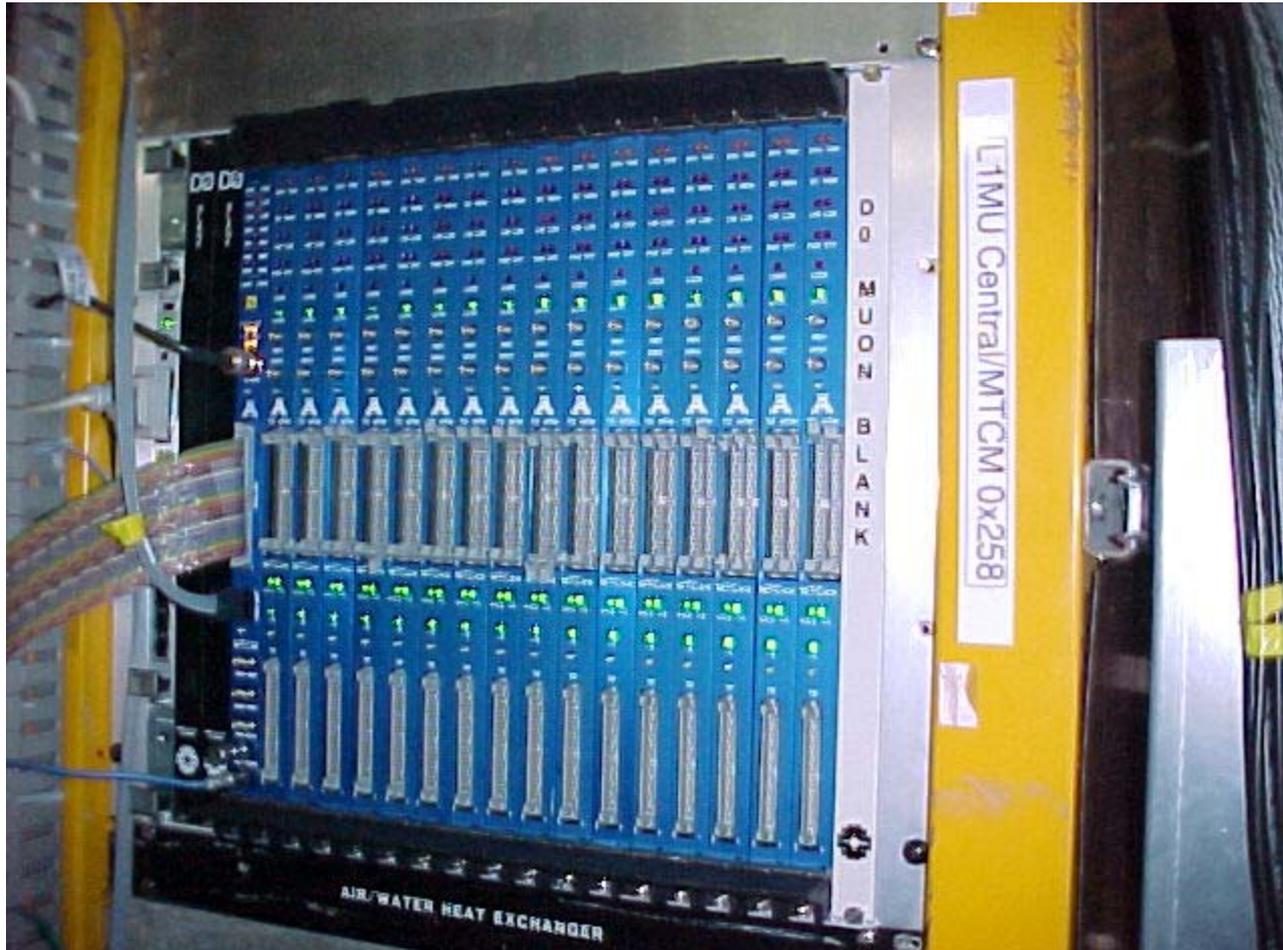
MTCM (Crate Manager)

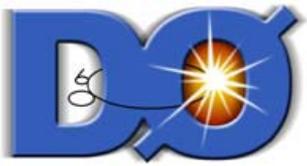


Some DO Meeting
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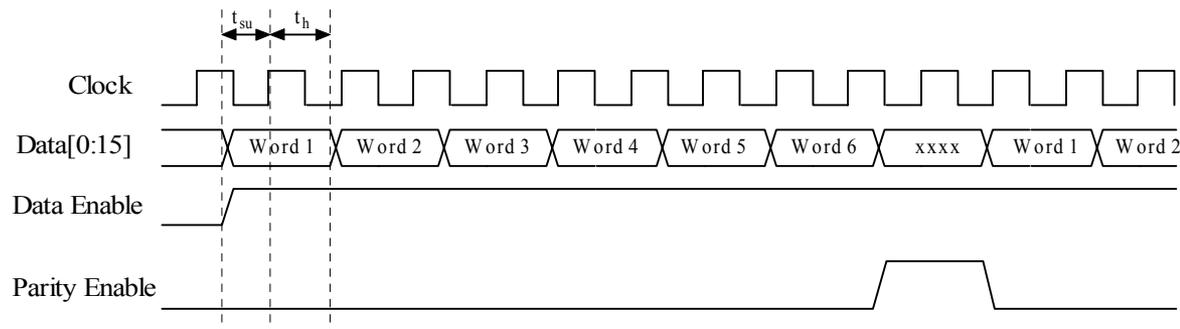
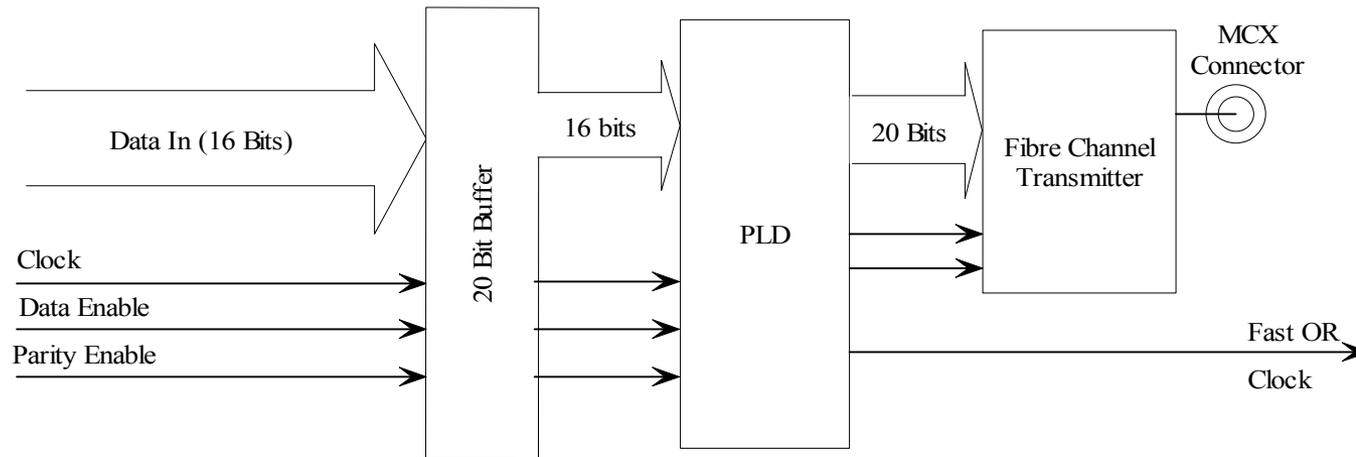


Installed in Collision Hall



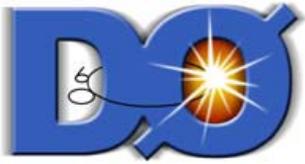


SLDB XMIT

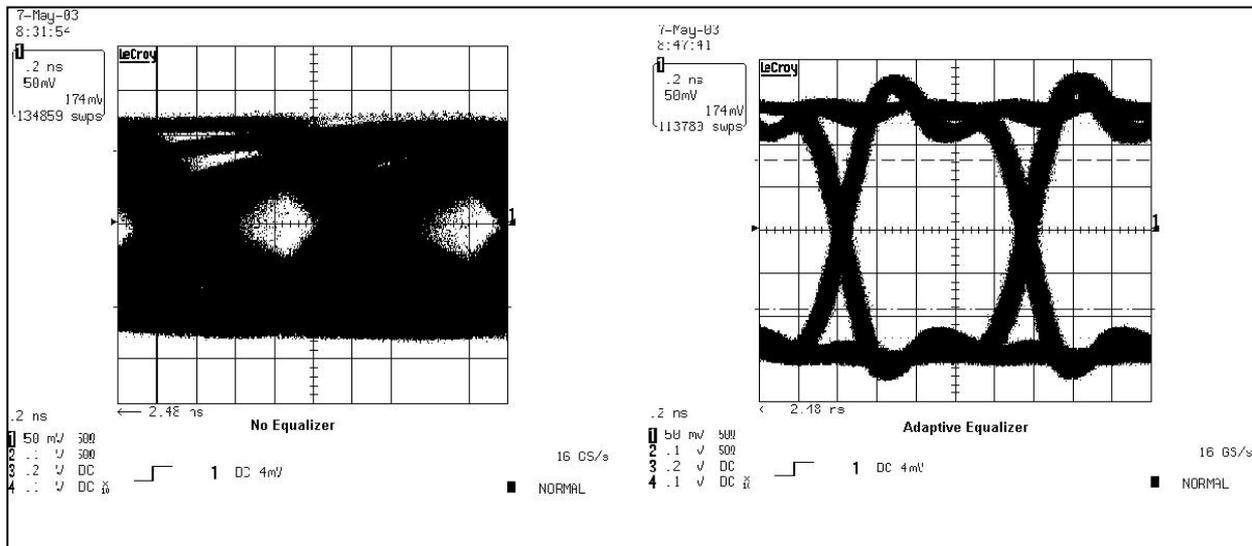
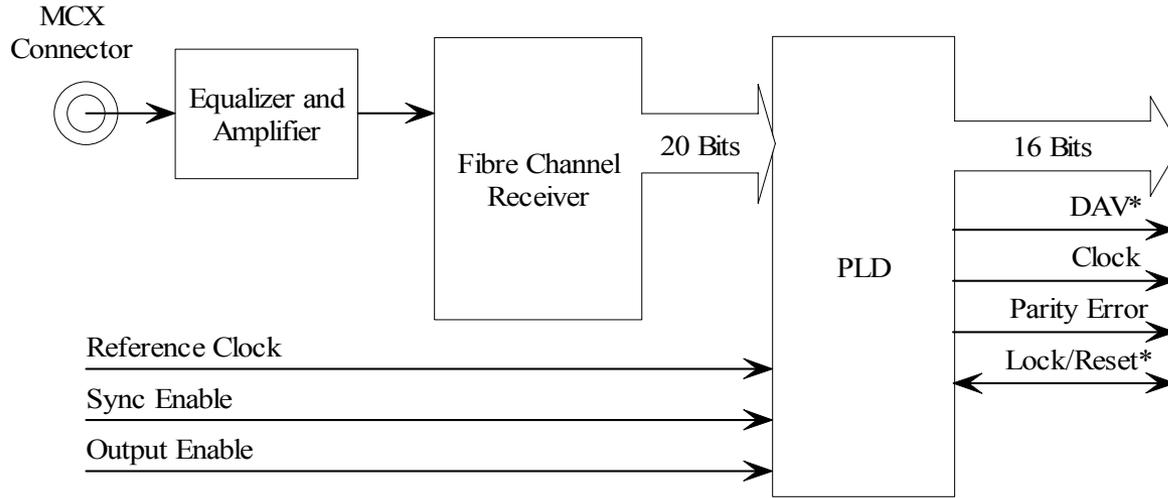


K28.5 are sent during synch gap only

Front-ends must ensure data from BC 7 is sent after synch gap

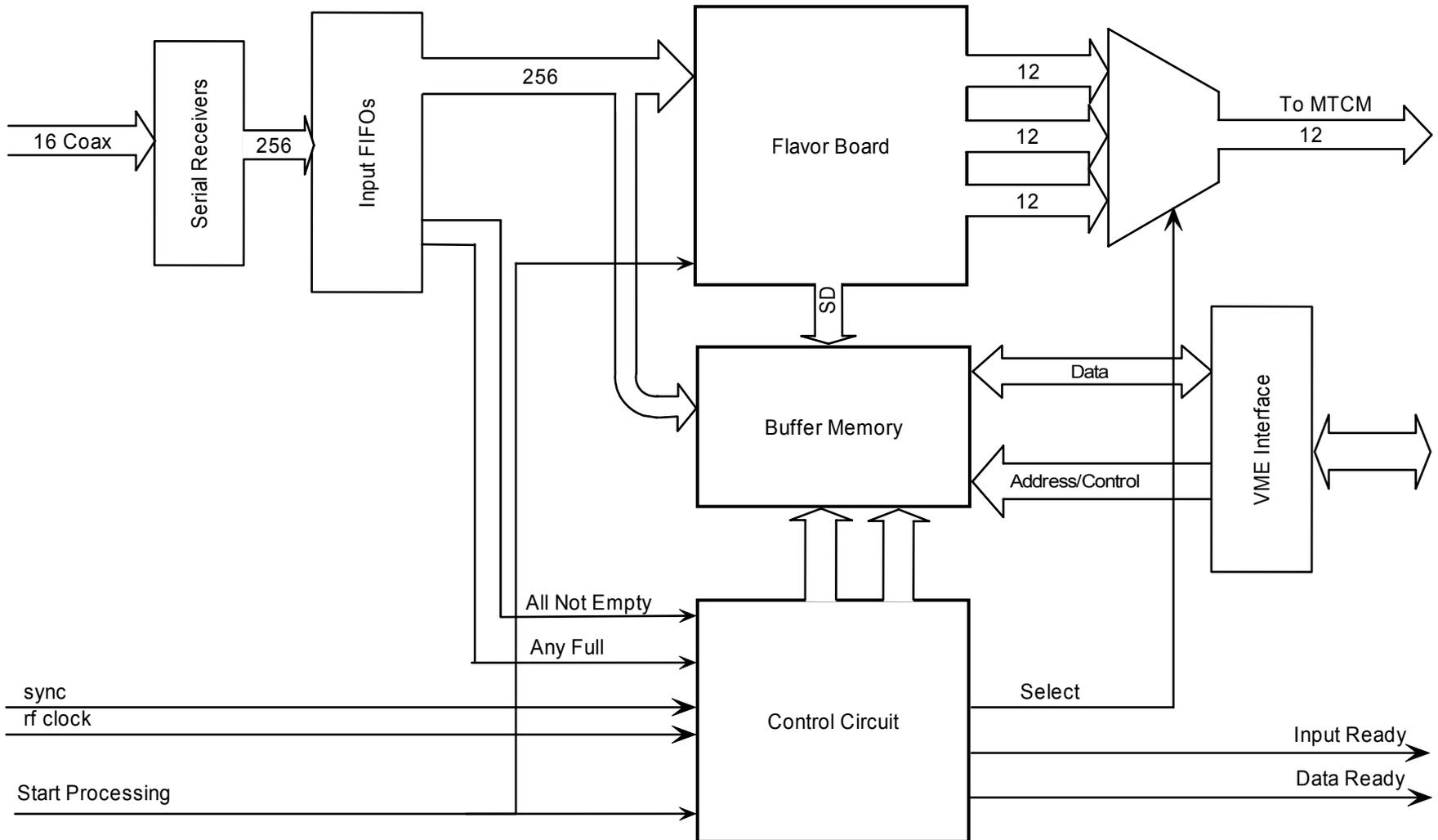


SLDB RECV





Synchronization, Input Ready, and Data Ready



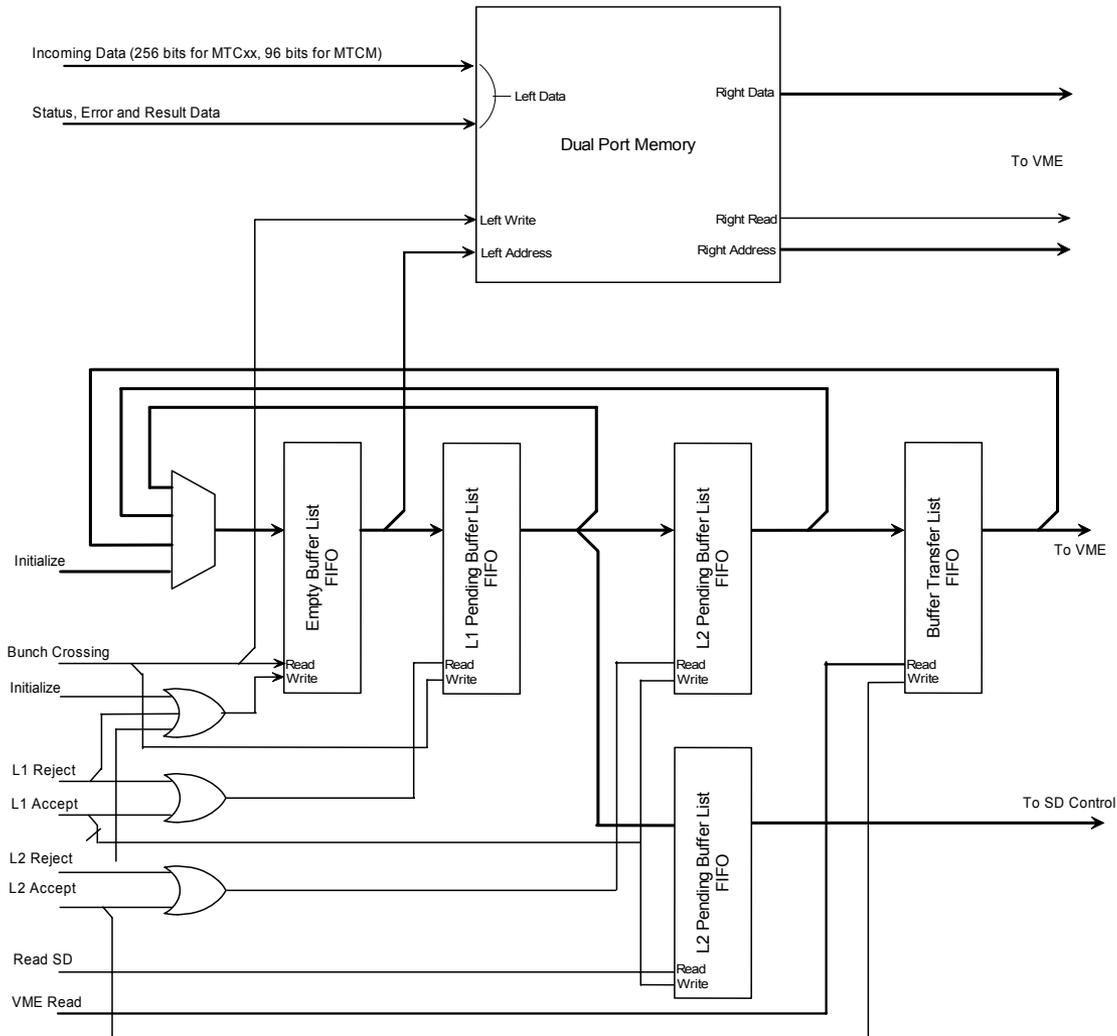


Input Ready and Data Ready

- IR == Issued by MTCxx when all non-masked input FIFO's are not MT
- DR == Issued by MTCxx when trigger decision FIFO is not MT
- Early problem was the open collector outputs resulted in a large RC time constant at MTCM
 - ◆ Now, IR only used for debugging front-ends
 - ◆ Now, DR sent through a shift register for meta-stability protection
 - ◆ We can set shift register length to determine Send Data from Data Ready after INIT
 - ◆ Thereafter we use an internal counter to create Send Data
 - ◆ Data Ready sets our local BC number = 7



Buffering





Buffering

- Data buffering pending L1, L2, L2 Transfer uses DPM and a set of FIFO's that keep track of DPM address
 - ◆ All addresses are initially in MT Buffer FIFO
 - ◆ As data comes in, it is written to DPM
 - ◆ DPM address gets written to L1 Pending Buffer FIFO
 - ◆ L1A causes address to be moved to L2 Pending Buffer FIFO
 - ◆ L1R causes address to be moved to MT Buffer FIFO
 - ◆ L2A causes address to be moved to Buffer Transfer FIFO
 - ◆ This address is then used by the MTCM to read the DPM in forming the L3 Data message
 - ◆ L2R causes the address to be moved to the MT Buffer FIFO



L1CalTrack Trigger Latency

- In order to achieve comfortable headroom
 - ◆ Increase the L1 trigger decision time by 4 BC's
 - ▲ Decisions due at 4092 ns from 3564 ns
 - ▲ Requires some modification to muon subsystem front ends
 - ▲ All other subsystems contain sufficient buffer depth
 - ◆ Bypass the MTCM in the trigger decision chain
 - ▲ Not needed since there is only one region (crate)
 - ▲ Serial link outputs added to the UFB



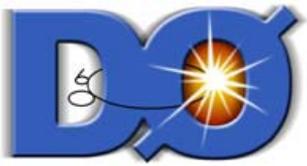
L1CalTrack Latency

ELEMENT	Δ TIME (ns)	TOTAL TIME (ns)
BC to ADF	650	650
ADF processing	1147	1797
TAB processing	728	2525
L1CTT processing	1592	
MTCxx processing	729	3254
MTM processing and transfer	589	3843
Run II upgrade L1 decision time		4092
Difference		-249



Inputs

- **L1CTT (10/80 sectors)**
 - ◆ 6 tracks per sector + parity
 - ◆ 16 bits / track = h layer position (6 bits), P_T (5 bits), curvature, CPS (3 bits)?, valid track
- **L1CAL (12/32 sectors)**
 - ◆ 4 phi sectors + 2 others (not null!!!) + parity
 - ◆ 16 bits / phi sector = 7 bits of jet threshold info, 7 bits of EM threshold info, 2 bits undefined
- **L1FPS (4/32 sectors)**
 - ◆ 3 (6?) FPS clusters
 - ◆ 16 bits / cluster = address (8 bits), U/V, mip, width (3 bits)



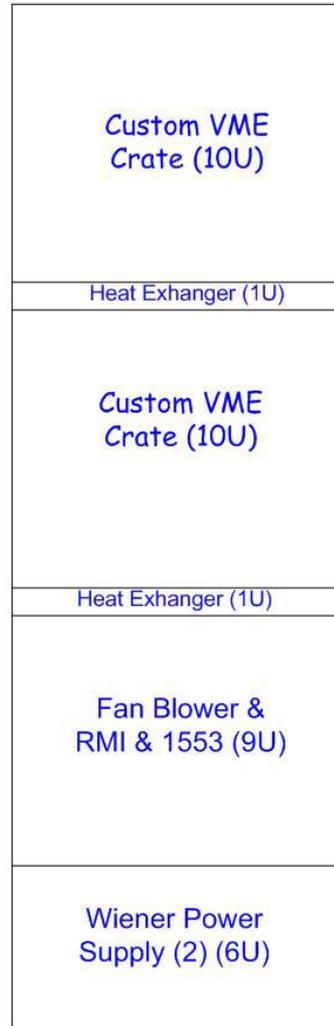
Cable Map

n	MTCxx	From	From
0	CTT0	MSPLIT	CTT0
1	CTT1	CTT1	
2	CTT2	CTT2	
3	CTT3	CTT3	
4	CTT4	CTT4	
5	CTT5	CTT5	
6	CTT6	CTT6	
7	CTT7	CTT7	
8	CTT8	CTT8	
9	CTT9	MSPLIT	CTT9
10	TAB0	TAB0	
11	TAB1	TAB1	
12	TAB2	TAB2	
13	FPS0	FPS0	
14	FPS1	FPS1	
15	FPS2	FPS2	
16	FPS3	FPS3	



MCH1 Rack Layout

L1CalTrack MCH1 Rack Layout





Manpower

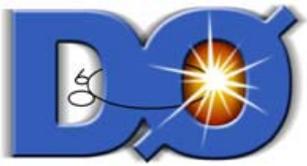
- Much of the manpower has experience designing/building/testing/running the L1MU trigger
 - ◆ Joel Steinberg - senior EE
 - ◆ Dan Tompkins - junior EE
 - ◆ Chris Leeman - undergrad technician
 - ◆ Semra Bekele - undergrad technician
 - ◆ Bryan Gmyrek - grad student
 - ◆ Ken Johns - faculty
 - ◆ Eric Varnes - faculty
 - ◆ Possibly some help from Eric Varnes' postdoc hire?



Cost Estimate

- **Cost Estimate**

- ◆ A detailed cost estimate is available
- ◆ Based on L1MU costs
- ◆ No overruns expected unless extra production cycle needed
- ◆ Need few k for miscellaneous projects (VME boundary scan PCB)
- ◆ Need few k for additional undergraduate technicians



Schedule

- Schedule

- ◆ A detailed, cost and resource-loaded schedule is available
- ◆ Change control needed to correctly update schedule
- ◆ A variety of things have slowed progress (physics analysis, loss of postdoc, shutdown, murky Run IIb plans, etc.)
- ◆ But all hardware should be finished if not tested and mostly installed in the next calendar year