

The DØ Silicon Track Trigger

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Abstract

We describe a trigger preprocessor to be used by the DØ experiment for selecting events with tracks from the decay of long-lived particles. This Level 2 impact parameter trigger utilizes information from the Silicon Microstrip Tracker to reconstruct tracks with improved spatial and momentum resolutions compared to those obtained by the Level 1 tracking trigger. It is constructed of VME boards with much of the logic existing in programmable processors. A common motherboard provides the I/O infrastructure and three different daughter boards perform the tasks of identifying the roads from the tracking trigger data, finding the clusters in the roads in the silicon detector, and fitting tracks to the clusters. This approach provides flexibility for the design, testing and maintenance phases of the project. The track parameters are provided to the trigger framework in twenty-five microseconds. The effective impact parameter resolution for high momentum tracks is 35 micrometers, dominated by the size of the Tevatron beam.

Key words:

PACS:

1 Introduction

With a collision rate of 2.3 MHz, the Run 2 DØ trigger must provide strong rejection of inconsequential collisions while at the same time maintaining high efficiency for those events that yield interesting physics. It must also provide a decision about each event fast enough to accommodate the 396 ns beam crossing time, while keeping the dead-time to a minimum.

The DØ Silicon Track Trigger (STT [1]), approved in 1999 as the newest addition to the DØ trigger system, is currently being commissioned. The STT performs precise reconstruction of charged particle tracks found in the Central Fiber Tracker (CFT) using data from the Silicon Microstrip Tracker (SMT). It provides the DØ trigger with the capability of selecting events containing tracks with large impact parameters. These tracks can be used to tag decays of long-lived particles, such as B or D hadrons or τ leptons. The presence of b

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quarks is a signature for Higgs boson decays and top quark decays. Events with b quarks are relevant for the understanding of mass generation and charge-parity violation. The CDF experiment makes use of a similar trigger, the Silicon Vertex Trigger [2].

2 The DØ Trigger

The DØ trigger has three levels. The first level locates significant energy deposits in the calorimeter and preprogrammed hit patterns in the Central Fiber Tracker and in the Muon Chambers. It also attempts to identify some spatial correlations between detector elements. The STT is a component of the second level, consisting of an array of dedicated preprocessors and a global Level 2 processor, which makes trigger decisions based on the information received from the preprocessors. Each major DØ detector component has a corresponding Level 2 preprocessor, the STT being the preprocessor for the Silicon Microstrip Tracker. The Level 2 global processor sends its output to the third level, which consists of a farm of computers that perform sophisticated reconstruction algorithms. To maintain a dead-time below 5%, the mean decision time for Level 2 must be under 100 μ s, with roughly 50 μ s for the preprocessors and 50 μ s for the global Level 2 decision.

3 The DØ Silicon Track Trigger

The STT utilizes information from the six cylindrical barrel sections of the SMT. These barrels comprise rectangular silicon detectors arranged in four concentric layers. All detectors have 50- μ m pitch silicon strips arranged axially (i.e., parallel to the beam line). The double-sided detectors also have 60–150- μ m pitch stereo strips at either 2° or 90° to the axial direction. For the purpose of the STT, the barrel sections are divided into 12 sectors, each 30° in azimuth. Because of overlaps between sectors, most high transverse momentum tracks hit detectors that belong to the same sector in all four layers, each 30° SMT sector can therefore be treated independently in the STT with a negligible loss.

For each event, the Level 1 CFT trigger sends a list of up to 46 tracks to each set of two neighboring 30° sectors of the STT. Due to the track curvature and impact parameter, these tracks could come from an angular region spanning approximately 80° centered on this sextant.

The STT finds clusters from the raw hits in the SMT. A ± 1 -mm road is defined around each track found by the Level 1 CFT trigger and the axial SMT clusters within the road are considered for the fit. The stereo clusters are stored for readout to Level 3. The STT track fit uses the hits in the inner and outer layers of the CFT as well as clusters on three or four layers of the SMT. The parameters for the fit for each road are provided to the Level 2 CFT trigger as well as to the global Level 3.

4 STT Hardware Design

The STT employs fast digital electronics based on custom-designed VME boards with on-board programmable processors. These boards are housed in six crates (see Fig. 1), each servicing one sextant of the SMT. Each crate has one crate controller, one CFT fiber road card, nine SMT trigger cards and two track fitting cards. Since these cards share common requirements for internal and external interfaces, they use a common motherboard, with the specific logic contained on daughter boards. Data are communicated between the cards using point-to-point links while control information uses dedicated backplane signals.

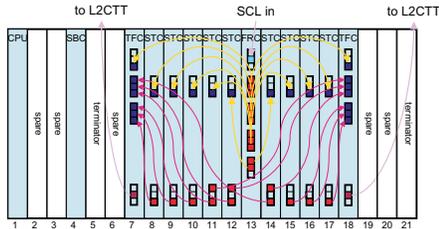


Fig. 1. Crate structure of STT.

4.1 Motherboard

The STT motherboard is a 9U \times 400-mm VME64x-compatible card containing three 33 MHz PCI busses to communicate between the logic daughter board and common input/output and data-buffering daughter boards. It has VIPA standard P0, P1 and P2 connectors. The J3/P3 connector is nonstandard to accommodate the backplane of the existing SMT readout system.

The unique logic for each of the three types of cards is located on individual PCI bus logic daughter boards, described in detail below. The three PCI busses connect the daughter boards to the crate backplane bus and to plug-in I/O interfaces containing Low Voltage Differential Signaling (LVDS) drivers (or receivers) and buffer logic. The LVDS Channel Link receiver/transmitter boards are grouped on two 32-bit wide PCI busses and transfer 32-bit words at a rate of 32 MHz. They are similar to PC-MIP (PCI Modules Industry Packs) standards and can therefore be installed on off-the-shelf carrier boards for testing and debugging applications. Six such cards can be mounted on each motherboard, as required by the daughter board.

The VME bus is used for readout to Level 3. The data produced by the daughter boards to be transmitted to Level 3 are stored in FIFOs on the daughter boards and then read out via the third PCI bus to dual-port memory buffers on separate daughter cards, the buffer controllers, that sit on each motherboard. A Fermilab standard Single Board Computer (SBC) card in each crate performs the readout of data to Level 3 via an ethernet connection.

The VME bus is also used for initialization and monitoring. A Universe II chip [3] on the motherboard, acting as a VME-to-PCI bus bridge, allows direct access to the daughter boards.

4.2 *Fiber Road Card*

The CFT Fiber Road Card (FRC) is composed of four functional elements implemented in three separate Altera FLEX10K Field Programmable Gate Arrays (FPGA) [4]. These include the trigger receiver, the road receiver, the trigger/road data formatter and the buffer manager.

The trigger receiver receives signals from the trigger framework via a special daughter card on the motherboard. This Serial Command Link (SCL) receiver mezzanine card provides clock, trigger and timing information, which is used by all cards in the crate. It is a DØ standard PC-MIP-like board (built at Fermilab). The trigger information is presented as 128 bits on two 64-pin connectors (J1 and J2 on the SCL receiver card). The FRC broadcasts any control signals to the other cards via a local bus on the J3 backplane. The trigger receiver also sends status information back to the trigger framework.

The road receiver receives track information sent to it from the Level 1 CFT trigger over an optical fiber link (using HP G-Link protocol). The data are received via a rear-mounted Fermilab standard VRB Transition Module (VTM). The trigger/road data formatter combines the road information with the relevant SCL data from the trigger framework and transmits the data blocks over LVDS links to the other cards in the STT. The logic for the trigger/road data formatter is combined with that of the road receiver and stored on a single Altera FLEX10K50 FPGA.

The buffer manager handles buffering and readout to Level 3. It manages the assignment of buffers on the buffer controller cards that store the data for each Level 1 accepted event for all the individual cards. Furthermore, the buffer manager decides if an event buffered by the other STT cards should be sent to Level 3 based on the Level 2 trigger information. The buffer manager communicates via the J3 backplane with buffer controller cards that are housed on each motherboard.

4.3 *Silicon Trigger Card*

The SMT Trigger Card (STC) receives the raw SMT data via a VTM. Each VTM has four fiber receivers, each servicing two SMT detector readout channels. Nine such cards are needed to process all the SMT channels in a sextant. In the STC, the hit data from the silicon strips are first compared to a lookup table (stored in on-board RAM) identifying bad strips. Data from good strips are then corrected for scale and offset using a second lookup table.

FPGAs programmed in VHDL find the centroids of any clusters of hit strips. A cluster is defined to be a group of contiguous strips with pulse heights above a given threshold. The cluster location is the pulse-height-weighted centroid of up to five strips centered around the strip with the largest pulse height. The axial (r - ϕ) clusters are matched to the tracks broadcast by the FRC using a third lookup table and then transmitted to the track fitting cards via point-to-point LVDS links. Both axial and stereo clusters are buffered on-board for VME readout to Level 3.

4.4 Track Fit Card

There are two Track Fit Cards (TFC) in each crate, one for each 30° sector of the SMT. The road information is received from the FRC on LVDS links using the STT standard PC-MIP receiver cards. For a typical event, the highest-occupancy sextant contains six roads. The TFC uses eight TI-TMS320C6203 [5] 300 MHz integer Digital Signal Processors (DSP) for fitting tracks to these roads in parallel. The fitting algorithm is programmed in C. Three Altera FLEX10K100 FPGAs supply the control logic on the board. The hardware definition for the road information is transformed into physical coordinates using lookup tables stored in the memory on the DSPs.

Each TFC receives axial clusters from approximately half of the STCs over LVDS links and the hardware address for each cluster is transformed into r - ϕ coordinates using a lookup table stored in on-board RAM.

The cluster in each layer that is closest in ϕ to the center of the road defined by the origin of the detector and the hits in the innermost (A) and outermost (H) layers of the CFT is selected (see Fig. 2). By requiring clusters in only three out of four SMT layers, the track reconstruction efficiency increases by 15% to around 85% for tracks with transverse momentum above 1.5 GeV. The track

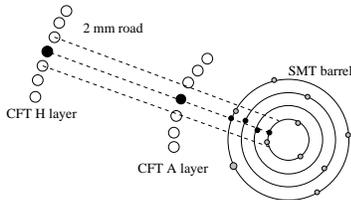


Fig. 2. Diagram depicting the cluster selection algorithm.

parameters in the r - ϕ plane are determined by fitting a linear parameterization to the SMT clusters and the CFT hits, with the form $\phi(r) = b/r + \kappa r + \phi_0$, where b is the impact parameter with respect to the detector origin, κ is the curvature of the track and ϕ_0 is the direction of the track at the point of closest approach. The track parameters b , κ and ϕ_0 are obtained from the ϕ values of the hits in the SMT and CFT layers by multiplying the ϕ vector with a precomputed matrix that is stored in a lookup table in on-board RAM.

The TFC can correct the impact parameter for beam position offsets from the detector origin. To this end, the beam position, (r_B, ϕ_B) , will be determined at the beginning of each data-taking run (of 4 hour maximum duration) from a sample of several hundred events by a program running on a dedicated computer and then made available to the Level 2 trigger framework. It is then downloaded to the TFC and used for the remainder of the data-taking run. The TFC outputs the track parameters and the fit χ^2 as well as minimal additional information regarding the fit and cluster selection. The data are transmitted to the Level 2 trigger. It is also buffered in a buffer controller card for VME readout to Level 3. These results are used by the Level 2 trigger framework for selecting events containing tracks of large impact parameter.

Such tracks indicate the presence of long-lived particles, such as b quarks or τ leptons. The impact parameter resolution of $35\ \mu\text{m}$ is dominated by a $30\text{-}\mu\text{m}$ component associated with the cross-section of the proton-antiproton beam and a $15\text{-}\mu\text{m}$ component associated with the resolution of the SMT, as determined by simulations.

5 Conclusions

The STT is a novel device that measures the impact parameters of displaced tracks, enabling the selection of large samples of events that contain b quarks and other long-lived particles in the presence of enormous backgrounds. The STT is currently being commissioned and will be operating shortly.

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