

# An Impact Parameter Trigger for the DØ Experiment

Huishi Dong, on behalf of the DØ Collaboration

**Abstract**—We describe a trigger to be used by the DØ Experiment for selecting events with tracks having a large impact parameter with respect to the collision point. This device utilizes information from the Silicon Microstrip Tracker to provide improved spatial and momentum resolutions for charged particles. It is constructed of custom digital boards with programmable processors. A common motherboard provides I/O and buffer management and three different daughter boards perform the tasks of identifying the roads from the tracking trigger data, finding the clusters in the roads in the silicon detector, and fitting tracks to the clusters. This approach provides flexibility for the design, testing and maintenance phases of the project. A  $\sim 60 \mu\text{m}$  impact parameter resolution is provided to the trigger framework in less than fifty microseconds. We present preliminary results from the first weeks of test run of this trigger integrated with the DØ trigger system.

**Index Terms**—Trigger system, Tracking system, Silicon detectors, Impact parameter.

## I. INTRODUCTION

TRACKS with large impact parameters can be used to tag the decays of long-lived particles, such as B or D hadrons or  $\tau$  leptons. These particles bear essential information for many interesting physics topics, e.g. the presence of b quarks is a signature for Higgs boson decays and top quark decays, and events with b quarks are relevant to the understanding of mass generation and CP violation. The ability to efficiently single out b quark events will considerably benefit solving these fundamental particle physics problems.

The DØ Silicon Track Trigger (STT) [1], approved in 1999 as the newest addition to the upgraded DØ trigger system, provides the DØ trigger system with the capability of selecting events containing tracks with large impact parameters. It performs high precision online reconstruction of charged particle tracks found in the Central Fiber Tracker (CFT) by utilizing much finer spatial resolutions of the Silicon Microstrip Tracker (SMT).

## II. DØ TRIGGER AND TRACKING SYSTEM

The Tevatron is delivering proton-anti-proton collisions at a rate of 2.53 MHz, while the data acquisition rate is only about 100 Hz. To bring down the data rate, the DØ has a three level trigger system, and Level 1 has pipelined buffers to absorb rate fluctuations. The Level 1 trigger must make a decision on each event fast enough to accommodate the 396 ns beam crossing time to reject the inconsequential collisions

while keeping the dead time to a minimum and maintaining high efficiency for those events that yield interesting physics. To accomplish this goal, the Level 1 trigger system is implemented in hardware and locates significant energy deposits in the calorimeter and preprogrammed hit patterns in the CFT, the Central Preshower (CPS), the Forward Preshower (FPS) and in the Muon Chambers. It also attempts to identify limited spatial correlations between detector elements. The Level 2 trigger consists of an array of dedicated preprocessors and a global Level 2 processor. Each major DØ detector component has a corresponding Level 2 preprocessor, and the STT is a preprocessor for the SMT. The global processor makes trigger decisions based on the information received from the preprocessors and sends its output to the third level only for the interesting events. To maintain a dead time below 1%, the mean decision time for Level 2 must be under  $100 \mu\text{s}$  with roughly  $50 \mu\text{s}$  for the preprocessors and  $50 \mu\text{s}$  for the global Level 2 decision. The Level 3 consists of a farm of computers that perform sophisticated reconstruction algorithms.

The DØ charged particle tracking system is mainly composed of three components: a superconducting solenoid, the CFT and the SMT. The solenoid, surrounding the CFT and the SMT, provides a 2 Tesla magnetic field to allow the measurement of the momenta of charged particles. The CFT consists of  $\sim 80,000$  1mm scintillating fibers mounted on eight carbon-composite cylinders at radii ranging from 20 to 55 cm. The position resolution is about  $250 \mu\text{m}$ . Although the very fast readout speed of the CFT and the small number of readout channels make it possible for the Level 1 Central Track Trigger (CTT) to use CFT data to select good charged particle tracks and send these Level 1 tracks to the Level 2 trigger. The resolution of the CFT is insufficient to provide a precise impact parameter measurement. On the other hand, the SMT consists of silicon disks and barrels formed into 6 disk/barrel modules. These barrels comprise rectangular silicon detectors arranged in four concentric layers. All detectors have  $50 \mu\text{m}$  pitch silicon strips arranged parallel to the beam line as well as in a stereo angle. In total there are about 793,000 readout channels. It provides a position resolution of about  $10 \mu\text{m}$ , which is good enough to provide a precise impact parameter but the large number of readout channels and the readout speed of silicon detector prevent it from being used in the Level 1 trigger.

The STT, combining SMT and CFT information together, can solve this dilemma. The STT uses the CFT track as the seed of a road that is extrapolated into the SMT. Silicon clusters within this road can then be included in the track fit, in addition to the original CFT information.

As shown in Fig. 1, for each event, the Level 1 CTT sends

Manuscript received October 31, 2003. This work is supported by the DOE/NSF.

H. Dong is with the State University of New York at Stony Brook.

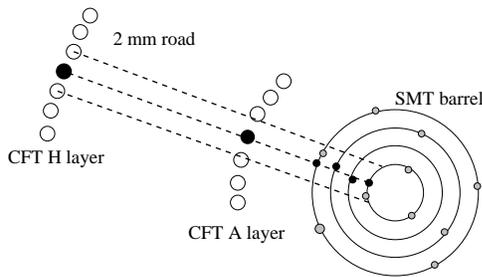


Fig. 1. The FRC roads forming and the SMT hits selection in STT.

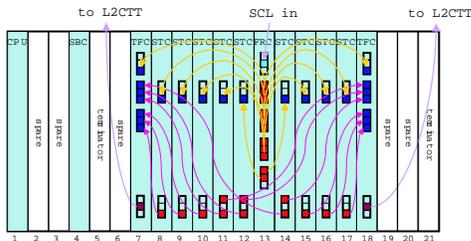


Fig. 2. The layout of the STT crate.

a list of up to 46 tracks to each STT. A  $\pm 2\text{mm}$  road is defined around each track and only the SMT clusters within the road are considered for the track fitting. In doing this the number of SMT clusters considered for each track fit is dramatically reduced so that the fitting can be done fast enough for the Level 2 trigger system. The STT uses the hits in the innermost and outermost layers of the CFT as well as clusters on three or four layers of the SMT to perform the track fitting, so the STT can provide fine enough impact parameters resolution. The fitting result of each road are sent to the Level 2 CTT as well as to the global Level 3 trigger system.

For the purpose of the STT, the SMT barrel sections are divided into 12 sectors, each roughly  $30^\circ$  in azimuth. Because of overlaps between sectors, most high transverse momentum tracks hit detectors that belong to the same sector in all four layers. Each  $30^\circ$  SMT sector can therefore be treated independently in the STT with a negligible loss.

### III. STT HARDWARE DESIGN

The STT uses custom-designed VME boards with on-board programmable processors. Six identical crates house these boards, each serving one of the SMT sextants. Each crate has one crate controller, one Single Board Computer, one Fiber Road Card, nine Silicon Trigger Cards and two Track Fitting Cards (See Fig. 2). Since these cards share common requirements for internal and external interfaces, they use a common motherboard, with the specific logic contained on daughter boards. Data are communicated between the cards using point-to-point serial links. Control information uses dedicated backplane signals.

#### A. Motherboard

The STT motherboard is a  $9U \times 400\text{-mm}$  VME64x-compatible card containing three independent 33 MHz PCI busses to communicate between the logic daughter board and common input/output and data-buffering daughter boards. It has VIPA standard P0, P1 and P2 connectors. The J3/P3 connector is nonstandard to accommodate the backplane of the existing SMT readout system.

The logic specific to the FRC, the STC and the TFC is located on individual PCI bus logic daughter boards, described in detail below. The three PCI busses connect the daughter boards to the crate backplane bus and to point-to-point serial links. There are two independent PCI-PCI bridges for simultaneous PCI-PCI data transmitting.

The VME bus is used for readout to Level 3 as well as for initialization and monitoring. A Universe II chip on the motherboard, acting as a VME-to-PCI bus bridge, allows crate controller CPU access to the daughter boards.

#### B. Internal/external data transmitting

The point-to-point serial links for data communication between the three types of logic daughter cards use Low-Voltage Differential Signaling (LVDS) drivers. The LVDS receiver/transmitter boards (LRB/LTB) are grouped on two 32-bit-wide PCI busses and transfer 32-bit words at a rate of 32 MHz. They approximately conform to PCI Modules Industry Packs (PC-MIP) standards and can therefore be installed on standalone carrier boards for testing and debugging applications. Up to six I/O cards can be mounted on each motherboard, as required by the daughter board.

The STT sends its output to the Level 2 trigger system via the hotlink transmitting card which is also seated on PC-MIP interfaces of the mother board. Each daughter board also produces and sends data to Level 3. These data are stored in FIFOs on the daughter boards and then read out via the third PCI bus to dual-port memory buffers on separate daughter cards—the buffer controllers (BC)—that sit on each motherboard. A DØ standard Single Board Computer (SBC) card in each crate reads data from the buffer controller and transfers to the Level 3 via an ethernet connection.

#### C. Fiber road card

The Fiber Road Card (FRC) is composed of four functional elements implemented in three separate Altera FLEX10K Field Programmable Gate Arrays (FPGA). These include the trigger receiver, the road receiver, the trigger/road data formatter and the buffer manager. [2]

The trigger receiver receives DØwide synchronization signals from the trigger framework via a special daughter card—the Serial Command Link (SCL) card—on the motherboard. It is a DØ standard PC-MIP-like board (built at Fermilab). The trigger information is presented as 128 bits on two 64-pin connectors. The FRC broadcasts a limited subset of these control signals to the other cards via a local bus on the J3 backplane. The

trigger receiver also sends status information back to the trigger framework.

The road receiver logic receives track information from the Level 1 CTT via an optical fiber link (using HP G-Link protocol). The data are received by a rear-mounted Fermilab standard VRB Transition Module (VTM) and transmitted through the back plane via J3 pins.

The trigger/road data formatter combines the road information with the relevant SCL data from the trigger framework and transmits the data to the other logic daughter cards. The logic for the trigger/road data formatter is combined with that of the road receiver and stored on a single Altera FLEX10K50 FPGA.

The buffer manager handles buffering and readout to Level 3. It manages the assignment of buffers on the BC's for Level 1 accepted events for all the individual STT logic cards. The buffer manager decides if an event buffered by the other STT cards should be sent to Level 3 based on the Level 2 trigger information. The buffer manager communicates via the J3 backplane with BC's.

#### D. Silicon trigger card

The Silicon Trigger Card (STC) receives the raw SMT data via a VTM. Each VTM has four fiber receivers, each of which receives two SMT detector readout channels. Nine such cards are needed to process all the SMT channels in a sextant. The SMT uses a Xilinx Virtex XCV812E chip programmed in VHDL for its main functionalities and 3 Altera ACEX EP1K30 chips for PCI interfaces controller.

In the STC, the hit data from the silicon strips are first compared to a lookup table (stored in on-board RAM) identifying bad strips. Data from good strips are then corrected for gain and pedestal by multiplication and subtraction. Then the FPGA find the clusters of hit strips. A cluster is a group of contiguous strips with pulse heights above a given threshold. The cluster location is determined by the pulse-height-weighted centroid of up to five strips. The resulting clusters are matched to the tracks broadcasted by the FRC using a second lookup table and transmitted to the track fitting cards. Clusters are also read out to Level 3 via the BC.

#### E. Track fit card

There are two Track Fit Cards (TFC) in each crate, one for each  $30^\circ$  sector of the SMT. The FRC road and the SMT cluster information are received using the STT standard PC-MIP receiver cards. The hardware road and cluster information is translated into physical coordinates ( $r - \phi$ ) by lookup tables stored in on-board RAM. Eight TI-TMS320C62033 300MHz integer Digital Signal Processors (DSP) are used by each TFC to perform track fitting. The fitting algorithm is programmed in C. Three Altera FLEX10K100 FPGAs supply the control logic on the board.

The cluster in each SMT layer that is closest in  $\phi$  to the center of the road represented by a CTT track is chosen by the TFC for the fit. The hits on the CFT innermost (A) and

outermost (H) layers are also used. (see Fig. 1). The fit will not be performed if there are hits in less than three different SMT layers within a CTT road. When there are only three SMT layers that contain clusters, the TFC performs a 1-pass fit. The TFC may perform a 2-pass fit when there are 4 SMT layers that have chosen clusters: first it fits with the 2 CFT hits and 4 SMT clusters. If the initial fit quality is poor, the hit that introduces the largest contribution to the  $\chi^2$  is discarded and the track is refit using the remaining three SMT hits. By requiring clusters in only three out of four SMT layers, the track reconstruction efficiency is increased by 15% to around 85% for tracks with transverse momentum above 1.5 GeV.

The track parameters in the  $r - \phi$  plane are determined by fitting with the form  $\phi(r) = b/r + \kappa r + \phi_0$ , where  $b$  is the impact parameter with respect to the detector origin,  $\kappa$  is the curvature of the track and  $\phi_0$  is the direction of the track at the point of closest approach. [3] The track parameters  $b, \kappa$  and  $\phi_0$  are obtained from the  $\phi$  values of the hits in the SMT and CFT layers by multiplying the  $\phi$  vector with a precomputed matrix that is stored in a lookup table in on-board RAM.

The TFC can correct for beam position offsets from the detector origin. The beam position ( $r_B, \phi_B$ ) will be determined at the beginning of each data-taking run (of 4 hour maximum duration) from a sample of several hundred events by a program running on a dedicated computer and then made available to the Level 2 trigger framework. It is then downloaded to the TFC and used for the remainder of the data-taking run.

The TFC outputs the track parameters and the fit  $\chi^2$  as well as additional geometric information regarding to the fitting and cluster selection. The data are transmitted to the Level 2 trigger where these results are used for selecting events containing tracks of large impact parameter. It is also buffered in a buffer controller card for VME readout to Level 3.

## IV. STT PERFORMANCE

The STT is now in the final stage of commissioning. All components for the six crates are at hand. Five of them have been fully-populated, and are fully functional; one is reserved for testing purposes. Two of the fully functional crates were successfully put into the DØ trigger system and read out during normal physics data taking runs. A package fully simulating the STT is also available.

Fig. 3 shows the TFC fitting time distribution during one of the physics runs. The TFC uses most of the STT decision time, and the mean TFC fitting time is within the requirement of  $50 \mu\text{s}$  for Level 2 preprocessors. The three spikes in the distribution are due to the rejection of tracks with less than three SMT hits and the 2-pass fitting procedure of the TFC.

Fig. 4 shows the intrinsic STT impact parameter resolution distribution as a function of the track  $p_T$  determined by simulations. The STT impact parameter resolution of  $60 \mu\text{m}$  is dominated by a  $30 \mu\text{m}$  component associated with the cross-section of the proton-antiproton beam, a  $15 \mu\text{m}$  component associated with the resolution of the SMT, and a  $p_T$  dependent component arising from multiple Coulomb scattering.

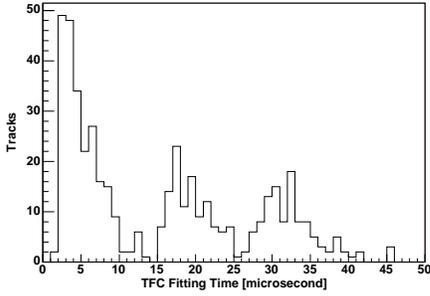


Fig. 3. The TFC fitting time recorded during a portion of physics run.

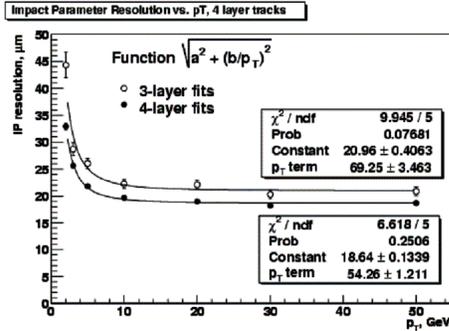


Fig. 4. The STT intrinsic impact parameter resolution vs. transverse track momentum  $p_T$ .

Fig. 5 shows the STT simulation on data from one of the physics runs which had the STT crates in. The beam spot corrections were applied to the data. A cut on tracks with  $\chi^2/\text{dof} < 4$  is applied to pick up the good fits. The  $\sim 1$  unit Gaussian width means the impact parameter resolution is well defined. The tails of the distribution are being studied.

## V. CONCLUSIONS

The STT is a novel device that measures the impact parameters of displaced tracks, enabling the selection of large samples of events that contain b quarks and other long lived particles in the presence of enormous backgrounds. The STT is currently being commissioned and will be operating shortly.

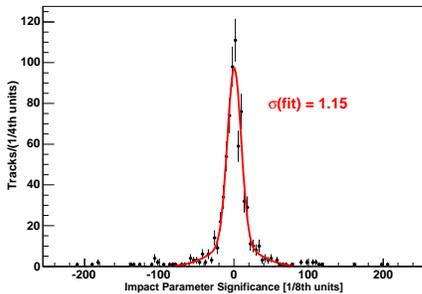


Fig. 5. The impact parameter significance distribution for a physics run.

## ACKNOWLEDGMENT

We thank the staffs at Fermilab and collaborating institutions. Major funding for this project came from the Department of Energy and from the National Science Foundation under NSF Major Research Instrumentation (MRI) Program Award No. 9977659, 9/1/1999. We would also like to acknowledge in kind contributions by the Altera and Xilinx Corporations.

## REFERENCES

- [1] DØ Note 3516, *A Silicon Track Trigger Processor for DØ*, <http://www-d0.fnal.gov/trigger/st/sttdesign/uli/tdr.980318.ps>
- [2] Georg Steinbrück, *The DØ Silicon Track Trigger*, Nucl. Instr. and Meth. A511 (2003) 145-149
- [3] Huishi Dong, John Hobbs, Charles Pancake, Wendy Taylor, *The DØ Silicon Track Trigger Track Fitting Design*, <http://sbhept.physics.sunysb.edu/~hobbs/12st/tfc.pdf>