

An Impact Parameter Trigger for the DØ Experiment

Wendy Taylor¹ for the DØ Collaboration

¹State University of New York, Stony Brook, NY 11794

Abstract

We describe a trigger preprocessor to be used by the DØ experiment for selecting events with tracks from the decay of long-lived particles. This Level 2 impact parameter trigger utilizes information from the Silicon Microstrip Tracker to reconstruct tracks with improved spatial and momentum resolutions compared to those obtained by the Level 1 tracking trigger. It is constructed of VME boards with much of the logic existing in programmable processors. A common motherboard provides the I/O infrastructure and three different daughter boards perform the tasks of identifying the roads from the tracking trigger data, finding the clusters in the roads in the silicon detector, and fitting tracks to the clusters. This approach provides flexibility for the design, testing and maintenance phases of the project. The track parameters are provided to the trigger framework in twenty-five microseconds. The impact parameter is measured with a thirty-five micron resolution.

I. INTRODUCTION

During Run II, after the upgrade presently in progress, the Fermilab Tevatron $\bar{p}p$ collider will operate at a higher center-of-mass energy ($\sqrt{s} = 1.96$ TeV) with a ten-fold increase in collision rate (7.6 MHz) compared to Run I. During the first two years of Run II, the Tevatron is expected to deliver 2 fb^{-1} of data, or twenty times the integrated luminosity of Run I. The Run II DØ trigger must provide strong rejection of inconsequential collisions while at the same time maintaining high efficiency for those events that yield interesting physics. It must also provide a decision about each event fast enough to accommodate the 132 ns beam crossing time, while keeping the dead-time to a minimum.

The DØ Silicon Track Trigger (STT [1]), recently approved as the newest addition to the DØ trigger system, is currently being designed. The STT performs precise reconstruction of charged particle tracks found in the Central Fiber Tracker (CFT) using data from the Silicon Microstrip Tracker (SMT) (see Figure 1). It provides the DØ trigger with the capability of selecting events containing tracks with large impact parameters. These tracks can be used to tag decays of long-lived particles, such as B hadrons or τ leptons. The presence of b quarks is a signature for Higgs boson decays and top quark decays. Events with b quarks are relevant for the understanding of mass generation and charge-parity violation.

II. THE DØ TRIGGER

The DØ trigger has three levels. The first level locates clusters of energy in the calorimeter and preprogrammed hit patterns in the Central Fiber Tracker and in the Muon Chambers. It also attempts to identify some spatial correlations between detector elements. The STT is a component of the second level,

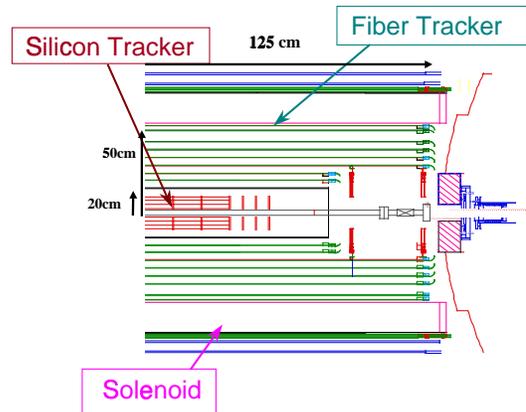


Figure 1: Cross section of half of the DØ tracking system.

consisting of an array of dedicated preprocessors and a global Level 2 processor, which makes the trigger decision based on the information received from the preprocessors. Each major DØ detector component has a corresponding Level 2 preprocessor, the STT being the preprocessor for the Silicon Microstrip Tracker. These preprocessors send their outputs to the third level, which consists of a farm of computers that perform sophisticated reconstruction algorithms. To maintain a dead-time below 5%, the mean decision time for Level 2 must be under $100 \mu\text{s}$, with roughly $50 \mu\text{s}$ for the preprocessors and $50 \mu\text{s}$ for the global Level 2 decision.

III. THE DØ SILICON TRACK TRIGGER

The STT utilizes information from the six cylindrical barrel sections of the SMT. These barrels comprise rectangular silicon detectors arranged in four concentric layers. All detectors have $50\text{-}\mu\text{m}$ pitch silicon strips arranged axially (i.e., parallel to the beam line). The double-sided detectors also have $60\text{--}150\text{-}\mu\text{m}$ pitch stereo strips at either 2° or 90° to the axial direction. For the purpose of the STT, the barrel sections are divided into six sectors, each 60° in azimuth. Since most high transverse momentum tracks hit detectors that belong to the same sector in all four layers, each 60° SMT sector can be treated independently in the STT with a negligible loss.

The Level 1 CFT trigger sends a list of up to 46 tracks to each sector of the STT for each event. Due to the track curvature and impact parameter, these tracks could come from an angular region spanning approximately 80° centered on the 60° SMT sector.

The STT finds clusters from the raw hits in the SMT. A $\pm 1\text{-mm}$ road is defined around each track found by the Level 1 CFT trigger and the axial SMT clusters within the road are considered for the fit. The stereo clusters are stored for readout to Level 3.

The STT track fit uses the hits in the inner and outer layers of the CFT as well as clusters on three or four layers of the SMT. The parameters for the fit for each road are provided to the Level 2 CFT trigger as well as to the global Level 3.

IV. STT HARDWARE DESIGN

The STT employs fast digital electronics based on custom-designed VME boards with on-board programmable processors. These boards are housed in six crates, each servicing one 60° sector of the SMT. Each crate has one crate controller, one CFT fiber road card, nine SMT trigger cards and two track fitting cards. Since these cards share common requirements for internal and external interfaces, they use a common motherboard, with the specific logic contained on daughter boards. Data is communicated between the cards using point-to-point links while control information uses dedicated backplane signals. This design incorporates as much of the standard DØ and Fermilab hardware as possible, thereby reducing the requirements for new hardware development and making the STT easier to maintain as a part of the entire DØ trigger system.

A. Crate Controller

The VME crate is controlled by a Motorola MVME2302 card, with a 200 MHz Power PC processor. The crate controller is in charge of initializing the other cards in the crate at power-up. All of the information needed for the functionality of the various boards is downloaded through the crate controller to the local memory on the boards. The crate controller is also in charge of gathering information to monitor the various cards.

B. Motherboard

The STT motherboard is a 9U×400 mm VME64x-compatible [2] card containing three 33 MHz PCI [3] busses to communicate between the logic daughter board and common input/output and data-buffering daughter boards. It has VIPA [4] standard P0, P1 and P2 connectors. The J3/P3 connector is non-standard to accommodate the backplane of the existing SMT readout system.

The unique logic for each of the three types of cards is located on individual PCI bus Mezzanine Card (PMC [5]) logic daughter boards, described in detail below. The three PCI busses connect the daughter boards to the crate backplane bus and to plug-in I/O interfaces containing Low Voltage Digital Signal (LVDS) drivers (or receivers) and buffer logic. The LVDS Channel Link receiver/transmitter boards are grouped on two 32-bit wide PCI busses and support a minimum 32-bit word point-to-point transfer speed of 26.5 MHz. They are fully compliant with PC-MIP (PCI Modules Industry Packs [6]) standards and can therefore be installed on off-the-shelf carrier boards for testing and debugging applications. Six such cards can be mounted on each motherboard, as required by the daughter board.

The VME bus is used for readout to Level 3. The data produced by the daughter boards to be transmitted to Level 3 is

stored in FIFOs on the daughter boards and then read out via PCI bus 3 to a dual-port memory buffer on the motherboard. A Fermilab standard VME Buffer Driver (VBD) card in each crate performs the readout of data to Level 3.

The VME bus is also used for initialization and monitoring. A Universe II chip [7] on the motherboard, acting as a VME-to-PCI bus bridge, allows direct access to the daughter boards.

C. Fiber Road Card

The CFT Fiber Road Card (FRC) is composed of four functional elements implemented in three separate Altera FLEX10K Field Programmable Gate Arrays (FPGA) [8]. These include the trigger receiver, the road receiver, the trigger/road data formatter and the buffer manager.

The trigger receiver receives signals from the trigger framework via a special daughter card on the motherboard. This Serial Command Link (SCL) receiver mezzanine card [9] provides clock, trigger and timing information, which is used by all cards in the crate. It is a DØ standard PC-MIP-like board. A separate set of connectors is provided to make the pin-out compatible with the PC-MIP standard. The trigger information is presented as 128 bits on two 64-pin connectors (J1 and J2 on the SCL receiver card). The FRC broadcasts any control signals to the other cards via a local bus on the J3 backplane. The trigger receiver also sends status information back to the trigger framework.

The road receiver receives track information sent to it from the Level 1 CFT trigger over an optical fiber link (using HP G-Link protocol). The data is received via a rear-mounted Fermilab standard VRB Transition Module (VTM [10]). The VTMs accept the data from Fermilab standard VME Readout Buffer (VRB [11]) cards, which receive the data directly from the CFT. These tracks are used to define a road in the SMT for filtering the clusters.

The trigger/road data formatter combines the road information with the relevant SCL data from the trigger framework and transmits the data blocks over LVDS links to the other cards in the STT. The logic for the trigger/road data formatter is combined with that of the road receiver and stored on a single Altera FLEX10K50 FPGA.

The buffer manager handles buffering and readout to Level 3. It manages the assignment of buffers that store the data for each Level 1 accepted event on all the individual cards. Furthermore, the buffer manager decides if an event buffered by the other STT cards should be sent to Level 3 based on the Level 2 trigger information. The buffer manager communicates via the J3 backplane with the local buffers that are included on each motherboard.

D. Silicon Trigger Card

The SMT Trigger Card (STC) receives the raw SMT data via a VTM. Each VTM has four fiber receivers, each servicing two SMT detector readout channels. Nine such cards are needed to process all the SMT channels in a 60° sector. In the STC, the hit data from the silicon strips is first compared to a

lookup table (stored in on-board RAM) identifying bad strips. Data from good strips is then corrected for scale and offset using a second lookup table. Updated versions of these lookup tables are downloaded to the STC when necessary.

FPGAs programmed in VHDL find the centroids of any clusters of hit strips. A cluster is defined to be a group of contiguous strips with pulse heights above a given threshold. The cluster location is the pulse-height-weighted centroid of the five strips centered around the strip with the largest pulse height. The axial (r - ϕ) clusters are matched to the tracks broadcast by the FRC using a third lookup table and then transmitted to the track fitting cards via point-to-point LVDS links. Both axial and stereo clusters are buffered on-board for VME readout to Level 3.

E. Track Fit Card

There are two Track Fit Cards (TFC) in each crate, one for each 30° sector of the SMT. The road information is received from the FRC on LVDS links using the STT standard PC-MIP receiver cards. For a typical event, the highest-occupancy sector contains six roads. The TFC uses eight TI-TMS320C6203 [12] 300 MHz integer Digital Signal Processors (DSP) for fitting tracks to these roads in parallel. Three Altera FLEX10K100 FPGAs supply the control logic on the board. For a given event, each road from the FRC is assigned to a DSP. The hardware definition for the road information is transformed into physical coordinates using lookup tables stored in the memory on the DSPs.

Each TFC receives axial clusters from approximately half of the STCs over LVDS links and the hardware address for each cluster is transformed into r - ϕ coordinates using a lookup table stored in on-board RAM. The road data and r - ϕ coordinates are temporarily stored in the input dual-port memory (IDPM) until the event has been entirely loaded. Then the SMT clusters are farmed out to the appropriate DSP to be processed. The track fitting algorithm is programmed in C and downloaded onto the DSPs before operation. An updated version of the algorithm can also be downloaded during Run II if necessary.

The cluster in each layer that is closest in ϕ to the center of the road defined by the origin of the detector and the hits in the innermost (A) and outermost (H) layers of the CFT is selected (see Figure 2). If the resulting fit is poor, the worst cluster from a four-layer track can be dropped and the fit can be recomputed with the remaining three clusters (a two-pass fit). Alternatively, a track can be formed when only three of the four layers have clusters. Accepting tracks with clusters in only three out of four SMT layers increases the track reconstruction efficiency by 15% to around 85%. (Here, efficiency is defined to be the fraction of tracks with transverse momentum above 1.5 GeV/c with clusters in at least three layers of the SMT that have a fit $\chi^2/d.o.f. < 3$.)

The track parameters in the r - ϕ plane are determined by fitting a linear parameterization to the SMT clusters and the CFT hits, with the form $\phi(r) = b/r + \kappa r + \phi_0$, where b is the impact parameter with respect to the detector origin, κ is the curvature of the track and ϕ_0 is the direction of the track at the

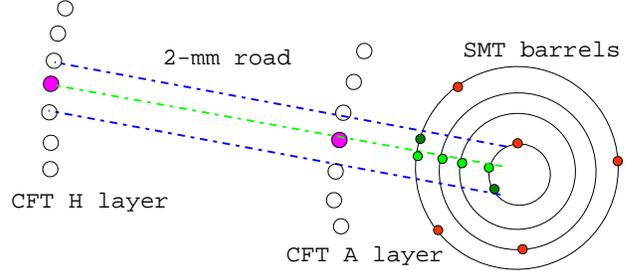


Figure 2: Diagram depicting the cluster selection algorithm.

point of closest approach. The calculation can be formulated in terms of the ϕ of the hits (three or four SMT plus two CFT hits). The ϕ residuals are defined by subtracting the ϕ value for the hit in the first SMT layer from all the other hits. Thus we have

$$\begin{pmatrix} b \\ \kappa \\ \phi_0 \end{pmatrix} = \begin{pmatrix} \text{Inverse Matrix} \\ 3 \times (N_{hits} - 1) \end{pmatrix} \times \begin{pmatrix} \Delta\phi_2 \\ \Delta\phi_3 \\ \Delta\phi_4 \\ \Delta\phi_A \\ \Delta\phi_H \end{pmatrix}. \quad (1)$$

Using near-zero ϕ residuals in the calculation allows the dynamic range required for the ϕ precision to be stored in 16-bit integers (the DSP naturally performs 16-bit integer multiplications and 32-bit summations.) This form of the calculation made feasible the use of the TI-TMS320C6203 DSP, which was deemed the best compromise of execution time, cost, processor footprint size and programming simplicity.

The matrix is precomputed as a lookup table and stored in on-board RAM. This results in a fit that is faster than computing the matrix on-the-fly and avoids problems associated with insufficient dynamic range required of 32-bit integers for the matrix inversion. To keep the lookup table size manageable, each matrix covers a range of roads. Once the matrix multiplication is performed, the final ϕ_0 value for the track is obtained by adding back the offset ϕ_1 value subtracted at the beginning. The execution time is 7.4 μs for a one-pass fit and 8.7 μs for a two-pass fit.

The TFC uses the detector coordinates to reconstruct the track impact parameter with respect to the detector origin. However, the impact parameter relevant to physics is that measured with respect to the $\bar{p}p$ interaction point (i.e., the beam spot position in the r - ϕ plane). The TFC can correct the impact parameter for beam position offsets up to 1 mm from the detector origin using a calculation easily performed in the DSP:

$$b_{corr} = b + \text{sign}(\kappa)r_B \sin(\phi_B - \phi_0). \quad (2)$$

The beam position, (r_B, ϕ_B) , is determined at the beginning of each data-taking run from a sample of several hundred events by a program running on a dedicated computer and then made available to the Level 2 trigger framework. It is then downloaded to the TFC and used for the remainder of the

data-taking run. A data-taking run may last for a few minutes up to several hours, depending on the length of the $\bar{p}p$ store.

The TFC outputs the track parameters and the fit χ^2 as well as minimal additional information regarding the fit and cluster selection. The data is transmitted to the Level 2 CFT trigger. It is also buffered on-board for VME readout to Level 3. These results are used by the Level 2 trigger framework for selecting events containing tracks of large impact parameter. Such tracks indicate the presence of long-lived particles, such as b quarks or τ leptons. The impact parameter resolution of $35\text{-}\mu\text{m}$ is dominated by a $30\text{-}\mu\text{m}$ component associated with the cross-section of the proton-antiproton beam and a $15\text{-}\mu\text{m}$ component associated with the resolution of the SMT. The uncertainty introduced by the precision of the track fitting algorithm is negligible.

F. Downloading

The contents of the lookup tables stored in on-board RAM on the STC and the TFC as well as the VHDL code and TFC DSP code must be supplied to the crate from the external system before operation. Furthermore, because some variables may change during Run II (e.g., bad strips in the SMT), some of this information may need to be updated after installation, in between data-taking run.

After power-up and initialization of the crate, the crate controlling CPU begins the procedure of downloading. The CPU first checks to see that the destination card is ready to receive the information. In the case of the TFC DSP code, the CPU checks that the TFC input dual-port memory is available and that the I/O controller FPGA is ready to receive the download. The DSP code is read from a host computer over Ethernet. It is then passed across the VME backplane, through the motherboard's PCI bus to the IDPM. The CPU then informs the I/O controller FPGA that the transfer is complete. The FPGA then transfers the program to the DSP. Then the next download can begin. Similar transfers occur with the other cards.

V. PERFORMANCE

A Monte Carlo calculation was performed to establish the properties of an unusually busy $\bar{p}p$ event as presented to the STT. For such events, it was found that on average 2.0 ± 4.3 Level 1 CFT tracks are sent to each 60° SMT sector. The average number of SMT hits per cluster is 3.6 ± 2.8 and the average number of clusters per sector is 13.9 ± 6.5 . On average, 3.7 ± 1.2 SMT clusters are used in each track fit. Using these results combined with the TFC fit execution times and estimates for the clustering and data transmission, a queuing simulation found that the STT latency is $25\ \mu\text{s}$ and the contribution to the Level 2 dead-time is negligible.

VI. CONCLUSIONS

These custom-designed VME boards make up the DØ Silicon Track Trigger. Utilizing a common motherboard, programmable processors and lookup tables for much of

the logic provides flexibility for the design, testing and maintenance phases of the project. At the time of writing, the card design is well underway and prototypes for all cards will be available in three months. The FPGA and DSP code is progressing in parallel. The STT will be installed and operating at DØ by March 2002. In conclusion, the STT is a novel device that measures the impact parameters of displaced tracks, enabling the selection of large samples of events that contain b quarks and other long-lived particles in the presence of enormous backgrounds.

VII. ACKNOWLEDGMENTS

We thank the staffs at Fermilab and collaborating institutions, and acknowledge support from the Department of Energy and National Science Foundation (USA), Commissariat à l'Énergie Atomique and CNRS/Institut National de Physique Nucléaire et de Physique des Particules (France), Ministry for Science and Technology and Ministry for Atomic Energy (Russia), CAPES and CNPq (Brazil), Departments of Atomic Energy and Science and Education (India), Colciencias (Colombia), CONACyT (Mexico), Ministry of Education and KOSEF (Korea), CONICET and UBACyT (Argentina), The Foundation for Fundamental Research on Matter (The Netherlands), PPARC (United Kingdom), A.P. Sloan Foundation, and the A. von Humboldt Foundation.

VIII. REFERENCES

- [1] DØ Collaboration, "A Silicon Track Trigger for the DØ Experiment in Run II," *DØ Note 3516*, September 1998.
- [2] VME International Physics Association, "American National Standard for VME64x 9U×400 mm Format," *ANSI/VITA 1.3*, 1997.
- [3] PCI Special Interest Group, "PCI Local Bus Specification," *PCI SIG Revision 2.2*, December 1998.
- [4] VME International Physics Association, "VME64 Extensions for Physics and Other Applications (VME64×P)," *VITA 23-1998 DRAFT*, February 1999.
- [5] IEEE Standards Department, "PCI Mezzanine Cards," *IEEE P1386.1 Draft 2.0*, April 1995.
- [6] ANSI/VITA Task Group, "PC-MIP Specification," *VITA 29 DRAFT 0.92b*, June 1999.
- [7] The Universe II chip is manufactured by Tundra Semiconductors Corporation, 603 March Road, Kanata, ON K2K 2M5.
- [8] The FLEX10K family of FPGAs is manufactured by Altera Corporation, 101 Innovation Drive, San Jose CA 95134.
- [9] The DØ SCL receiver card is being built at Fermilab, Batavia, IL 60510.
- [10] The VTM card is being built at Fermilab, Batavia, IL 60510.
- [11] The VRB card is being built at Fermilab, Batavia, IL 60510.
- [12] The TI-TMS320C6203 DSP is manufactured by Texas Instruments Incorporated, 12500 TI Boulevard, Dallas TX 75243-4136.