L2 Silicon Track Trigger

D0 Trigger Workshop

22 April 2002

Ulrich Heintz

Boston University

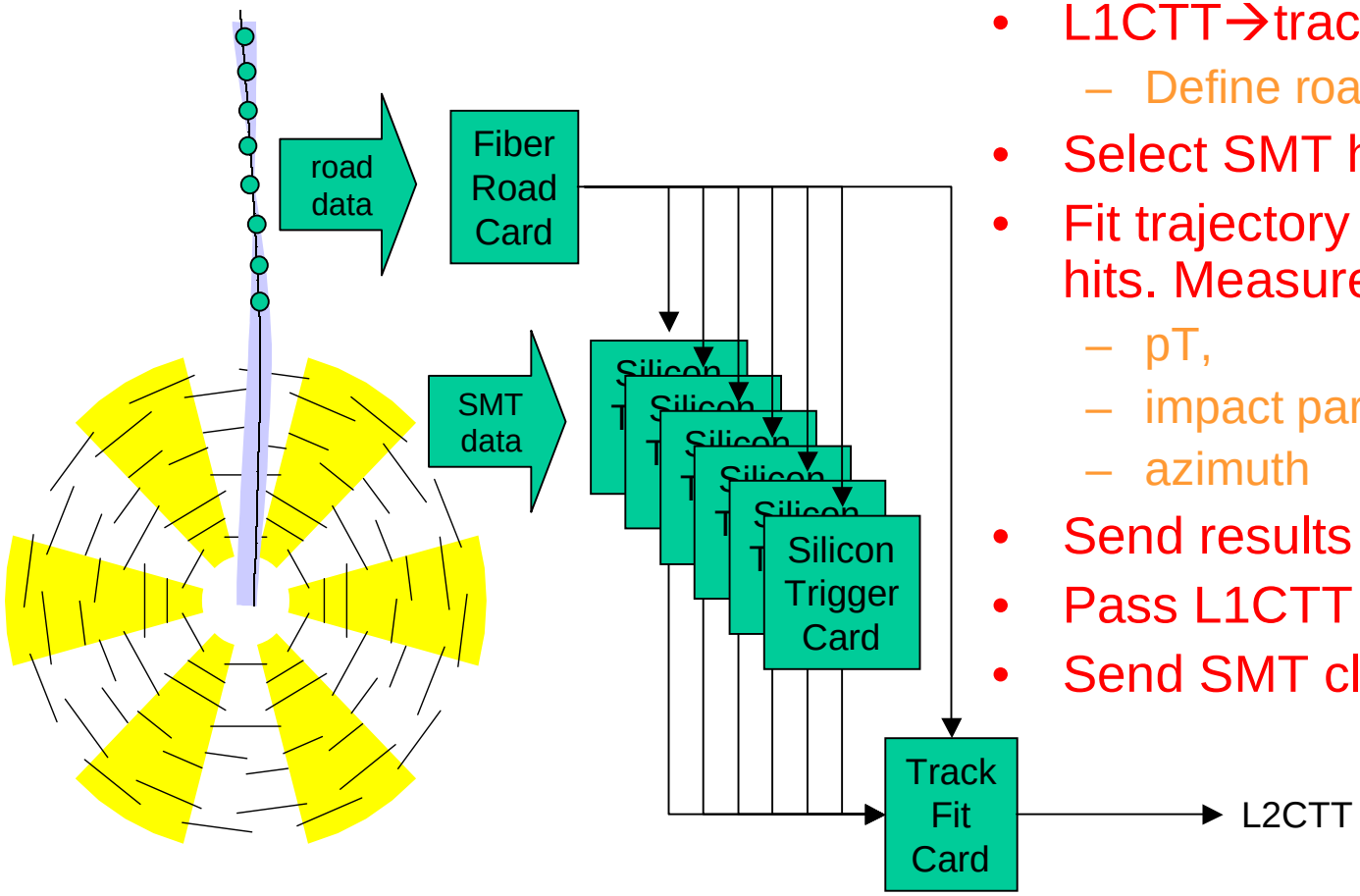
People and Institutions

- Boston University
  - Ulrich Heintz, Meenakshi Narain
  - Evgeny Popkov, Lars Sonnenschein, Jodi Wittlin
  - Kevin Black, Sarosh Fatakia, Lorenzo Feligioni, Alex Zabi
  - Eric Hazen, Bill Earle, Shouxiang Wu
- Columbia University
  - Hal Evans
  - Georg Steinbrück
  - Tulika Bose
  - An Qi
- Florida State University
  - Horst Wahl, Todd Adams, Sue Blessing, Stephen Linn, Harrison Prosper
  - Bill Lee, Sylvia Tentinto-Repond
  - Reginald Perry, Arvindh Lalam, Shweta Lolage
- SUNY Stony Brook
  - John Hobbs
  - Wendy Taylor
  - Huishi Dong
  - Chuck Pancake, Bonnie Smart, Jane Wu

STT Functionality

- Include SMT data in track trigger
  - Only available at level 2
  - Use level 1 tracks as seeds for roads
  - Search for SMT hits in roads
  - Perform fit to SMT + CFT hits

Conceptual Design



- L1CTT→tracks in CFT
  - Define road in SMT
- Select SMT hits in roads
- Fit trajectory to L1CTT+SMT hits. Measure
  - pT,
  - impact parameter,
  - azimuth
- Send results to L2
- Pass L1CTT information to L2
- Send SMT clusters to L3

Motherboard

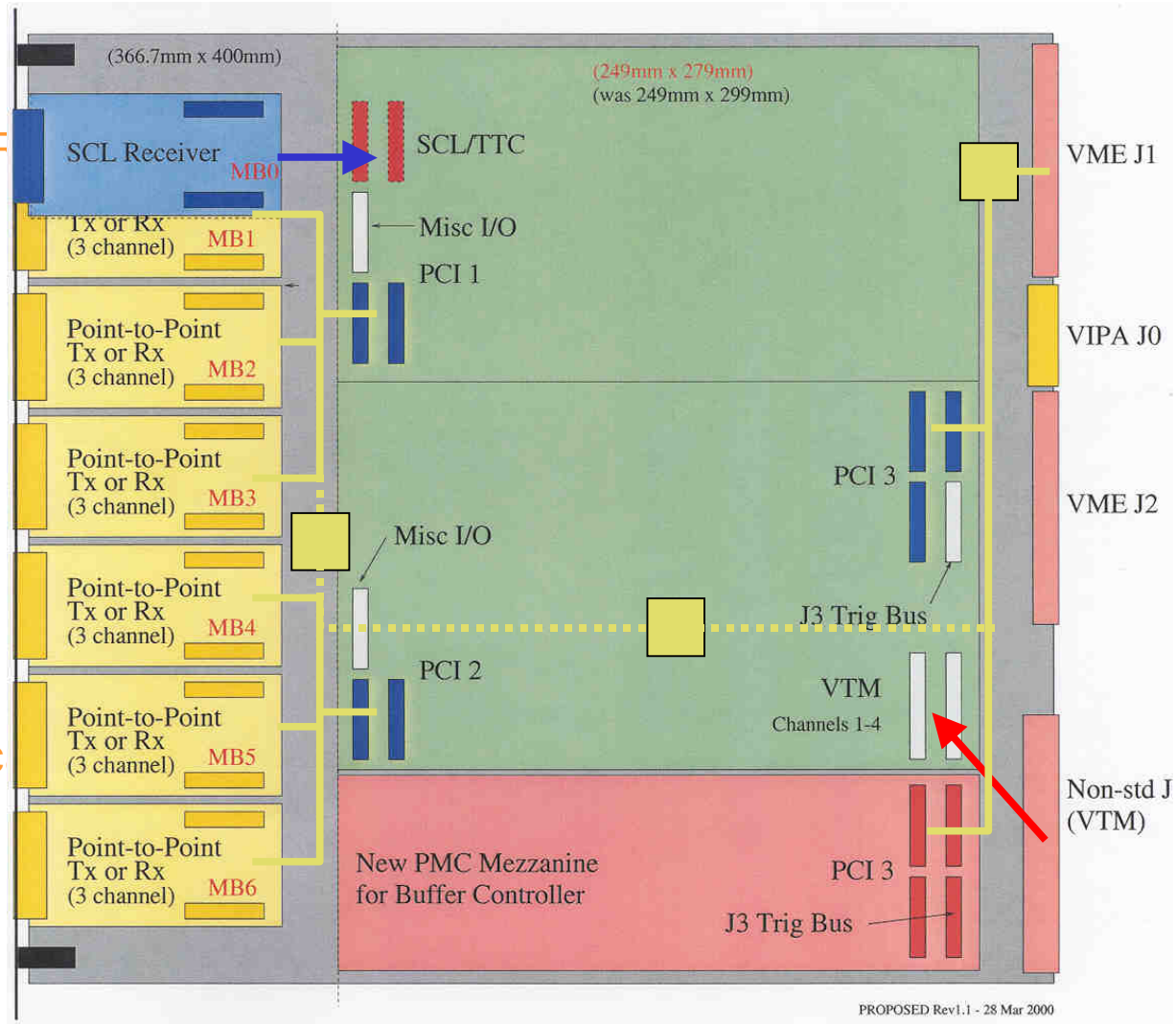
9Ux400mm VME board

- SCL mezzanine card (FF
- Up to 6 link boards
- Logic card
- Buffer controller

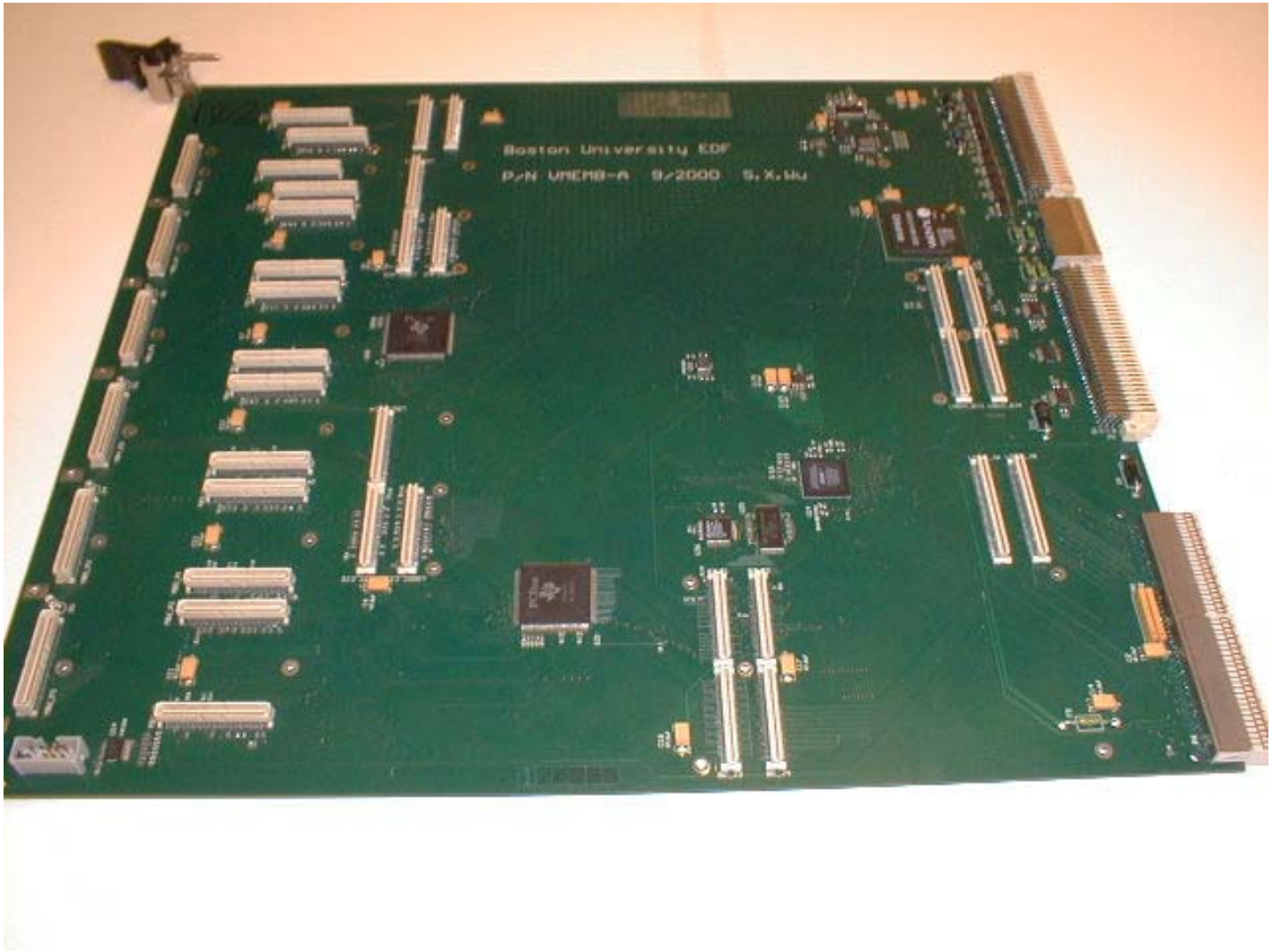
Dedicated lines
- SCL→logic card
- VTM→logic card

3 PCI busses (32bit/33MHz)
- Link boards→logic card
- Buffer controller→logic c

Universe II bridge
PCI bus to VME bus

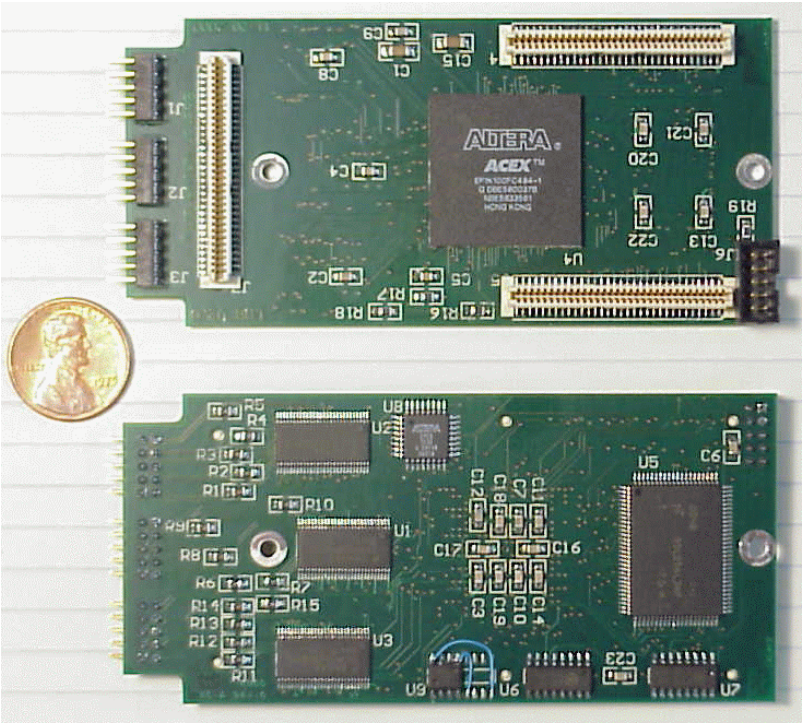


Motherboard



Link Transmitter/Receiver Boards

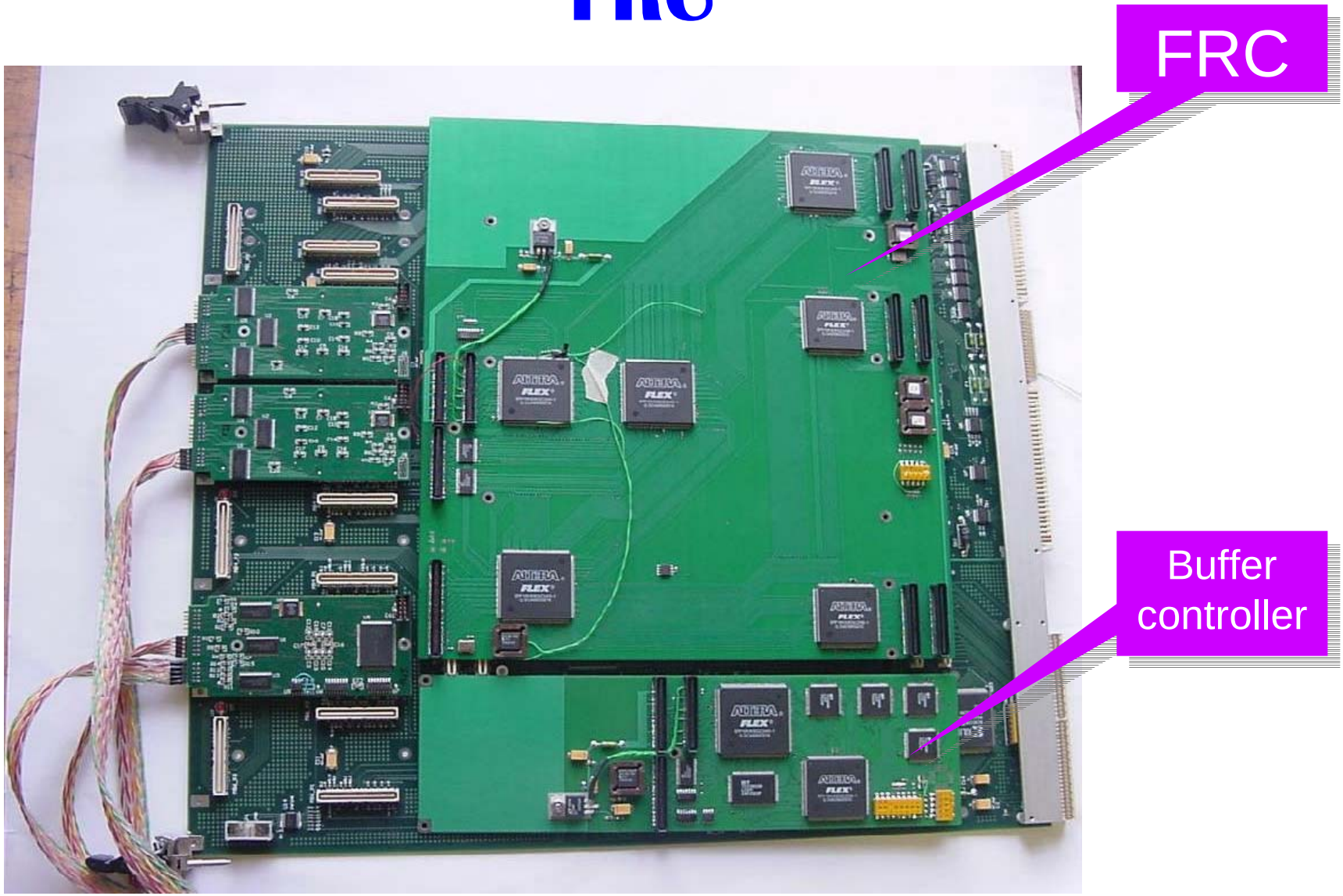
- PCMIP standard
- 3 LVDS serial links
  - 24 bits @ 66 MHz
  - 16 data bits
  - Single bit error correction
  - Multibit error detection
  - $>10^{12}$ bits w/o error
- 256k buffer
- design complete



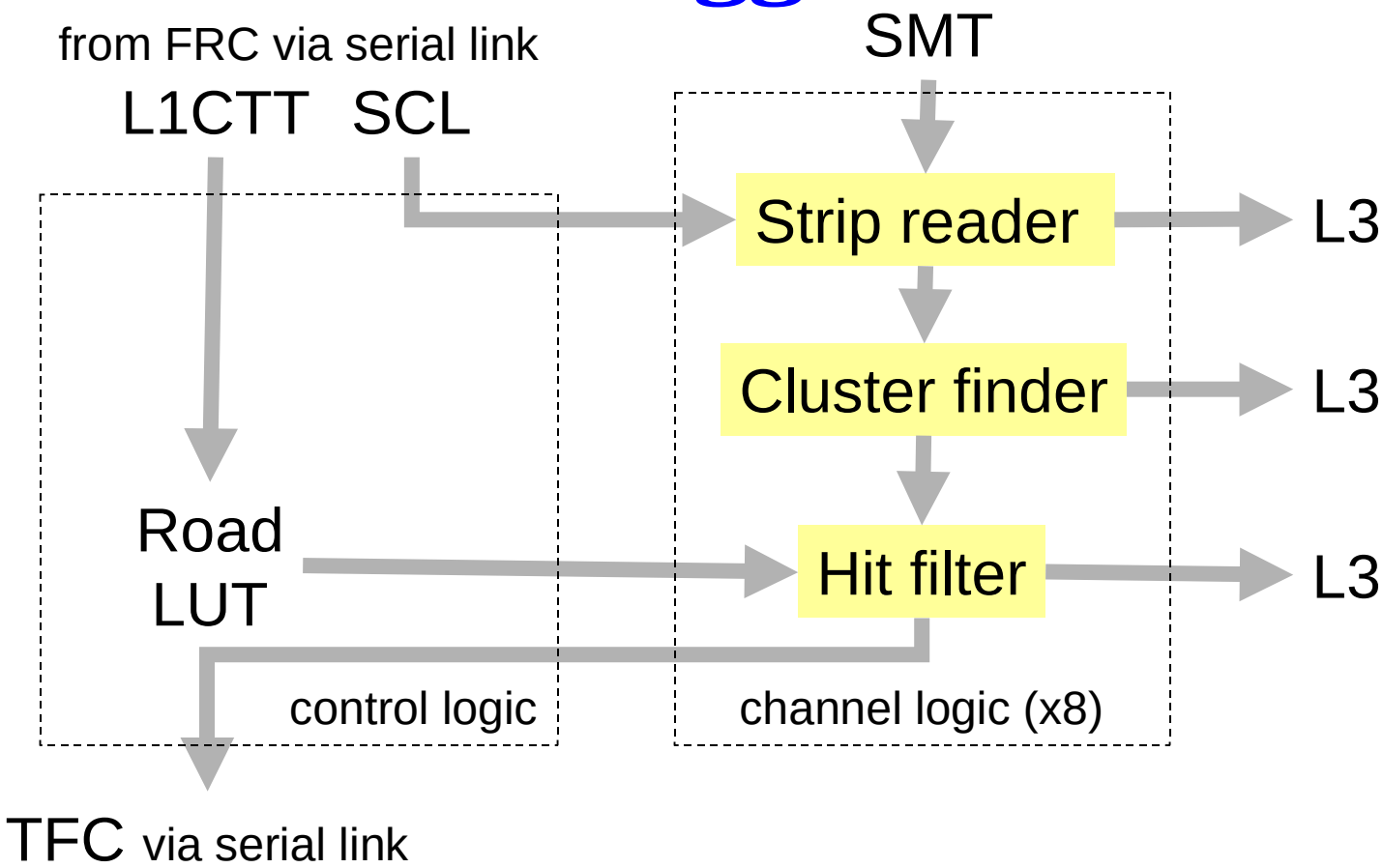
Fiber Road Card

- SCL
  - Receive 128 bits every 132 ns
  - Fan out L1_QUAL, L1_TURN, L1_BX
- L1CTT data
  - Receive 1.5 Gbit/s glink → VTM
  - Fan out
- manage L3 buffers
  - control allocation/deallocation of L3 buffers
  - send readout requests to VBD
  - send monitoring requests to CPU
- arbitrate VME bus

FRC



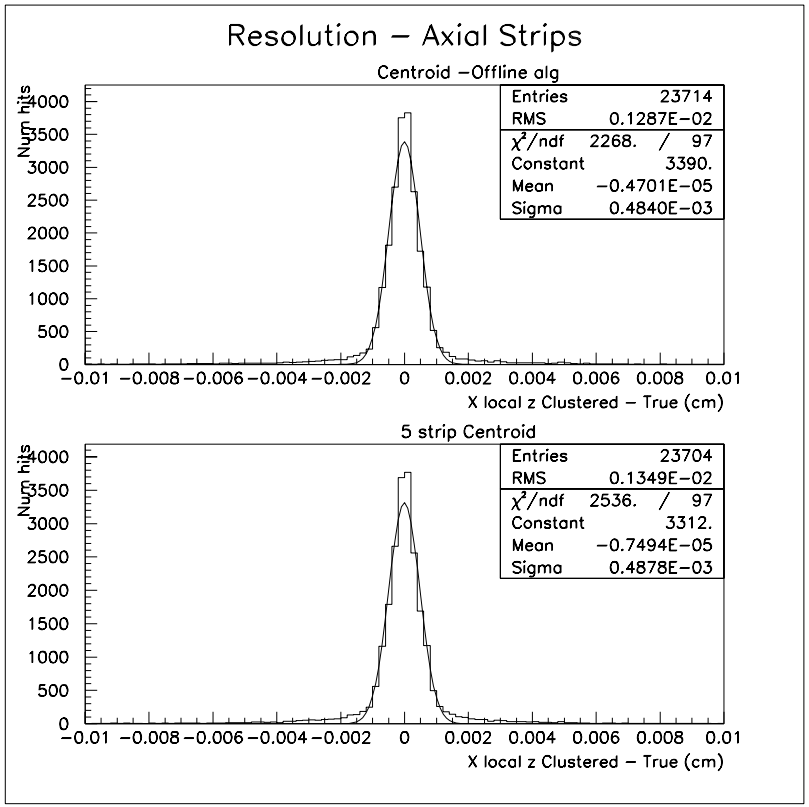
Silicon Trigger Card

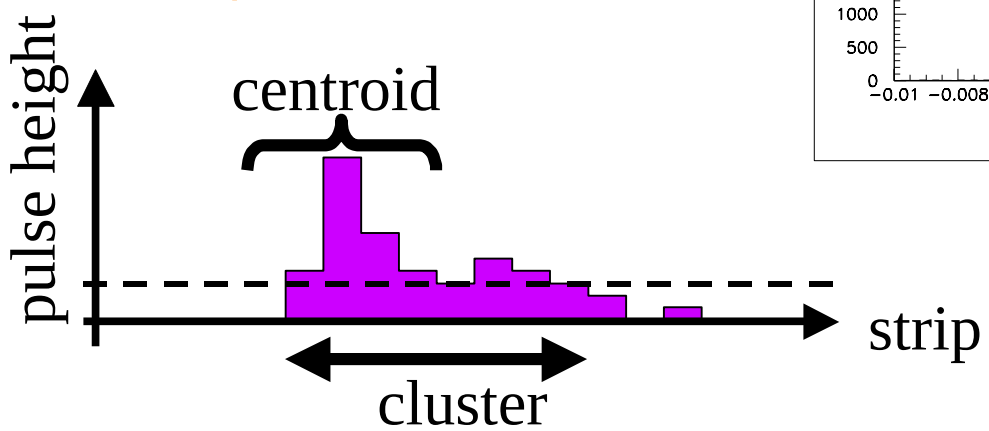


31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
track						$\frac{dE}{dx}$			sequencer							HDI			chip				centroid								

Processing of SMT Data

- bad strip mask
  - zero amplitude of flagged strips
- pedestal/gain calibration
  - chip-by-chip lookup table
- clustering algorithm
  - similar to offline, use 5 strips for centroid

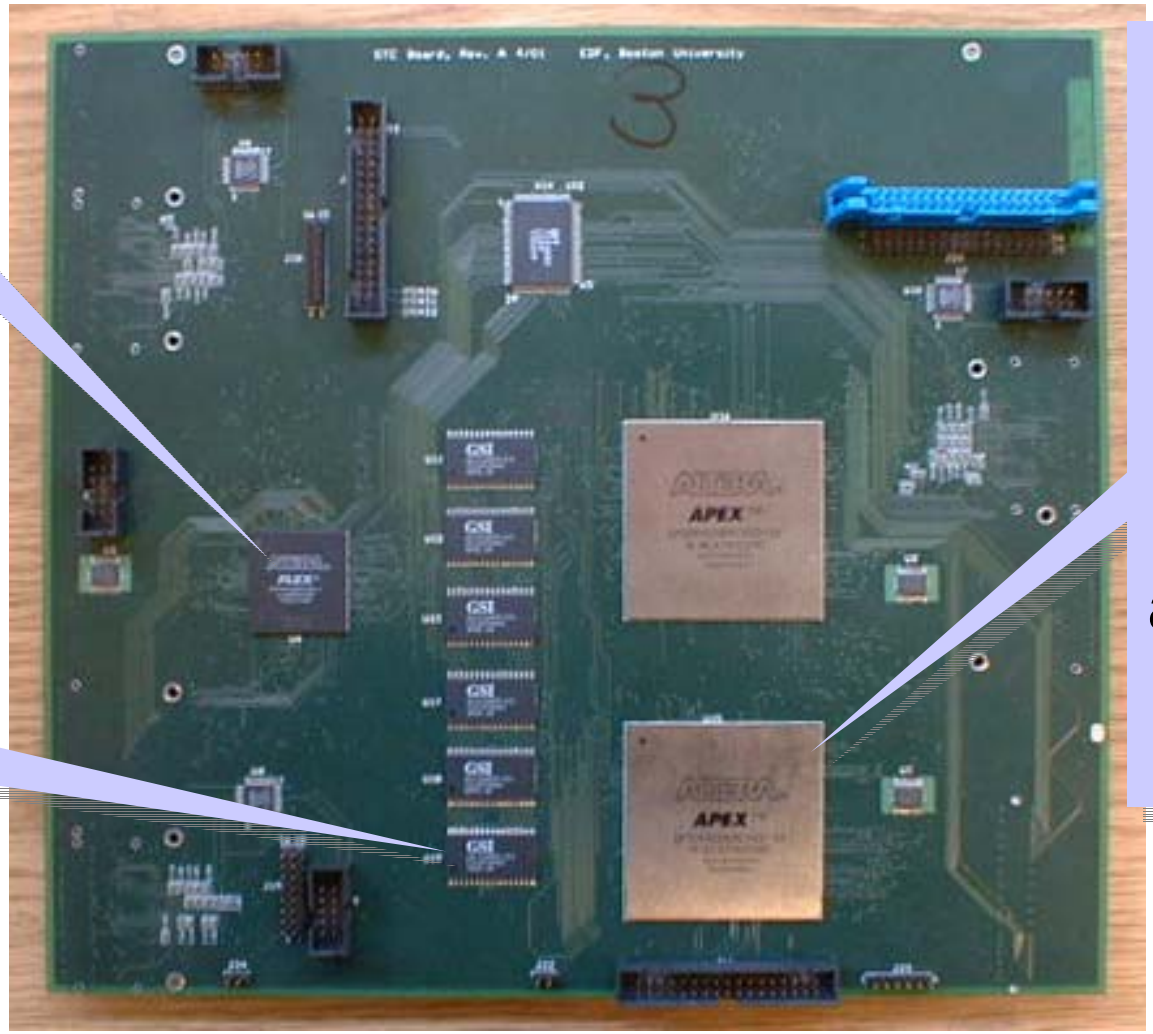




STC Prototype 1 (2 channels)

control logic

Road LUT

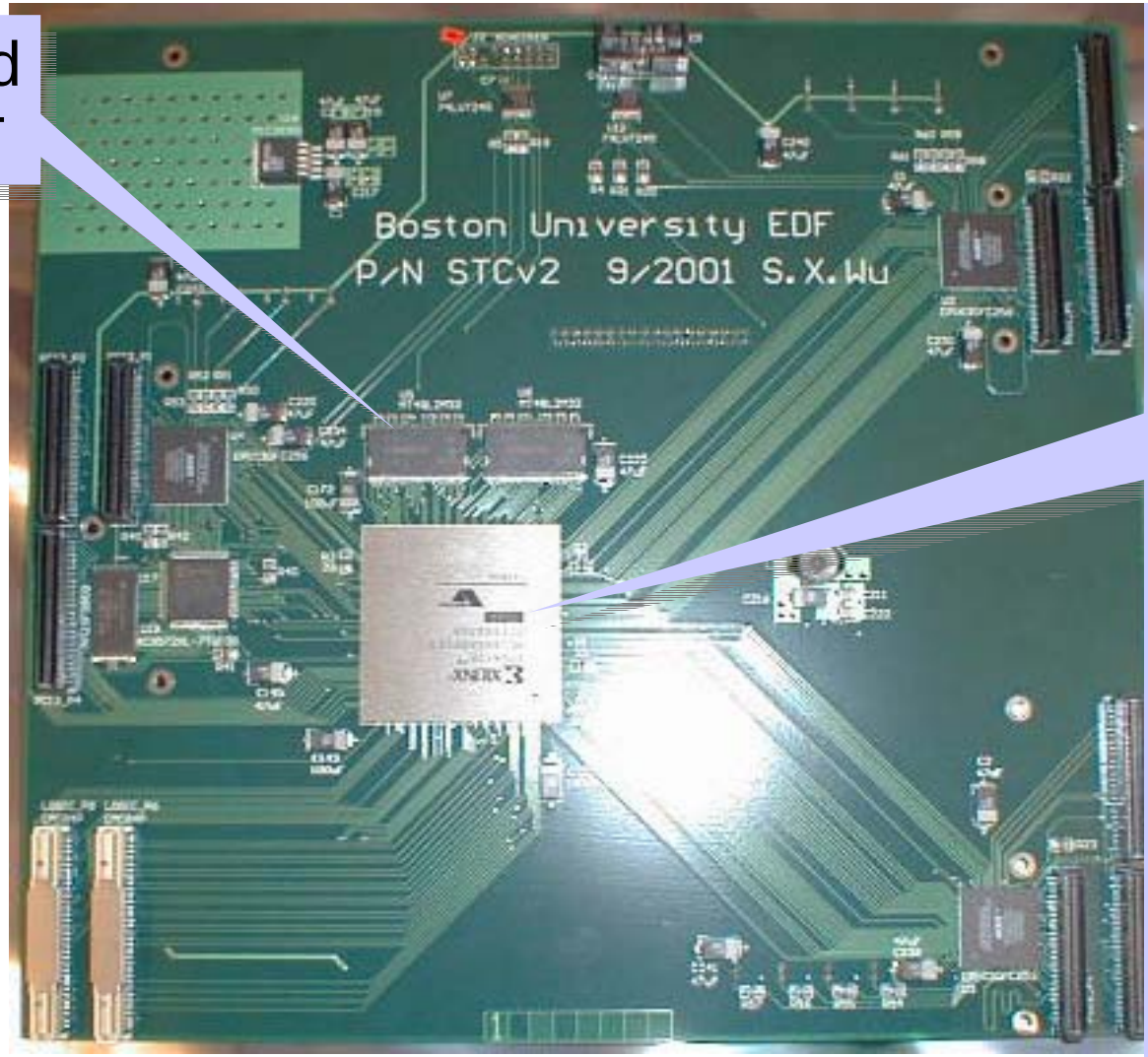


channel logic
(Altera APEX)
1.5M gates
300 kbits RAM
652 pin BGA
$1270

accommodates
2 channels
→need 4/STC

STC Prototype 2 (8 channels)

Road LUT



control logic
(8x) channel logic
(Xilinx Virtex E)
800k gates
1.1 Mbits RAM
560 pin BGA
$1200

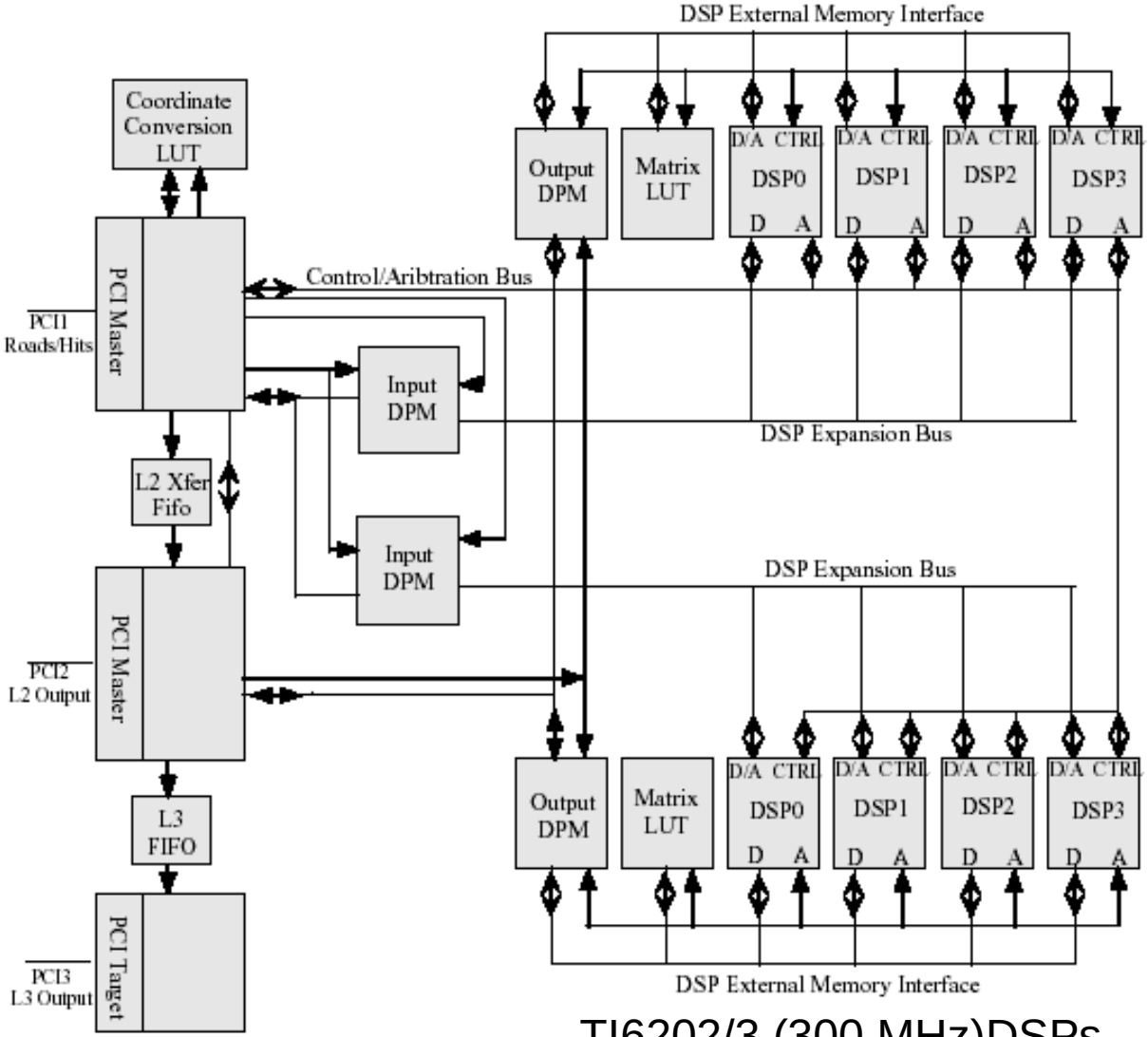
accommodates
all 8 channels
→need 1/STC

Xilinx donated
¼ 70 FPGAs

Track Fit Card

roads from FRC
hits from STC

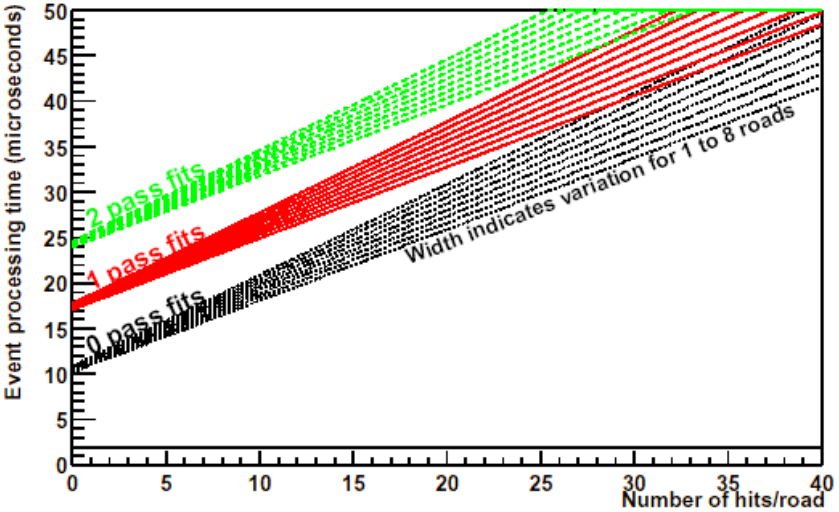
tracks to L2



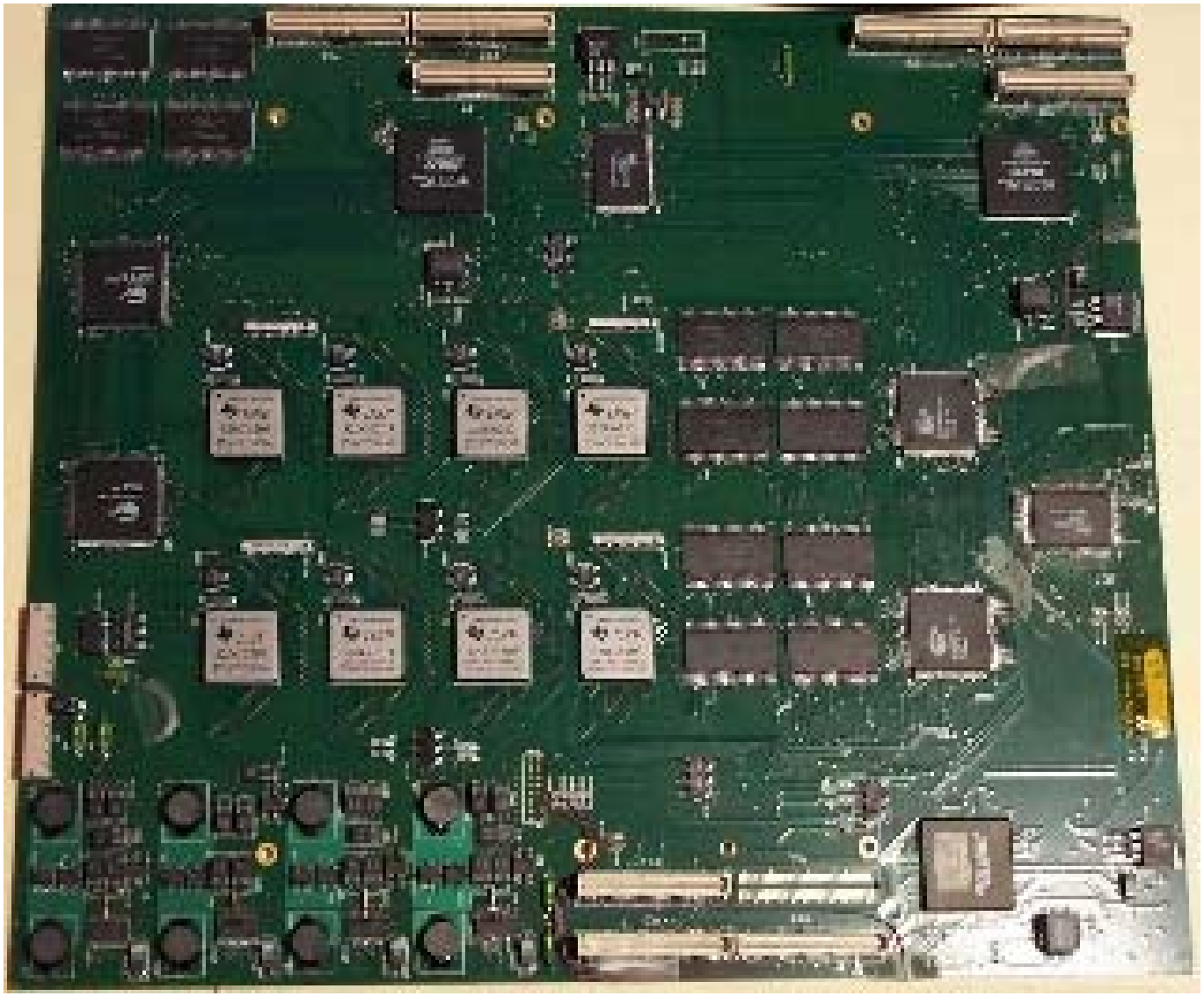
TI6202/3 (300 MHz)DSPs

Track Fit Algorithm

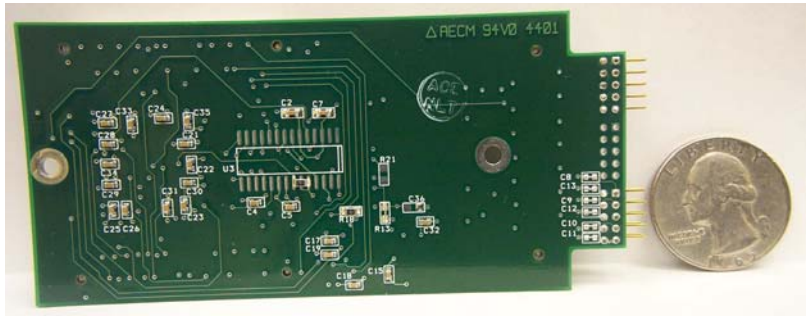
- require hits in
  - at least 3 of the 4 SMT layers
  - in same 30 degree sector
  - in at most 2 adjacent barrels
- choose hits
  - closest to trajectory defined by CFT and origin
- linearized χ^2 fit
  - $\phi(r) = b/r + \kappa r + \phi_0$
  - drop worst hit and refit if 4-hit χ^2 bad
  - measured execution time ¼25 μs



TFC

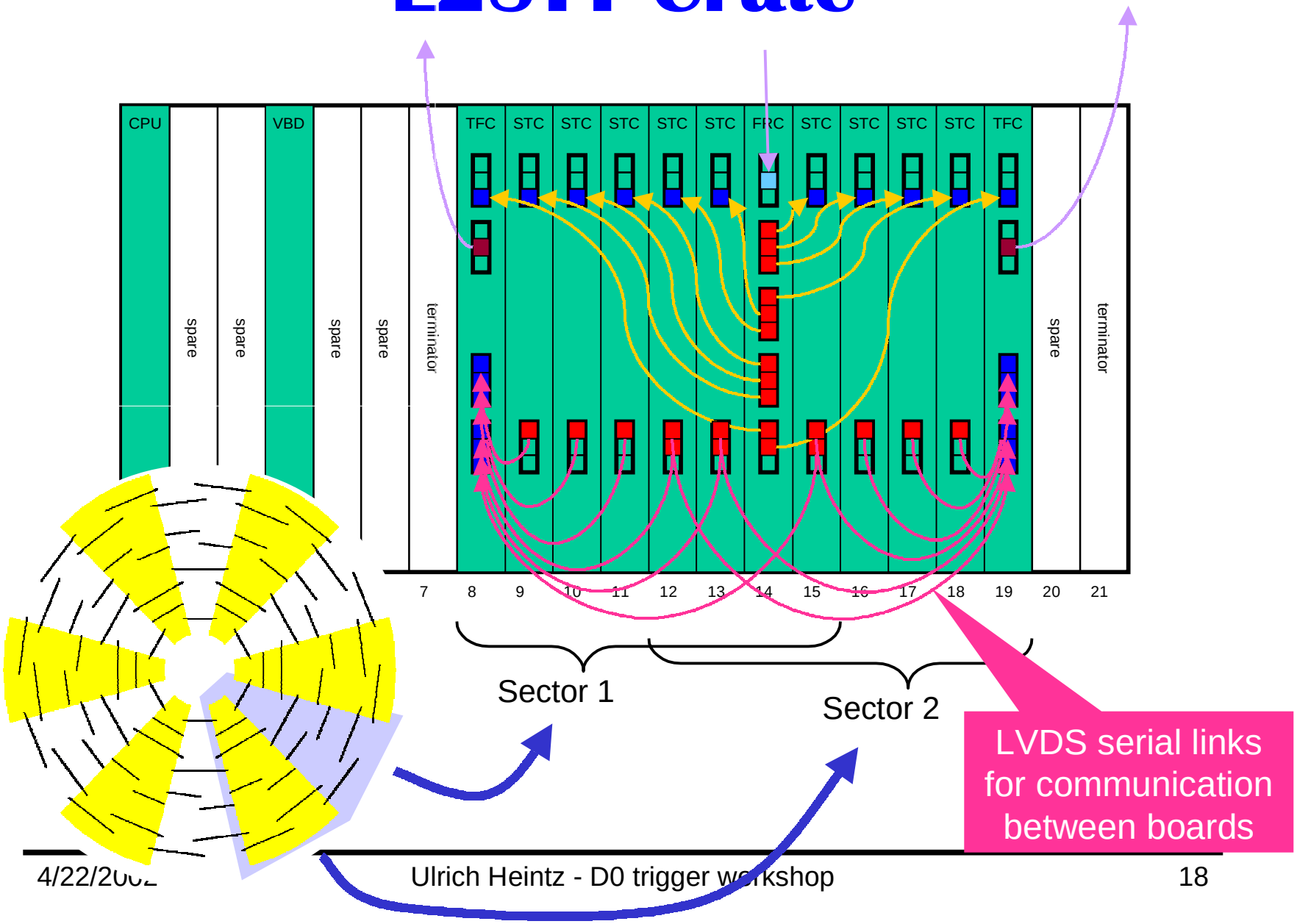


Hotlink Transmitter



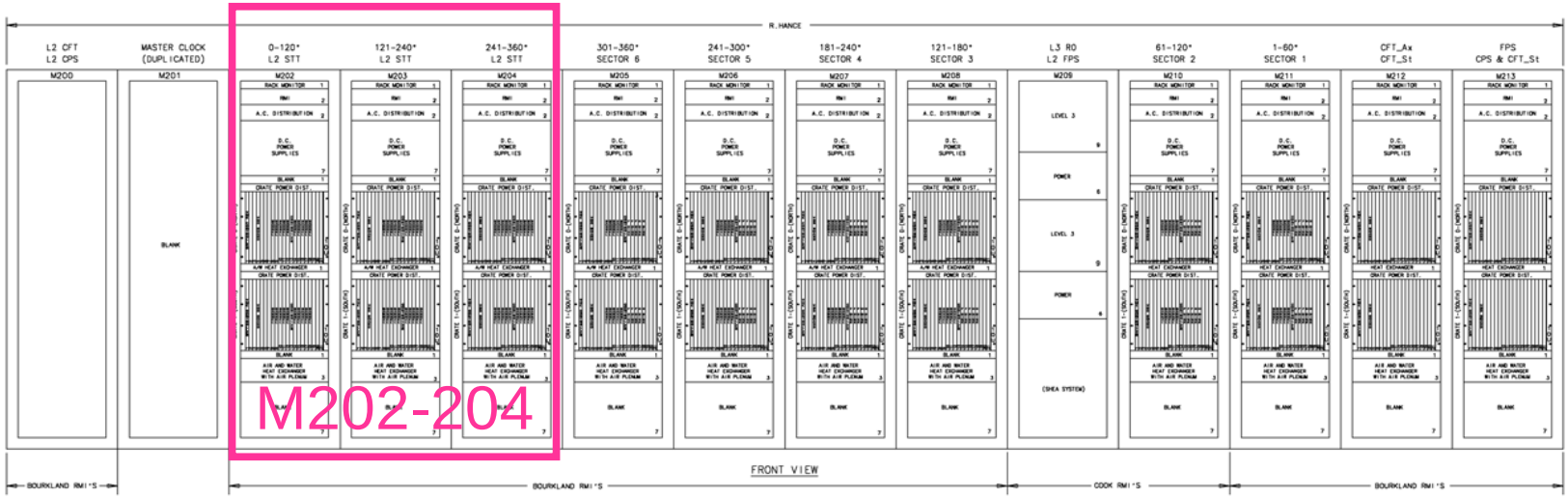
- Transmits data from TFC to MBT in L2CTT
  - cypress hotlink
  - 8 bits @ 16 MHz
  - no errors in 5£10^{12} bits transferred to MBT using built-in self test

L2STT Crate


CPU
spare
spare
VBD
spare
spare
terminator
TFC
STC
STC
STC
STC
STC
FRC
STC
STC
STC
STC
TFC
spare
terminator
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
Sector 1
Sector 2
LVDS serial links for communication between boards

MCH2

- Passive Splitters in MCH2
  - split g-link fiber from sequencer into two paths: STT and VRB
- Racks M202, M203, M204 in MCH2



Output

- to L2CTT
  - all data from L1CTT
  - for each track

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
p_T							±	S								ϕ								χ^2					x	x	f
b												x	dE/dx			track						x	x	f	f	f	f	barrel			f

p_T	transverse momentum encoded in 0.25(3) GeV increments for p_T <(>) 25 GeV:	b	impact parameter
		dE/dx	ionization
±	sign	track	track number (0-45)
S	impact parameter significance	barrel	barrel number
ϕ	azimuth	f	topology flags
χ^2	goodness of fit	x	spares

Output

- to L3 for each event
  - all information sent to L2CTT
  - for all SMT clusters

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	chan			typ		$\frac{dE}{dx}$		sequencer								HDI			chip				centroid								

  - for all SMT clusters associated with a track

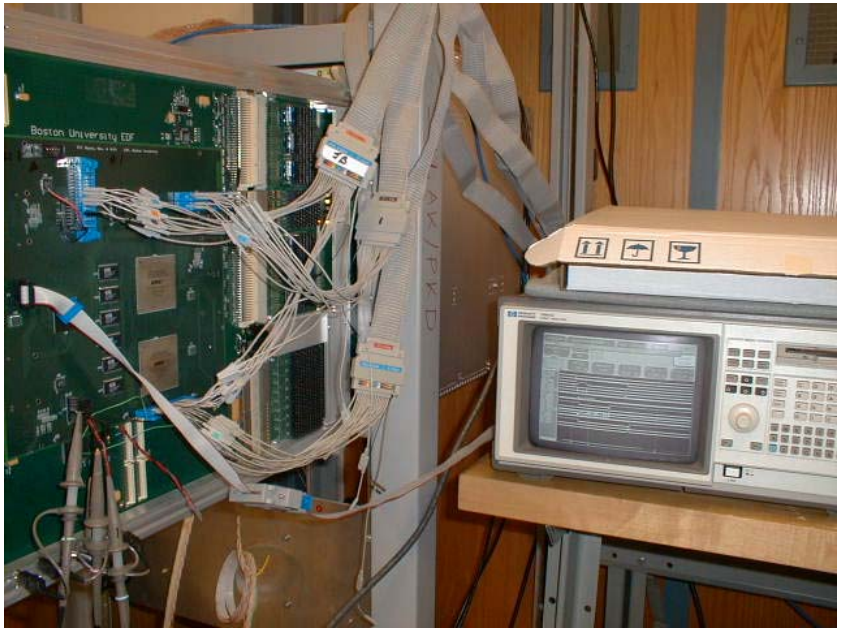
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
track						$\frac{dE}{dx}$		sequencer								HDI			chip				centroid								

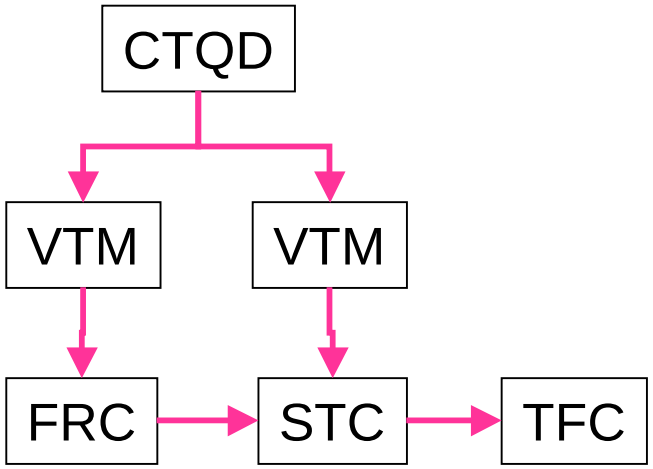
Beam Stability

- Need:
  - <500 μm offset, stable to <30 μm
  - <100 μrad tilt
- Vertex package in EXAMINE
  - Measure beam trajectory during run
  - Download at beginning of run
  - Store in accelerator control system
  - Input to feedback system

System Tests

- BU
  - Test vectors
  - FRC→STC→TFC
- FNAL
  - Communication tests
    - FRC ←→ SCL
    - SMT → VTM → STC
    - VBD ←→ FRC/BC
  - send test data from CTQD test card
    - L1CTT data and one SMT fiber
    - no SCL
    - VTM→FRC→STC→TFC
  - need L1CTT inputs for complete test
    - synchronized SCL/L1CTT/SMT data
    - need for tests with full speed





Schedule

- System Test
  - in process
- Production
  - in process

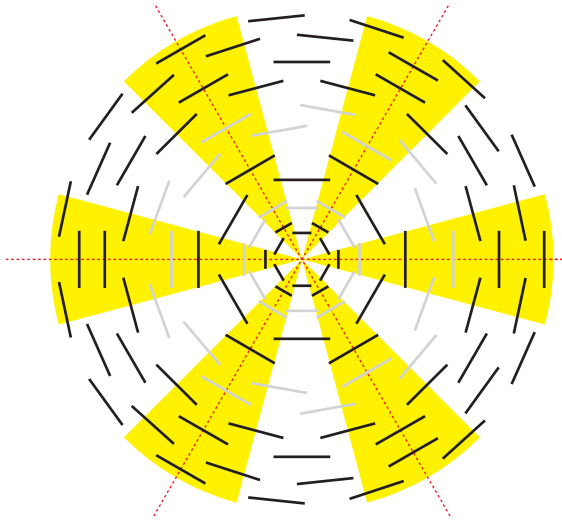
need L1CTT inputs to complete tests and commit all modules to production

- Installation/Commissioning
  - end summer 2002....(?)

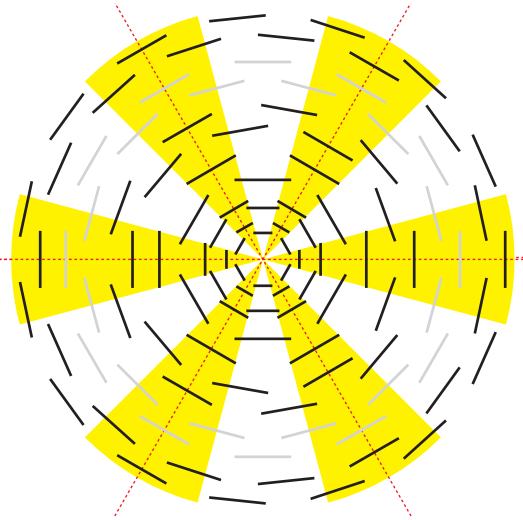
Run 2b

- SMT replacement: 6 axial barrel layers
  - more readout units (HDIs)
  - **need more STC boards**

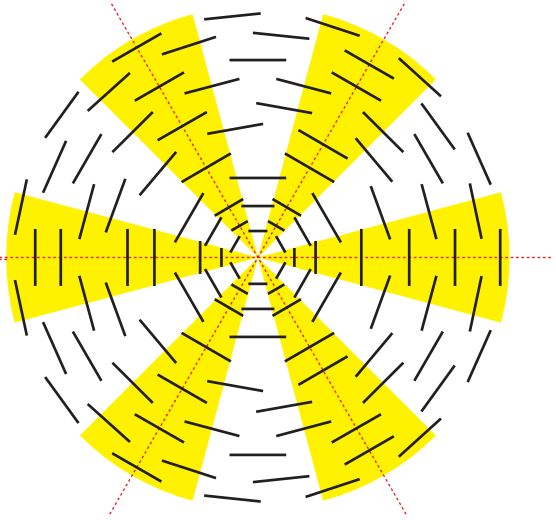
no upgrade



modest upgrade



full upgrade



Run 2b

Option	No upgrade	Modest upgrade	Full upgrade
FRC logic board	6	6	6
STC logic board	54	60	72
TFC logic board	12	12	12
motherboard	72	78	90
SCL mezzanine card	6	6	6
link transmitter	78	90	102
link receiver	90	96	108
hotlink transmitter	12	12	12
buffer controller	72	78	90
VTM	60	66	78
Additional cost (no cont.)	$34k	$81k	$231k

Conclusions

- All modules prototyped
- Integration tests under way
  - need L1CTT inputs asap
- Production
  - started for most boards
- Goal: operational end summer 2002
- Documentation
  - http://www-d0.fnal.gov/trigger/stt/