



**Fermi National Accelerator Laboratory**

## **D0 Central Tracking Solenoid**

### **Specification for Solenoid Energization, Controls, Interlocks and Quench Protection**

**D0 Engineering Note 3823.111-EN-418**

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## 1 Introduction

This document has served as the specification for the **energization, control, interlocking and quench protection systems** for the DZERO superconducting solenoid installation. This does not include the cryogenics system. As the work proceeded, the details of the design were "fleshed out" such that this document ultimately describes the system "as built". See "Revisions to this document" for a description of all changes incorporated since the initial date. These changes have been integrated into this document; but are listed separately for historical reference.

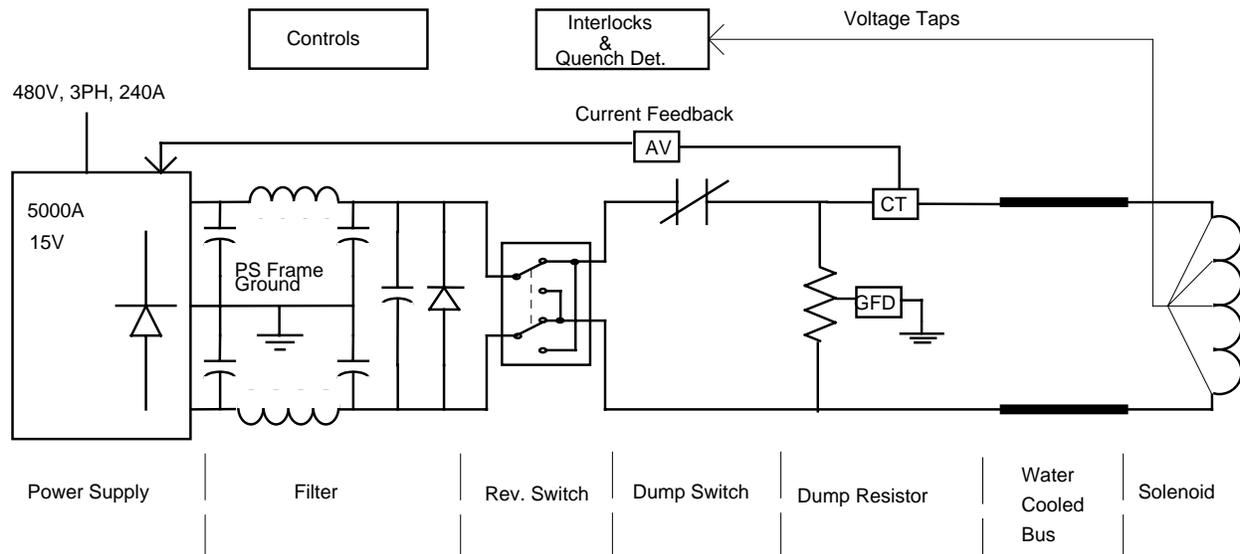
**The basis for this specification is the FERMILAB-TM-1886, May 13, 1994: "Conceptual Design of a 2 Tesla Superconducting Solenoid for the Fermilab D0 Detector Upgrade", Chapter 9, "Control and Instrumentation"; and Chapter 10, "DC Energization Circuit".**

This spec. has provided a stationary target for final design; and a central source of reference to the finished system. The original sources are identified wherever possible if they differ from FERMILAB-TM-1886. Please forgive the unintentional omission of credits and the initial errors. "If Argos hyer himself haft been, he would perhaps not all haft seen"

## 2 System Overview<sup>1</sup>

### 2.1 Block Diagram of system

This is a sketch of the configuration of the DC energization system. It does not show the flow of controls, interlocks and quench protection. Each component is discussed in this document.



<sup>1</sup>FERMILAB-TM-1886 "Conceptual Design of a 2 Tesla superconducting solenoid for the Fermilab D0 detector Upgrade", Chapter 9 and 10, 5/13/94

## 2.2 Documentation Index

This is a listing of major documents associated with this project. Most relevant documents, including drawings, may be viewed and obtained from the world wide webb (WWW) at:

<http://www-d0.fnal.gov/~hance/solenoid.htm>

'Full size' copies of **drawings** may also be obtained from masters which are maintained in the DZERO flat file system located in the DZERO third floor hi-bay. Copies of **D0 Engineering notes** can also be obtained from the D0 department files. Copies of R. Hance Engineering Notes may be obtained from R. Hance at D0. Copies of **Fermilab TMs** may be obtained from the publications office. A full list of ALL engineering notes -- including detail design notes not listed here, are kept in a data base maintained by R. Hance.

Document Number	Description
FERMILAB-TM-1886	Conceptual Design of a 2 Tesla Superconducting Solenoid for the Fermilab D0 Detector Upgrade
D0 Engineering Note 3823.111-EN-418	Specification for Solenoid Energization, Controls, Interlocks and Quench Protection (This document)
R. Hance Engineering Note H941109A	Project Description/Status/Standards
R. Hance Engineering Note H960305A	Solenoid Energization Overview - Slides
R. Hance Engineering Note H951107A	Solenoid Energization Cost Estimate
R. Hance Engineering Note H980826B	Solenoid Energization Operating Procedures
D0 Dwg. 3823-111-ED-330052	Schematic - Solenoid Energization, Controls & Interlocks - 17 Pages
EAD Spec. 6005-ES-44047	Power Supply Spec. - PE150
R. Hance Engineering Note H960730A	Power Supply Ripple Calculation
R. Hance Engineering Note H970528A	Power Supply Regulation During Charging
R. Hance Engineering Note H970729A	Power Supply Charging Voltage Limiter
R. Hance Engineering Note H960314A	Solenoid Quench Detector Signals
R. Hance Engineering Note H971203B	Quench Detector Single Component Failure Analysis
R. Hance Engineering Note H960703A	Filter Design
R. Hance Engineering Note H960801A	Filter Analysis - Fast and Slow Dump
R. Hance Engineering Note H960731A	Filter Component Ratings
R. Hance Engineering Note H960918A	Filter Capacitor Conductor Sizing
R. Hance Engineering Note H960625A	Filter Air Core Coils
EAD Dwg. 6008-ED-43551	Reversing Switch Controls
DO Dwg. 3823-111-ME-330100	Dump Resistor - Mechanical Dwg.
R. Hance Engineering Note H960814A	Dump Resistor - Design Note - W. Jaskierny
R. Hance Engineering Note H960917B	Dump Resistor - Design Review
R. Hance Engineering Note H950919A	Bus Characterization

R. Hance Engineering Note H950306A	Bus Length Calculations
R. Hance Engineering Note H950306B	Bus Force Calculations
R. Hance Engineering Note H961028A	Bus Connections - Bolts, Area, Prep, Torque
EAD Dwg. 2214-EE-173374	Research Division Dzero Cable Tray; DC Bus for Solenoid Magnet
R. Hance Engineering Note H951013A	Solenoid Characterization
R. Hance Engineering Note H961107A	Controls End Rack Wiring Standard
R. Hance Engineering Note H961025B	Controls End Rack Wiring Database
R. Hance Engineering Note H961209A	Controls Modules Jumper Settings
R. Hance Engineering Note H961216A	Controls DMAPS Tagname Standards
R. Hance Engineering Note H970603A	Controls PLC Program
R. Hance Engineering Note H970603B	Controls DMAPS Program
R. Hance Engineering Note H970603C	Controls DMAPS Database
R. Hance Engineering Note H970423A	Absolute Value Module Design Review
R. Hance Engineering Note H970727A	Ground Fault Detector Module Design Review
R. Hance Engineering Note H971029A	LCW & Condensation Control
R. Hance Engineering Note H980127A	Initial System Checkout Procedure
R. Hance Engineering Note H980826B	Operating Procedures

### 2.3 Location of Power Supply and Equipment Racks

The DC power supply, filter, polarity switch, dump switch, dump resistor and controls rack are located in room 511 on the South Side of the DZERO Assembly Building (DAB). The equipment rack contains the controls I/O base, interlock and quench detection/protection crate. An "end rack" of terminal strips is installed on the rack and **all** interface connections are made using "faston" type connectors in those terminal strips. A document listing all endrack connections shall be maintained and displayed at all times on the door to the end rack. The door is equipped with a lock to discourage unauthorized tampering with the connections.

The location has floor loading limitations which have been considered (EMAIL Krempetz/Hance 1/11/96); and has a large double door to the outside and is convenient for lifting in equipment, installing AC power and cooling water; and routing DC bus work to the collision hall. This location is preferred to keep the bus length short in order to run the power supply at maximum efficiency by using the 15V tap.

### 2.4 AC Distribution

The 150 kW power supply requires 480 Volts, 3 phase, 240 Amps ( $\approx 138$  Amps at our 75 kW maximum operating point<sup>2</sup>).

A 480 Volt 3 phase, 300 Amp circuit breaker is installed in the switch gear in the 3rd floor utility room. This provides a common lockout point for the WAMUS and Solenoid power supplies in addition to integrating into the existing building power monitoring system. From the circuit breaker to DAB 5th floor north, 350 MCM conductors are used. These conductors were

<sup>2</sup> See also - Engineering Note - H970123A - R. Hance - Solenoid power supply circuit breaker calculation.

previously used by the now de-commissioned SAMUS power supply. These conductors end on DAB 5th floor north. From there, paralled 350 MCM conductors are butt spliced and routed up through the floor to DAB 6th floor, out through the wall into a cable tray, across the top of the assembly pit and directly into room 511 on the south side of DAB. Paralled 350 MCM conductors are used to minimize voltage drop as the cables traverse the asembly pit, a distance of about 80 feet. A 400 Amp lockable disconnect switch is provided adjacent to the power supply to facilitate safe servicing. In addition, the power supply has an integral disconnect switch to prevent opening its access door with energized AC.

Accessory power at 120/240 volts is also provided. This is derived locally from power panels in the south assembly hall area.. Interlocks and controls are provided with uninterruptable power from the nearby commercial UPS that also supplies the cryo systems.

## **2.5 Cooling Water**

Low conductivity chilled water (LCW) is piped in from the north side of the assembly hall pit. The routing of the pipes follows the routing of the 300 Amp AC service. LCW is provided to the power supply, power supply filter coils, free-wheeling diode, and water-cooled bus. The cooling water requirements, controls, and condensation prevention are described in a separate document<sup>3</sup>.

The LCW monitoring system shall supply a relay contact to the interlock system to indicate that resistivity is above the limit and that flow is adequate.

## **3 DC Power**

The DC power supply circuit includes the power supply, filter, reversing switch and DC bus . The dump switch and resistor are described under Interlocks and Quench Detection/Protection.

### **3.1 Power Supply<sup>4</sup>**

1. The power supply is a Power Energy Industries model #SR-1029 also known as a PEI 150-5. This is a 150 kW, 12 phase unfiltered supply, designed for superconducting loads and is tapped to provide a maximum of 5000 Amps at a maximum of 15 volts (75 kW).
2. The power supply shall be operated in the current regulating mode. The experiment has requested current regulation to 7.5 Amperes or better<sup>5</sup> (0.15%, 1500 ppm). The supply is specified by the vendor to provide current regulation of < 0.05% when operated between 20% and 100% of range. Thus the power supply current is expected to deviate less than  $\pm 2.5$  amps when operating at 5000 amps. From actual experience, the supply is expected to regulate to less than  $\pm 0.50$  amps.
3. The power supply incorporates a programmable internal voltage limiter circuit<sup>6</sup> which allows controls software in the PLC to limit the maximum output voltage during charging to prevent

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<sup>3</sup> See also - Engineering Note - H971029A - R. Hance - Solenoid Power Supply and Bus Cooling and Condensation Control.

<sup>4</sup> The connection details of the power supply are shown on Sheet-7 of schematic #3823-111-ED-330052.

<sup>5</sup>R.P Smith note titled "Power Supply Current Regulation for the D0 Solenoid" dated March 7, 1995.

<sup>6</sup> Power supply charging voltage limiter described in engineering notes #H970528A and H970729A by Hance and is detailed on Sheet-7 of schematic #3823-111-ED-330052

quenching. Note that a fast or slow dump shuts off the power supply, bypassing the rate limiting. In this case discharge rates are controlled by circuit impedance.

4. An external transducer<sup>7</sup> is mounted between the dump resistor and the solenoid magnet to provide current feedback to the power supply regulation circuit in order to compensate for the losses in the filter and the dump resistor.
5. The experiment has requested current readback resolution precision of 7.5 Amps or better. The read back of the power supply current shall have an absolute precision of  $\pm .05\%$  at full scale. Thus the read back should be within  $\pm 2.5$  amps of the actual value.
6. The ground fault monitor within the power supply is not used. Instead, ground faults are monitored at the dump resistor center tap by a custom designed circuit<sup>8</sup>.

### 3.2 Power Supply Filter<sup>9</sup>

A filter is provided at the output of the power supply to reduce primarily the high frequency common mode noise due to SCR firing and transformer inter-winding capacitances. The design of this filter is described in separate documents (see footnote).

The filter is in the form of a choke in the supply lead and another in the return lead of the power supply; with a capacitor across the output of the chokes for differential mode noise suppression.

Also of utmost concern is the reduction of the high frequency common mode noise. Common mode noise is suppressed by configuring a pi filter using the two chokes along with capacitors to ground on the inputs and outputs. The term "ground" refers to the power supply frame. The capacitor grounds return directly to the power supply frame via a wide, flat, low inductance copper strap.

The power supply contains a freewheeling diode to conduct the current decay when the supply is turned off. However, this power supply diode is not rated to carrying the decaying current if a cooling water failure occurs during a discharge. Therefore, an extra freewheeling diode is installed downstream of the filter choke and is sized to carry the decaying current without cooling water. These diodes also prevent the possibility of polarity reversal across the filter capacitors.

### 3.3 Reversing Switch<sup>10</sup>

The reversing switch assembly is a 5000 amp dc mechanical, motorized polarity reversing switch and integral switch controller.

1. The switch is floor mounted and requires no water cooling.
2. The switch controller is remotely controlled by an isolated relay contact in the control system. Open contact signals the switch to be in the forward state, closed contact signals the switch to be in the reversed state.

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<sup>7</sup> The Holec transducer and its electronics chassis is detailed on Sheet-11 of schematic #3823-111-ED-330052.

<sup>8</sup> See also - Engineering Note - H970627A - R. Hance - Solenoid Ground Fault Detector Module Design Review.

<sup>9</sup> The power supply filter is described primarily in Engineering note #H960703A by Hance and on Sheet-8 of schematic #3823-111-ED-330052. See also the documentation list for other related notes.

<sup>10</sup> The reversing switch and controller is detailed on Sheet-9 of schematic #3823-111-ED-330052

3. The switch controller provides a status contact to the control system to indicate the status of the switch i.e. forward/reverse/cycling. This contact mirrors the forward/reverse control contact when the switch is not cycling. If the status contact does not mirror the control contact, then the switch status is assumed to be "cycling". The control system allows sufficient time between setting a new state and reading status to allow the status to change as the switch begins cycling
4. The switch controller performs the essential function of ensuring that the polarity reversal occurs at zero load current and that the power supply programming voltage is held disabled during the reversing process.
5. The switch controller uses a motor driven timer with cam switches. Once a cycle is started, it must complete before it can be used again. A complete cycle is expected to take approximately 40 minutes including discharging the solenoid, cycling the switch and charging the solenoid.

### 3.4 DC Power Bus<sup>11</sup>

The interconnecting links between the power supply, filter, reversing switch, dump switch and dump resistor are solid copper buses. The buses are sized such that current density is 1000 Amps per square inch or less. Thus the contact area of bolted connections is 1 square inch per 1000 Amps or more. The contact force of bolted connections is 2000 pounds per square inch or more<sup>12</sup>. The bus connections, bolts, torques, contact area and preparation for assembly are described in a separate document<sup>13</sup>.

The bus from the power supply room to the superconducting solenoid is a 5000 Amp water cooled system as is traditional at Fermilab. The resistance of the bus will help dissipate the energy of the solenoid, filter and bus inductance during a discharge. Two separate buses are installed. One for each location of the solenoid as follows: One bus runs from the dump resistor, located in the power supply room, to the solenoid located in the collision hall. The other bus runs from the same starting location, to the position occupied by the solenoid when it is in the assembly hall. Each bus shall have the same electrical resistance in order to minimize variables between testing and operation. The resistance shall be equalized either by making the buses the same physical length or by inserting a length of stainless steel bus into the shorter bus run to increase its resistance. Bolted connections at the dump resistor are used to select the collision hall bus or the assembly hall bus.

1. The bus consists of 1.5" double extra strong copper pipe (CDA alloy 102) joined by silver soldering or brazing couplings or elbows as is customary through out the Research Division (FERMILAB-TM-1372).
2. High impact PVC pipe is slipped over the straight lengths of copper pipe for insulation; and shrink-on sleeves is used at couplings and elbows as required.

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<sup>11</sup>The dc power bus is detailed in FERMILAB-TM-1372 "Description of a high current water cooled bus" A.T. Visser, Dec. 1985; and section 10-6, "Water cooled bus" of FERMILAB-TM-1886.

<sup>12</sup>Electrical Design Guidelines for Electronics to be used in Experiment Apparatus at Fermilab Rev 2.1 -- EED Department Document dated 12/22/94

<sup>13</sup> The bolt connections, bolts, torques, contact area and preparation for assembly for the high current solid copper bus work are detailed in engineering note H961028A by Hance.

3. The buses are routed within a covered, aluminum cable tray. The tray, which acts as an electro-static shield and as a return path for filtered noise currents, is welded at its seams to eliminate degraded continuity from corrosion. The tray is insulated from ground everywhere except at the power supply frame. It is physically and electrically attached to the power supply frame which is firmly attached to the building frame (ground).
4. A suspension system of Unistrut, pipe clamps and fiberglass insulators is used to route the tray and insulated buses from the power supply area to the assembly hall and collision hall. Routing is above the south catwalk.
5. The supply and return bus is routed adjacent to each other on 5" centers in order to reduce the loop area and inductance of the bus system.
6. Copper flags are brazed or bolted to the ends of the bus for cable attachment.
7. Water cooling is accomplished with LCW hose connections to the bus end caps.
8. Over temperature switches are installed near the cable connections flags and wired to the interlock system.

*The electrical parameters of the bus is as follows: Resistance = 8.88 $\mu\Omega$ /ft (both conductors) @ 20 °C, temperature coefficient of resistance = .004/°C, Inductance = 0.157 $\mu$ Hy/ft @ 3" center to center in free air (note centers were changed to 5" during installation, L not yet re-calculated). Res/ft=Res + (Res X Tempco X  $\Delta T$ ). AC resistance = 1.07 m $\Omega$ /ft (both conductors) @ 1MHz.*

#### **4 Controls**

The solenoid power supply is provided with two modes of operation, local and remote. Local operation is provided on the front panel of the power supply and interlocks chassis. Remote operation is provided via networked computer consoles; and crash buttons in the D0 control room. A switch on the front panel selects local or remote operation of the power supply. Likewise, a switch allows for local reset of the interlock chassis. The reversing switch must be manipulated remotely. The power supply is provided with a locking Plexiglas cover to discourage unauthorized or unintentional local manipulation. The common key to the Plexiglas cover shall be under control room supervision. Local operation can not override interlocks and interlocks can not be reset unless they are properly made up.

The remote control system is an extension to the present D0 CRYO control system<sup>14</sup>. This system uses a Texas Instruments series TI555 programmable logic controller (PLC) installed in an I/O chassis (base). The base is installed in a standard 19" equipment rack in the power supply room. The equipment rack also contains the Interlocks and Quench detection/protection chassis. A lockable "end rack" containing terminal strips of female disconnects is installed and all interconnects are made in that end rack. I/O modules installed in the base provide relay contacts; and analog and digital inputs/outputs to the solenoid system. This system is designed and widely used for industrial automation. It is comprised of commercially available hardware and programmed with simple but powerful software tools (TISOFT). The operator interface is provided by commercial software known as Intellution's "Distributed Manufacturing and Control Software" (DMACS). This software runs on IBM PC compatible personal computers similar to

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<sup>14</sup>FERMILAB-TM-1886 "Conceptual Design of a 2 Tesla superconducting solenoid for the Fermilab D0 detector Upgrade", Chapter 9, 5/13/94

those used for cryo controls. DMACS terminals are networked over the Fermilab WAN via TCP/IP protocol.

*This commercial control system is presently in use in D0, P4 and lab A, has been selected for KTEV; and is being considered for an upgrade to CDF. This system has the advantages of commonality with the present CRYO control system, ease of expansion, commercially available; and straightforward implementation. It provides for data and operator input logging, interface to the D0 alarms server and transmittal of status information to the Main Control Room. It implements a voice synthesized auto-dialer and can be operated from home for diagnostics. It also allows the execution of real time control algorithms which would not be possible with the present WAMUS/SAMUS control system. Software professionals **will not** be required to program the solenoid control system. They will however be required to program the present D0 control system to accept the status and alarms data from the solenoid control system.*

#### 4.1 Operator Interface

The operator interface is displayed on the personal computers presently running DMACS software for the cryo system. The operators have a graphical user interface with a process control diagram showing all controlled and monitored points of the solenoid energization circuit.

1. Loss of function of the operators console shall result in a D0 alarm.
2. All operator commands shall be logged in a file.
3. Password protection shall be provided for control.
4. The operator shall have the following controls and monitors:

<b>Control</b>
Reset power supply
Reset interlocks (will not override condition or reset if condition persists)
Set power supply charging voltage
Set power supply final current (Amps)
Turn power supply ON/OFF
Charge solenoid to final current at preselected voltage
Pause/continue charging or discharging
Execute polarity reversal (discharge, reverse, charge)
Execute Fast Dump (This is a crash button )
Trigger/reset quench emulation (diagnostic)
<b>Monitor</b>
Status of power supply - On, off, Local/Remote, polarity (via reversing switch), interlocks, reg. mode, reference, over current
Status of each individual interlock
Display of first interlock to open (first fault)
Status of reversing switch, dump switch power, dump switch position, dump resistor cage lock, dump resistor current
Solenoid current value (0 - 5000A)
Power supply current value (0-5000A)
Power supply voltage value (0 - 15V)
Environment Status - H2O temp, conductivity etc.
Solenoid and lead voltages (diagnostic)
Temperature of chokes, filter diode, dump resistor

## **4.2 Data Logging<sup>15</sup>**

Data logging shall be performed by the control system. The fast, real-time logging of quench data will be done locally by the PLC. The slower, less critical logging of operator input and miscellaneous system status will be done by the DMACS terminal. These log files shall be reachable from the D0 host computers.

### **4.2.1 Operator Input**

Each command entered by an operator shall be time stamped and logged to a file by the DMACS software for record keeping.

### **4.2.2 System Status**

The capability shall exist for certain selected system status information to be time stamped and logged to a file by the DMACS software for record keeping.

### **4.2.3 Quench Data**

Approximately 10 channels of data from the quench detection chassis shall be logged in a circular buffer at a rate of 20 Hz and a depth of 60 seconds. After a quench is signaled, data logging will continue for 30 more seconds whereupon the data will be saved in a file for on-line or off-line analysis. If this data rate is unsatisfactory, a dedicated data-logger may be connected to the buffered voltage tap signals for finer resolution.

## **4.3 Status Information to the Accelerator Control System**

Any status of any entity shall have the potential of being delivered to the accelerator control system. The mechanism is as follows: The accelerator control system has a multiplexed analog to digital converter (MADC) in the D0 control room. The solenoid control system will have analog output ports connected to the MADC. Thus the PLC control system can deliver any control entity as an analog voltage to the Main Control Room via the accelerator control system.

Initially, the following information shall be provided:

1. Solenoid status (on/off)
2. Solenoid status (polarity)
3. Solenoid Current (Amps)

## **4.4 Status information to the D0 Data Acquisition System**

Any status of any entity shall have the potential of being delivered to the D0 data acquisition system (DAQ). The mechanism is as follows: The present cryo control system has a serial link to the D0 DAQ system whereby cryo system data are transferred to the DAQ system for monitoring by the alarms server. This same system will be used for the solenoid controls data merely by the addition of the data points to the transfer block.

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<sup>15</sup>Extracted from 1/17/95 memo, RP Smith, Solenoid Control, Protection, Energization.

#### 4.5 Control Algorithms<sup>16</sup>

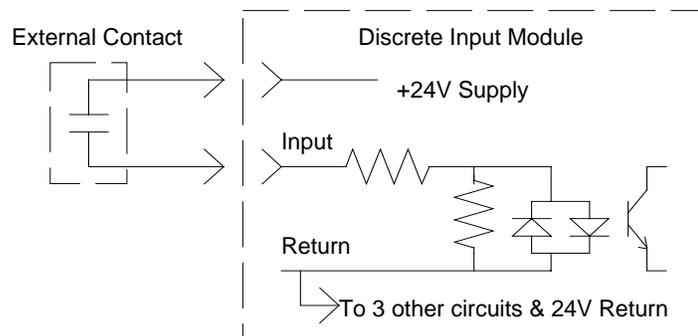
The PLC control system shall be able to implement various control algorithms. For example, the power supply shall have a hardware voltage limiter which sets the maximum charge and discharge voltage of the solenoid. The limit voltage to the hardware circuit shall be provided by a software control loop whose parameters are changeable at the operators console. The control algorithms which shall be implemented are as follows:

1. Execute charging or discharging of the solenoid at voltage XXX to level YYY Amps; where XXX and YYY are operator entered variables. The control system will not allow values for voltage XXX or level YYY which would attempt to exceed pre-determined limits or time constant limitations.
2. Execute slow dump of the solenoid at maximum discharge rate until current has decreased to 50 amps (variable in software). Then trigger fast dump.
3. Pause/continue charging or discharging of the solenoid.
4. Execute a polarity reversal by discharging the solenoid, reversing the polarity and recharging the solenoid at the preselected rate.

#### 4.6 Signal and Cabling Specs<sup>17</sup>

A separate document describes the "Solenoid Endrack Wiring Standards" (see footnote). In general, signals are interfaced as follows:

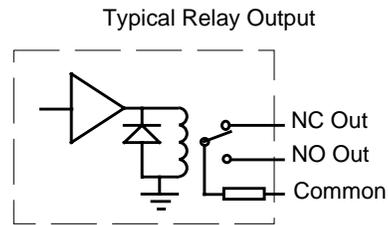
1. All interfacing between the PLC control system and the solenoid energization system are via "faston" type connections to terminal strips mounted in the "end rack" of the equipment rack.
2. Most analog input voltages to the PLC control system and analog output voltages from the control system are unipolar 0 to +10V differential, 12 bits of resolution. A minimal number of bipolar  $\pm 10V$  differential, 12 bit signal input channels are provided.
3. All analog input and output voltages are connected via shielded twisted pair wiring. The shield are grounded only once - at whichever end the signal is grounded.
4. All status inputs to the PLC control system are IEC type 1 which is the input to an optoisolator circuit as shown at right. The control system provides 24Vdc such that the **controlled** component need only provide a relay contact.
5. All status inputs to the PLC control system are wired with shielded, twisted pair wiring with the shield grounded at the controls module only.



<sup>16</sup> See also - Engineering Note - H970408A - R. Hance - Solenoid Control Algorithms

<sup>17</sup> See also - Engineering Note - H961107A - R. Hance - Solenoid end rack wiring standards

6. All discrete outputs from the PLC control system are relay contacts of type form C, isolated, non-latching, rated for 0-120 Vdc @ 1 amp (2A for 1 sec. overload). Max on resistance 50 milliohms.
7. All relay outputs from the PLC control system are wired with shielded twisted pair wiring with the shields grounded at the destination end only (destination provides current supply, thus shield is grounded for electric field shielding).
8. All temperatures are connected into the PLC control system via 3 wire RTDs and RTD interface modules.



#### 4.7 Control Signal List

This table lists the inputs and outputs to the control system and miscellaneous sources. Connection to all sources is via "faston" type male/female disconnects in the end rack attached to the controls/interlocks rack. All control and monitoring is done by standard I/O modules in the PLC I/O chassis (base). These I/O modules contain signal conditioning elements as appropriate thereby eliminating the need for a special controls interface chassis. All remote control and monitoring of the solenoid power system are via these I/O signals. Several signals represent automatic control functions which are implemented in hardware in the interlocks and quench detection/protection chassis. These automatic functions (e.g. fast dump on quench) are supplied to the PLC control system for monitoring. The term "first fault" as used in this list is explained in the interlocks section. Signals are listed in alphabetical order. Refer to the system schematic drawing.

Signal Name	Source/Destination	Signal Type	Description
<b>&lt;25A-2</b> (Current less than 25 Amps in solenoid)	From absolute value module to PCL control system	N/O bi-directional opto isolated contact	Held closed if the current in both the PEI and holec transducers are less than 25 Amps
<b>ABS I-2</b> (Absolute current in solenoid)	From absolute value module to PLC control system	Low impedance, differential, 0 to 10V, 14-bits ADC resolution	Absolute value of current in holec. 10V = 5000 A, 0.305A/lb
<b>Accel Intl</b> (accelerator interlock status)	From interlock chassis to PLC control system	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if accelerator permit interlock is OK
<b>Accel Pmt</b> (Accelerator permit)	From accelerator control to interlock chassis	N/O Isolated relay contact	Held closed accelerator to permit operation
<b>Buf Gnd Sense</b> (buffered ground sense)	From ground fault detector module to PLC control system	Low impedance single ended, 0 to 5V, 14-bits ADC resolution.	Indicates actual resistance to gnd in system. 2.50V = 0 Ohms to gnd 3.30V = 2.5k to gnd 4.58V = 25k to gnd 5.00V = infinite
<b>Bus Flow Sw</b> (Bus flow switch)	From LCW flow switch in bus cooling return line to PLC control system	N/O isolated switch contact	Closed = LCW is flowing in return line from solenoid bus and free-wheeling diode

<b>Bus LCW Sol</b> (bus LCW solenoid)	From PLC control system to LCW solenoid feeding solenoid bus & free-wheeling diode	Switched +24V dc @ 0.5A	+24 to energize the solenoid which routes LCW to the bus & diode
<b>Chimney A HiTRP</b> (Solenoid Buffered chimney lead 3A-4A high trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Chimney A Intl</b> (Chimney lead A interlock)	From interlock chassis to PLC	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if chimney lead A interlock is OK
<b>Chimney A LoTRP</b> (Solenoid Buffered chimney lead 3A-4A low trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Chimney A V</b> (Solenoid Buffered chimney lead 3A-4A voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Chimney B HiTRP</b> (Solenoid Buffered chimney lead 3B-4B high trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Chimney B Intl</b> (Chimney lead B interlock)	From interlock chassis to PLC	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if chimney lead B interlock is OK
<b>Chimney B LoTRP</b> (Solenoid Buffered chimney lead 3B-4B low trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Chimney B V</b> (Solenoid Buffered chimney lead 3B-4B voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Crash Intl</b> (Crash button interlock status)	From interlock chassis to PLC control system	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if crash button interlock is OK
<b>Crash Pmt</b>	From crash buttons to interlock chassis	N/O isolated switches	Closed by crash buttons if all disengaged to permit operation
<b>Cryo Pmt</b>	From cryo control system contact in cryo control room	N/O isolated relay contact	Held closed by cryo control system if all necessary cryo inputs are normal
<b>CT Imbal HiTRP</b> (Solenoid Buffered center tap bridge imbalance high trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 100uV/lb
<b>CT Imbal Intl</b> (center tap bridge imbalance interlock)	From interlock chassis to PLC	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if center tap bridge interlock is OK
<b>CT Imbal LoTRP</b> (Solenoid Buffered center tap bridge imbalance low trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 100uV/lb

<b>CT Imbal V</b> (Solenoid Buffered center tap bridge imbalance voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 100uV/lb
<b>Ctrl Intl</b> (Control system permit interlock status - Cryo & Misc. Sums)	From PLC control system to interlock chassis	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if PLC permit interlock is OK
<b>Ctrl Pmt</b>	From PLC control system to interlock chassis	N/O isolated relay contact	Held closed by PLC to permit operation of system. Based on Cryo, temps, etc.
<b>DC Ovr I Intl</b> (DC overcurrent interlock)	From interlock chassis to PLC control system	N/O Isolated relay contact	Held closed by interlock chassis if DC overcurrent interlock from ABS circuit is OK.
<b>DS Intl</b> (Dump switch interlock status)	From interlock chassis to PLC control system	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if dump switch interlock is OK
<b>DS Lock</b> (Dump Switch cabinet Locked status)	From interlock chassis to PLC control system	N/O Isolated relay contact	Held closed by dump switch if doors are closed
<b>DS Pwr</b> (Dump switch power)	From dump switch to PLC control system	N/O Isolated relay contact	Held closed by dump switch if AC power is present.
<b>DS Reset</b> (Dump switch reset)	From PLC control system to dump switch	N/O Isolated relay contact	Cycled closed by PLC to reset dump switch.
<b>DS Stat</b> (Dump switch status)	From dump switch to PLC control system	N/O Isolated relay contact	Held closed by dump switch if operation normal ie. no dump
<b>Dump 3</b> (Direct control of dump switch)	From PLC control system to dump switch	N/C Isolated relay contact	Normally Closed. Opened to open dump switch
<b>FF D4</b> (First fault) <b>D2</b> <b>D1</b>	From interlock chassis to PLC	N/O bi-directional Opto isolated contacts - Binary number	D4,2,1 form binary word of interlock first fault. closed contacts = 111. See text "Interlock first faults"
<b>FF A Flag</b>	From interlock chassis to PLC	N/O bi-directional Opto isolated contacts	Held open by interlock chassis if no "first fault" present in group A
<b>FF B Flag</b>	From interlock chassis to PLC	N/O bi-directional Opto isolated contacts	Held open by interlock chassis if no "first fault" present in group B
<b>FF C Flag</b>	From interlock chassis to PLC	N/O bi-directional Opto isolated contacts	Held open by interlock chassis if no "first fault" present in group C
<b>Filter Intl</b> (filter interlock status)	From interlock chassis to PLC control system	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if filter interlock is OK
<b>Flow Intl</b> (Flow interlock)	From interlock chassis to PLC control system	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if LCW flow chassis interlock is OK
<b>Flow Status</b> (Flow permit to interlocks)	From PLC control system to interlock chassis	N/O Isolated relay contact	Held closed by PLC switch if LCW flow OK as determined by several factors.

<b>Gate Pmt</b>	From microswitch on room 511 security gate to PLC controls	N/O isolated switch contact	Held closed if security gate in room 511 is closed
<b>Gnd &lt; HiLim</b> (ground resistance is less than hi limit)	From ground fault detector module to PLC control system	N/O isolated relay contact	Held closed if the ground resistance is less than the upper limit pot setting
<b>Gnd &gt; LoLim</b> (ground resistance is greater than lower limit)	From ground fault detector module to PLC control system	N/O isolated relay contact	Held closed if the ground resistance is more than the lower limit pot setting
<b>Gnd Flt Enabled</b>	From Ground fault detector to PLC control system	N/C isolated relay contact	Opened by ground fault detector if GFD is disabled by dump switch (fast dump).
<b>Gnd Flt Intl</b> (ground fault interlock)	From interlock chassis to PLC control system	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if ground fault interlock is OK
<b>Gnd Sense LoLim</b> (ground sense lower limit)	From ground fault detector module to PLC control system	Low impedance single ended 0 to 5V	Indicates setting of ground fault trip pot 3.30V = 2.5k to gnd 4.58V = 25k to gnd 5.00V = infinite
<b>Holec Valid</b>	From Holec chassis to PLC control system	N/O isolated relay contact	Held closed by holec if transducer signal is valid
<b>I&lt;0.1%</b>	From Holec chassis to reversing switch	N/O isolated relay contact	Held closed by holec if current is less than 5 A
<b>Inner Coil V</b> (Solenoid Buffered inner coil 4B-5A voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 5mV/lb
<b>LCW Intl</b> ( Low conductivity water interlock)	From interlock chassis to PLC control system	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if LCW interlock is OK
<b>LCW Pmt</b> (LCW permit)	From LCW chassis to interlock chassis	N/O Isolated relay contact	Held closed by LCW chassis if conductivity OK
<b>Lead A HiTRP</b> (Buffered solenoid vapor cooled lead 1A-2A high trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Lead A Intl</b> (Vapor cooled lead A interlock)	From interlock chassis to PLC	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if vapor lead A interlock is OK
<b>Lead A LoTRP</b> (Buffered solenoid vapor cooled lead 1A-2A Lo trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Lead A V</b> (Buffered vapor cooled lead 1A-2A voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Lead B HiTRP</b> (Buffered solenoid vapor cooled lead 1B-2B high trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Lead B Intl</b> (Vapor cooled lead B interlock)	From interlock chassis to PLC	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if vapor lead B interlock is OK

<b>Lead B LoTRP</b> (Buffered solenoid vapor cooled lead 1B-2B Lo trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Lead B V</b> (Buffered solenoid vapor cooled lead 1B-2B voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/lb
<b>Mag Curr-2</b> (Magnet current)	From Holec transductor to PLC control system via ABS value module	Low impedance, differential, -10 to +10 volt signal. To 13-bit bipolar ADC	Actual bipolar value of current in <b>transductor</b> . 10V = 5000 Amps, -10V = -5000 A. 0.610A/LSB
<b>Outer Coil V</b> (Solenoid Buffered outer coil 4A-5A voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 5mV/lb
<b>PS Curr</b> (Power supply current)	From Power supply transductor to PLC control system	Low impedance, differential, 0 to 10 volt signal. To 14-bit unipolar ADC.	Value of current in <b>power supply</b> . 10V = 5000 amps. 0.305A/lb
<b>PS Ext Intl#1</b> (Power supply external interlock #1)	From power supply to PLC control system	Isolated relay contact	Closed = interlock to PS from interlock chassis is made up
<b>PS Flow Sw</b> (Power supply flow switch)	From LCW flow switch in PS return line, to PLC control system	N/O Isolated switch contact	Closed = LCW is flowing in return line from power supply and filter
<b>PS Int/Ext</b> (Power supply reference status)	From power supply to PLC control system	Isolated relay contact	Closed = external reference in use
<b>PS Intl Comp</b> (Power supply interlocks complete)	From power supply to PLC control system	N/O Isolated relay contact	Held closed by power supply if power supply interlocks OK.
<b>PS LCW Sol</b> (Power supply LCW solenoid)	From PLC control system to LCW solenoid feeding power supply & filter	Switched +24V dc @ 0.5A	+24 to energize the solenoid which routes LCW to the power supply & filter
<b>PS Level</b> (Power supply current level)	From PLC control system to power supply	Low impedance, differential, 0 to 10 volt signal. 12 bits resolution, short and long term drift less than 1/2 LSB.	Programming voltage to power supply. 10V = 5000 amps. Resolution = 1.22 A per LSB.
<b>PS Loc/Rem</b> (Power Supply Local/Remote Status)	From power supply to PLC control system	Isolated relay contact	Closed = Remote controlled operation
<b>PS Off</b> (Power supply off)	From PLC control system to power supply	N/C Isolated relay contact	Momentary, >100ms OPENING turns OFF power supply.
<b>PS On</b> (Power supply on)	From PLC control system to power supply	N/O Isolated relay contact	Momentary, >100ms CLOSURE. Turns ON power supply.
<b>PS On/Off</b> (Power Supply On/Off Status)	From power supply to PLC control system	N/O Isolated relay contact	Closed = Supply is ON
<b>PS Reg Mode</b> (Power Supply Regulation Mode Status)	From power supply to PLC control system	Isolated relay contact	Closed = current regulated mode
<b>PS Reset</b> (Power supply reset)	From PLC control system to power supply	N/O Isolated relay contact	Momentary, >100ms CLOSURE. Resets power supply.

<b>PS VLimit</b> (Power supply voltage limit)	From PLC control system to power supply	Low impedance, differential, 0 to 10 volt signal. 12 bits resolution, short and long term drift less than 1/2 LSB.	Programming voltage to power supply voltage limit input. 10V = 35V limit. Resolution = 0.00854V per LSB.
<b>PS Volts</b> (Power supply volts)	From Power supply to PLC control system	Low impedance, differential, 0 to 10 volt signal.	Value of voltage from <b>power supply</b> . 10V = 35 volts output
<b>QT Imbal HiTRP</b> (Solenoid Buffered quarter tap bridge imbalance high trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 200uV/LSB
<b>QT Imbal Intl</b> (quarter tap bridge imbalance interlock)	From interlock chassis to PLC	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if quarter tap bridge interlock is OK
<b>QT Imbal LoTRP</b> (Solenoid Buffered quarter tap bridge imbalance low trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 200uV/LSB
<b>QT Imbal V</b> (Solenoid Buffered quarter tap bridge imbalance voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 200uV/LSB
<b>Remote QT</b>	From PLC control system to Quench Detector Modules	N/O Isolated relay contact	Closed by PLC to force artificial imbalance in quench detector circuits
<b>Reset Intl</b> (Reset the interlock and quench chassis - will not override condition or reset if condition persists.)	From PLC control system to interlock chassis	N/O Isolated relay contact	Momentary, 1 sec CLOSURE. Resets interlocks.
<b>RS Ctrl</b> (Reversing switch control)	From PLC control system to Rev. Switch	N/O Isolated relay contact	Open = forward, Closed = reverse
<b>RS Intl</b> (Reversing switch interlock)	From interlock chassis to PLC control system	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if reversing switch interlock is OK
<b>RS Pmt2</b>	From reversing switch to control system	Isolated relay contact	Open=switch cycling, closed=switch stopped
<b>RS Stat</b>	From reversing switch to PLC control system	Isolated relay contact	Open=forward, Closed=reverse
<b>RTD01</b> (Power supply interphase transformer temperature)	From power supply interphase xfmr to PLC control system	RTD - 3 wire	RTD mounted on interphase transformer in power supply
<b>RTD02</b> (Power supply bus temperature)	From air-cooled bus above PS to PLC control system	RTD-3 wire	RTD mounted on negative air-cooled bus above power supply
<b>RTD03</b> (Filter choke temperature)	From filter choke to PLC control system	RTD -3 wire	RTD mounted on filter choke negative bus
<b>RTD04</b> (Filter choke temperature)	From filter choke to PLC control system	RTD -3 wire	RTD mounted on filter choke positive bus
<b>RTD05</b> (free-wheeling diode temperature)	From free-wheeling diode to PLC control system	RTD - 3 wire	RTD mounted on free-wheeling diode heat sink

<b>RTD06</b> (Reversing switch positive input temperature)	From reversing switch to PLC control system	RTD - 3 wire	RTD mounted positive input of reversing switch
<b>RTD07</b> (Reversing switch negative input temperature)	From reversing switch to PLC control system	RTD - 3 wire	RTD mounted negative input of reversing switch
<b>RTD08</b> (Dump switch input A temperature)	From dump switch to PLC control system	RTD - 3 wire	RTD mounted on input A of dump switch
<b>RTD09</b> (Dump switch input B temperature)	From dump switch to PLC control system	RTD - 3 wire	RTD mounted on input B of dump switch
<b>RTD10</b> (Dump switch output A temperature)	From dump switch to PLC control system	RTD - 3 wire	RTD mounted on output A of dump switch
<b>RTD11</b> (Dump switch output B temperature)	From dump switch to PLC control system	RTD - 3 wire	RTD mounted on output B of dump switch
<b>RTD12</b> (Dump resistor temperature)	From dump resistor to PLC control system	RTD - 3 wire	RTD mounted on dump resistor
<b>Smoke Pmt</b>	From RMI chassis in control rack to PLC control system	N/O isolated relay contact	Held closed by RMI if smoke detector in controls rack is normal
<b>Sol Stat Curr</b> (Solenoid current value to accel. controls)	From PLC control system to Accel. control system	Low impedance, differential, 0 to 10 volt signal. 12 bits resolution,	Current from Transductor 10V = 5000 amps. Resolution = 1.22 A per LSB.
<b>Sol Stat On/Off</b> (Solenoid On/Off status to accel controls)	From PLC control system to Accel. control system	Low impedance, differential, 0 to 10 volt signal. 12 bits resolution,	0 V = ON 5V = OFF
<b>Sol Stat Pol</b> (Solenoid polarity status to accel controls)	From PLC control system to Accel. control system	Low impedance, differential, 0 to 10 volt signal. 12 bits resolution,	0 V = Forward 2.5V = Cycling 5V = OFF
<b>Steel Pmt</b>	String of limit switches on muon steel	N/O isolated switches	Held closed by limit switches if toroid steel is closed
<b>Steel Intl</b> (Steel interlock)	From interlock chassis to PLC control system	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if toroid steel position interlock is OK
<b>Temp Intl</b> (Temperature interlock status -klixons on bus connectors)	From interlock chassis to PLC control system	N/O bi-directional Opto isolated contact	Held closed by interlock chassis if klixon string interlock is OK
<b>Trans A Intl</b> (Transition lead A interlock)	From interlock chassis to PLC	N/O bi-directional opto isolated contact	Held closed by interlock chassis if transition lead A interlock is OK
<b>Trans B Intl</b> (Transition lead B interlock)	From interlock chassis to PLC	N/O bi-directional opto isolated contact	Held closed by interlock chassis if transition lead B interlock is OK
<b>Trans B V</b> (Buffered solenoid transition lead 2B-3B voltage )	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/LSB
<b>Trans A HiTRP</b> (Buffered solenoid transition lead 2A-3A high trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/LSB

<b>Trans A LoTRP</b> (Buffered solenoid transition lead 2A-3A low trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/LSB
<b>Trans A V</b> (Buffered solenoid transition lead 2A-3A voltage )	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/LSB
<b>Trans B HiTRP</b> (Buffered solenoid transition lead 2B-3B high trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/LSB
<b>Trans B LoTRP</b> (Buffered solenoid transition lead 2B-3B low trip threshold voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/LSB
<b>Trans B V</b> (Buffered solenoid transition lead 2B-3B voltage)	From quench detector chassis to PLC control system	Low impedance, differential, 0 to 10V	5v offset. 50uV/LSB
<b>Xducer Val Intl</b> (current transducer valid)	From interlock chassis to PLC	N/O bi-directional opto isolated contact	Held closed by interlock chassis if current transducer valid interlock is OK

## 5 Interlocks and Quench Detection/Protection

The function of Interlocks, quench detection and control of quench protection devices all reside in a single NIM bin chassis hereafter referred to as the "**chassis**". The chassis contains modules which provide the interlock functions of interlock summing and first fault reporting ; and the quench detection and protection functions of solenoid lead voltage monitoring, imbalance detection and dump switch interface.

This chassis resides in the equipment rack in the power supply room. All connections to this chassis are made via "faston type" disconnects in terminal strips mounted on the side of the equipment rack. This chassis receives inputs from the various sensors and the control system; and provides status to the control system and control to the power supply and dump switch.

1. The chassis is powered by an uninterruptable power supply to provide power in case of loss of AC input.
2. The chassis is hardwired with no easy means for remotely disabling interlocks.
3. The chassis is resettable locally and remotely. However, resets can not override or clear persisting interlock conditions.

### 5.1 Interlocks

Interlocks are generated by three general sources: 1) Internally within the power supply, 2) From various protective devices via the chassis; and 3) From the control system. Interlocks within the power supply and from the protective devices are hardwired and cannot be over ridden. The interlock from the control system is programmable and is based on cryo information and/or refined interpretations of sensor inputs.

There are two categories of interlocks: those that disable the power supply and open the dump switch (fast dump); and those that disable the power supply but do not open the dump switch (slow dump).

Fast dump interlocks represent conditions where it is imperative that the system be discharged as quickly as possible. These interlocks disable the power supply and open the dump switch. A fast dump may require some recovery by the cryo system. Fast dump interlocks are identified in the "List of Interlocks (type FD)".

Slow dump interlocks represent conditions where the system must be inhibited from starting or may discharge at a slow rate if already charged; but need not be as catastrophic as a fast dump. A slow dump interlock shall not open the dump switch. These interlocks merely disable the power supply without opening the dump switch. If charged, the solenoid will discharge through the bus resistance and free wheeling diodes in parallel with the dump resistor. Slow dump interlocks are identified in the "List of Interlocks (type SD)".

**5.1.1 Interlock Modules**

1. "Interlock & First Fault Detector Modules" provide a central point for all interlocks external to the power supply. They are linked to function as one module and provide an isolated output to the control system representing the status of each interlock.
2. The "Interlock & First Fault Detector Modules" provide a "Power supply enable" signal to the solenoid power supply.
3. The "Interlock & First Fault Detector Modules" latch the first interlock source that opens. An encoded "first fault" identifier is provided to the PLC control system. This is in addition to the status outputs described above.

**5.1.2 List of Interlocks**

The following interlocks are hardwired within the **power supply**. These interlocks are separate from those processed through the chassis. The status of these interlocks is displayed by LEDs on the front of the power supply. A summation signal "power supply interlocks complete" is provided to the control system. FD refers to fast dump. SD refers to slow dump.

<b>Internal Power Supply Interlocks</b>	<b>Type</b>	<b>Enabled Condition</b>
Door switch	SD	Enabled if access doors are closed
Interlock chassis permit (see below)	FD or SD	Enabled if all chassis interlocks are OK
AC balance	SD	Enabled if phase currents are balanced
AC current	SD	Enabled if AC input currents within limits
DC current	SD	Enabled if output < 5100 amps (Hi resolution)
SCR condition	SD	Enabled if all SCRs are working
SCR temperature	SD	Enabled if all SCRs are cool
Water temperature	SD	Enabled if internal water temp is normal

The following interlocks are processed by the "Interlocks and quench detection/protection chassis". A summation signal "Interlock chassis permit" is provided to the power supply as listed above. Each of these signals is provided to the control system for remote monitoring. In addition, each of these is provided a second time to the control system by the "first fault" module to provide diagnostic capability.

Interlock Chassis Processed Interrupts	Type	Description
Accelerator permit	SD	Permit from accelerator = closed contact
Bus temperature permit	SD	String of thermal switches on bus closed = OK
Control system permit (see below)	SD	Control system permit = closed contact
Crash buttons permit	SD	String of crash buttons OK = closed contact
Cryo Permit	SD	Contact from cryo control system PLC
DC Overcurrent	SD	Power supply current and holec current below trip level
Dump switch permit	SD	Switch & resistor normal = closed contact
Filter permit	SD	Filter ground/hi pot switch in normal position
Flow permit	SD	LCW is flowing = closed contact
Gate permit	SD	Microswitch on RM511 security gate
Ground fault permit	SD	From GFD module = closed contact if OK
LCW Permit	SD	From LCW system OK = closed contact
Steel closed permit	SD	Muon steel closed = closed contact
Quench detection permit	FD	Quench det. modules OK = closed contact
Reversing switch permit	SD	Reversing switch is not cycling = closed contact
Smoke permit	SD	Contact from RMI in controls rack - smoke detector
Xducer valid permit	SD	Power supply current and holec current agree

The following parameters of the solenoid systems are examined by the **control system** software and summed to produce the signal "Control system permit" which is fed to the interlock chassis. The signal is in the form of a normally open relay contact which is held closed if all conditions are satisfactory. The term "OK" will be replaced with quantities as this specification develops. These values shall also be displayed at the operators console.

Parameter	Type	Description
VC lead temp	SD	Vapor cooled lead temperatures OK
Vapor Cooled lead flow	SD	Vapor Cooled lead flow OK
Cryostat vacuum pressure	SD	Cryostat vacuum pressure OK
Radiation shield temperature	SD	Radiation shield temperature OK
Solenoid cold mass temperature	SD	Solenoid cold mass temperature OK
Control dewar helium level	SD	Control dewar helium level OK
Helium supply temp	SD	Helium supply temp OK
Helium supply dewar level	SD	Helium supply dewar level OK
Helium pressure in solenoid	SD	Helium pressure in solenoid OK
Helium flow rate in solenoid	SD	Helium flow rate in solenoid OK
De-centering forces	SD	De centering forces OK
PLC	SD	Programmable controller OK
UPS battery	SD	UPS battery OK
Vapor cooled lead voltage	SD	Software limit on vapor cooled lead voltage

### 5.1.3 Interlock First Faults

There are three interlock modules. Each module monitors eight interlocks for a total capability to monitor 24 interlocks. Each module has "first fault" circuitry which latches and encodes the first of its eight interlocks to open. The encoded outputs are "wire-or'd" together. The three modules are linked together such that the first interlock to occur in any of the modules will lock out the other two modules. The PLC monitors and decodes the wire-or'd binary word from the three interlock modules. A flag bit (closed contact) in each group indicates valid data. Thus the PLC is provided information as to which interlock occurred first. The table below lists the grouping and encoding of interlock first faults. FF A, FF B and FF C refer to first fault module A, B and C respectively. D4,2,1 refer to the encoded contacts. The "flag" contact (not shown) must be closed to indicate valid data. The system schematic contains further information. A "0" is an open contact and a "1" is a closed contact.

FF A	D4,2,1	Description			100	Crash Pmt
	000	QT Imbal Pmt			101	LCW Pmt
	001	CT Imbal Pmt			110	Accel Pmt
	010	Lead B Pmt			111	Ctrl Pmt
	011	Trans B Pmt				
	100	Chimney B Pmt				
	101	Chimney A Pmt	FF C	D4,2,1		Description
	110	Trans A Pmt			000	Cryo
	111	Lead A Pmt			001	Access Gate
					010	Smoke
FF B	D4,2,1	Description			011	DC Over I Pmt
	000	Filter Pmt			100	Xducer Val Pmt
	001	Temp Pmt			101	Rs Pmt
	010	Flow Pmt			110	Gnd Flt Pmt
	011	Steel Pmt			111	DS Pmt

### 5.2 Quench Detection

The solenoid is specified to be capable of absorbing its stored energy without an external protection resistor<sup>18</sup>. It is further specified to be capable of discharging safely from design operating current using an external protection resistor. The purpose of the quench detection system is to merely detect the occurrence of a loss of superconductivity within the solenoid, and then to set the power supply to zero output as quickly as possible. The power supply must be set to zero to avoid damage which might occur if current were continually delivered to the solenoid's superconductors after they have quenched and developed resistance. The quench detection system is in the form of voltage taps on the solenoid and its vapor cooled, transition and chimney leads; and quench detection and interlock modules in the "Interlocks and Quench Detection Chassis".

The quench detection modules monitor voltages on the leads and within the solenoid for imbalances which signal a loss of superconductivity. Upon detection of an actual quench or receipt of a remote quench emulation command, the quench detection modules will signal the interlock circuits which will disable the power supply and open the dump switch. Opening the

<sup>18</sup> Technical Specification for a 2 Tesla superconducting solenoid magnet for D0 at Fermilab E823-94-01 Rev. 0 5/31/94, rev 7/1/94.

dump switch removes the power supply, filter, free-wheeling diode, and reversing switch from the circuit and leaves the "Dump Resistor" in series with the dc bus and the solenoid. The power supply shuts off and "free wheels" while the stored energy of the filter and power supply dissipates in the filter snubber networks and component resistance. The stored energy in the solenoid coil and DC bus dissipates in the DC bus and the "Dump Resistor". Although not necessary for safe operation (as explained in the first sentence), the dump resistor speeds up the discharge process and dissipates the energy away from the solenoid and its cryo support system – hopefully reducing the recovery time.

### **5.2.1 Quench Detection Modules<sup>19</sup>**

Isolation amplifier modules installed in the "Interlocks and Quench Detection/Protection Chassis" provide signal conditioning for the quench detection function and control of the dump switch. These identical modules serve as either lead voltage conditioners or imbalance detectors. These modules are interfaced within the chassis with the "Interlock Summation and First Fault" modules as appropriate.

1. The "Lead Voltage" modules and the "Imbalance Detector" modules within the chassis monitor the voltage taps from the solenoid for the purpose of detecting and acting on the formation of a quench in the superconducting leads or coils.
2. The "Lead Voltage" modules and the "Imbalance Detector" modules provide buffered and scaled differential analog signals to the control system of all inputs from the solenoid.
3. The "Lead Voltage" modules and the "Imbalance Detector" modules provide test points on the front panel for monitoring or fast data logging of the buffered analog signals.
4. The "Lead Voltage" modules and the "Imbalance Detector" modules provide a means for internal adjustment of sensitivity so appropriate levels can be set once field data has been acquired and analyzed.
5. The "Lead Voltage" modules and the "Imbalance Detector" modules accept a relay contact input which can be opened by the control system to force a quench emulation for testing. A quench emulation forced by the control system will have all the ramifications of an actual quench (except the solenoid does not actually quench) i.e. it disables the power supply and triggers a fast dump.
6. The "Lead Voltage" modules and the "Imbalance Detector" modules provide signals to the "Interlock Summation and First Fault" modules, which then indicate the source of a quench indication i.e. solenoid voltages or control system contact.
7. Test points on the solenoid interface allow voltages to be injected for testing the quench detection circuits by emulating lead voltage or by unbalancing the solenoid bridge circuits. The solenoid is connected but unpowered during these tests.
8. The "Interlock Summation and First Fault" modules control the dump switch by consolidating the interlocks from all sources associated with fast dumps. In addition, the "Imbalance Detector" modules and the PLC control system directly control the dump switch to provide redundancy.

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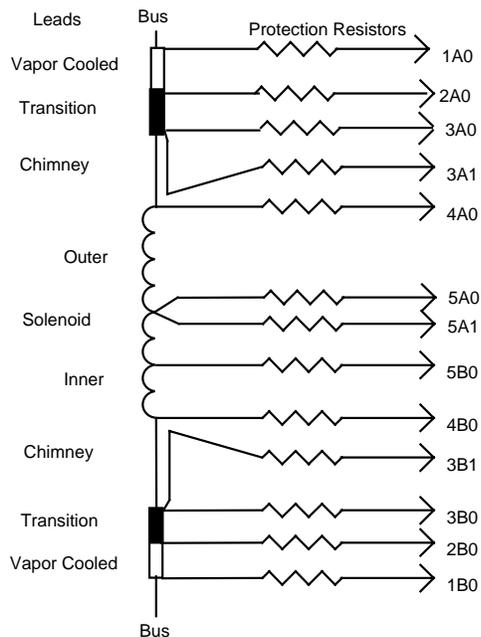
<sup>19</sup> See also - Engineering Note - H960624A - R. Hance - Design review of Quench Detection and Interlocks Modules

### 5.2.2 Voltage Taps on Solenoid<sup>20</sup>

Quench detection is performed by the means of monitoring voltage taps on the solenoid leads and coils. An increase in differential voltage other than due to  $\Delta I/\Delta T$  from charging and discharging shall indicate loss of superconductivity and require immediate action by the quench detection system.

The solenoid provides voltage signals from each end of the vapor cooled leads, transition leads, and chimney leads to measure voltage drop across the leads. In addition, there is a voltage signal from each end of the solenoid coil, one in the middle; and one halfway between the middle and one end.

There are current limiting resistors (10K  $\Omega$ ) in series with the voltage leads and located very near the lead attachment points. The signals are then cabled to the interlocks and quench detection/protection chassis located in the power supply room with multiconductor, shielded, high voltage cable. Isolation amplifiers in the chassis receive the following signals in various differential combinations:



<sup>20</sup> See also - Engineering Note - H960314A - R. Hance - Solenoid Quench Detector Signals

### **5.2.3 Signals from Solenoid to Quench Detection Circuitry**

As shown above, the following signals from the solenoid are monitored by the quench detection chassis:

- Differential voltage across each vapor cooled lead (1A0-2A0, 2B0-1B0).
- Differential voltage across each transition lead (2A0-3A0, 3B0-2B0).
- Differential voltage across each chimney lead (3A1-4A0, 4B0-3B1).
- Differential voltage across the outer coil and chimney lead A (3A1,5A1).
- Differential voltage across the inner coil and chimney lead B(5A0-3B1).
- Differential voltage - Center tap bridge imbalance. One side is center tap of coil, other side is center of balanced bridge between outside leads of coil (4A0-5A0-4B0).
- Differential voltage - Quarter tap bridge imbalance. One side is quarter tap of coil, other side is quarter point of balanced bridge between outside leads of coil (4A0-5B0-4B0).

### 5.2.4 Signals from Quench Detection Circuitry to PLC Control System

All of the previously defined signals will be buffered, scaled and presented to the PLC control system for monitoring.

The scaling of the signals as presented to the PLC control system is as follows. Note that all signals have a +5 volt offset. This is to provide fail-safe indication of cable integrity and amplifier functionality. Scale factors were chosen to provide maximum resolution of expected signals, equalize performance of each amplifier channel; and provide interchangeability of amplifier modules:

Signal	Scaling Information	Frequency Response
Differential voltages across vapor cooled leads, transition leads and chimney leads.	0-10V. Voltage to PLC = $(V_{in} \times 50) + 5V$ . Resolution of 12-bit ADC = 50 $\mu$ V/bit.	Step response = 1.2 msec. Freq. response = -3db @ 250Hz, -6db @ 500Hz
Differential voltage across the outer coil + vapor cooled lead A, and inner coil + vapor cooled lead B.	0-10V. Voltage to PLC = $(V_{in} \times 0.5) + 5V$ . Resolution of 12-bit ADC = 5 mV/bit.	Step response = 1.2 msec. Freq. response = -3db @ 250Hz, -6db @ 500Hz
Differential voltage representing Center tap bridge imbalance.	0-10V. Voltage to PLC = $(V_{in} \times 25) + 5V$ . Resolution of 12-bit ADC = 100 $\mu$ V/bit.	Step response = 1.2 msec. Freq. response = -3db @ 250Hz, -6db @ 500Hz
Differential voltage representing Quarter tap bridge imbalance.	0-10V. Voltage to PLC = $(V_{in} \times 12.5) + 5V$ . Resolution of 12-bit ADC = 200 $\mu$ V/bit.	Step response = 1.2 msec. Freq. response = -3db @ 250Hz, -6db @ 500Hz
Differential voltages representing Hi and Lo trip thresholds for vapor cooled, transition, and chimney leads.	0-10V. Voltage to PLC matches lead signals described above.	DC voltage
Differential voltages representing Hi and Lo trip thresholds for Center tap imbalance.	0-10V. Voltage to PLC matches Center tap voltage described above.	DC voltage
Differential voltages representing Hi and Lo trip thresholds for Quarter tap imbalance.	0-10V. Voltage to PLC matches Quarter tap voltage described above.	DC voltage

### 5.2.5 Signals from Quench Detection Circuitry to Interlock Circuitry

The following signals are processed by the Quench Detector Chassis with comparators that have manually adjustable thresholds (normally inaccessible potentiometer adjustment). The discriminated signals are routed to the interlock chassis to provide interlock signals to initiate the FAST dump processes. Note that all voltages are used except for the differential voltages across the outer and inner coil.

- Differential voltage across each vapor cooled lead.
- Differential voltage across each transition lead.
- Differential voltage across each chimney lead.
- Differential voltage - Center tap bridge imbalance. One side is center tap of coil, other side is center of balanced bridge between outside leads of coil.
- Differential voltage - Quarter tap bridge imbalance. One side is quarter tap of coil, other side is quarter point of balanced bridge between outside leads of coil.

### 5.2.6 Special Considerations

In addition to the processing discussed above, some signals are hardwired to provide an emergency FAST DUMP signal directly to the dump switch. This is for the purpose of providing a redundant level of solenoid protection:

- Differential voltage - Center tap bridge imbalance. One side is center tap of coil, other side is center of balanced bridge between outside leads of coil .
- Differential voltage - Quarter tap bridge imbalance. One side is quarter tap of coil, other side is quarter point of balanced bridge between outside leads of coil.

### 5.2.7 Redundancy

It is imperative that the power supply be set to 0 Amps or turned off if a quench occurs. Redundancy shall be provided to preclude missing a quench due to the failure of a single point ie. voltage tap, differential amplifier, comparator or interlock channel.

Refer to the voltage tap diagram and signal descriptions. The delicate **chimney leads** have several redundant paths for sensing a quench. Each lead's differential voltage is monitored directly by an isolation amplifier. In addition, lead A is included in the amplifier circuit isolating the outer coil's differential voltage, and lead B is included in the amplifier circuit isolating the inner coil's differential voltage. The isolation amplifiers route their signals through separate buffers to hardware threshold comparitors and to the PLC for potential software threshold comparison. The hardware comparitors are the primary path by design. However, the PLC may be programmed with lower thresholds or it may just act as a backup to preclude hardware comparator failure. The isolation amplifiers utilize offset circuits to preclude a voltage tap, amplifier or cable failure going undetected by either the hardware or software path. Thus from the foregoing discussion, each **chimney lead** has two hardware and two software channels.

The **vapor cooled leads** and **transition leads** each have one hardware channel with software providing redundancy by comparing the voltages across the two leads. Each path includes sensing of voltage tap, amplifier or cable failure as described above.

The **solenoid** itself has 5 redundant paths of protection: Two hardware channels are implemented using the center tap bridge imbalance circuit and the quarter tap bridge imbalance circuit. Two software channels are possible using the above signals. And finally, a software channel is implemented by differentially summing the inner and outer coil voltages. Each path includes sensing of voltage tap, amplifier or cable failure as described above. The solenoid coil itself has sufficient resistance to limit the maximum current from the 15V power supply to safe levels ( $15V/1.58\Omega=9.49A$ ). A full discussion of redundancy is provided in engineering note H971203B - Solenoid Quench Protection System Single Device Failure Analysis.

### 5.3 Dump Switch<sup>21</sup>

A mechanical switch is used in order to minimize the  $I^2R$  losses inherent in a solid state switch. The switch is located in series with the power supply and solenoid; and downstream of the reversing switch. It is normally closed to provide a current path between the power supply and the solenoid. The switch opens when triggered to separate the power supply, filter and reversing switch from the solenoid and its discharge (dump) resistor.

1. The switch is an ABB FBK-S-8000 which is rated at 8000 Amps/1000 Volts
2. The switch shall open when signaled by the opening of one of two contacts in the "Interlock and Quench Detection/Protection" chassis; or the opening of a contact from the PLC control system. The switch shall close in response to a contact closure by the PLC when and if all contacts from the above sources are closed.
3. The switch shall provide a closed contact to the "Interlock and Quench Detection/Protection" chassis and the PLC control system when it is in the normal operating mode.

### 5.4 Dump Resistor<sup>22</sup>

An air-cooled dump resistor is placed in parallel with the solenoid to absorb the solenoid energy when the dump switch is opened. This resistor serves to discharge the bus inductance as well as the solenoid magnetic field (5 MJ). The resistor is fabricated of stainless steel bars and provides a resistance of  $48 \times 10^{-3} \Omega$  (including the bus resistance to the solenoid) at 20°C to limit the fast discharge voltage to 250V maximum. Its temperature may rise to about 100°C during a discharge of 5 MJ. The design of this resistor is discussed in other documents<sup>23</sup>.

1. The resistor shall recool in about 30 minutes following a discharge.
2. The midpoint of the dump resistor is grounded (through a resistor) to limit solenoid coil voltages to less than 125V peak during a discharge from 5000 A.

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<sup>21</sup> The dump switch is detailed on Sheet-10 of schematic drawing 3823-111-ED-330052.

<sup>22</sup> The dump resistor is detailed on Sheet-10 of schematic drawing 3823-111-ED-330052.

<sup>23</sup> See also Engineering Notes H960814A - R. Hance (author W. Jaskierny) - Solenoid Dump Resistor Design; and H960917B - R. Hance - Solenoid Dump Resistor Review.

## **6 Ground Fault Protection**

1. A 2500 Ohm resistor in series with the grounded center tap of the dump resistor limits ground fault currents to less than 50 milliamps.
2. A "Ground Fault Detector" module<sup>24</sup> in the "Interlock and Quench Detection/Protection" chassis monitors the center tap and provides a closed contact to the interlock circuits if the resistance to ground is between settable limits.

## **7 Revisions to this Document**

The following significant changes have been made to this document since the original issue date. Each of these changes has been integrated into the text already. Therefore, the document is correct as it reads. The changes are listed here merely to provide a history.

1. 3/8/95 - The data logging rate of the solenoid voltage taps was changed from 1 Khz to 20 Hz. A dedicated data logger may be used if finer resolution becomes necessary.
2. 3/8/95 - Added analog signals to provide solenoid status to Accel. control system.
3. 5/26/95 - Changed location of energization equipment. Revised control signals list. Added drawing number for schematic. Change drawing and designation of P taps for quench detection. Revised interlocks to represent evolution of system design.
4. 2/16/96 - Changed description of solenoid Ptap signals to reflect evolution of design of the quench detector circuits.
5. 3/5/96 - Change all references to old series dump resistor to reflect newest architecture decision which incorporates a parallel dump resistor. Also changed from "T" bus serving both assembly hall and collision hall, to two single buses -- one for each area.
6. 5/6/96 - Added detailed descriptions of quench detector voltage signals, levels and frequency response.
7. 5/8/96 - Clarification of quench detection and addition of QD threshold signals to PLC.
8. 6/5/96 - Updated all controls signal names to reconcile schematic. Added section on interlock first faults.
9. 6/7/96 - Renamed two control signals (Intl Pwr & Reset Intl).
10. 6/12/96 - Clarification of control signal names and states.
11. 6/24/96 - Changed crash button interlock from "fast dump" to "slow dump" as result of engineering review of interlock module.
12. 11/25/96 - Updated to current information for electrical safety review. No significant changes.
13. 1/21/97 - Change ground fault current maximum from 40A to 50mA.
14. 1/30/97 - Change solenoid taps numbers and expound on quench detection redundancy.
15. 1/31/97 - Add power supply requested regulation and readback precision.

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<sup>24</sup> The ground fault detector module is detailed on Sheet-14 of schematic drawing 3823-111-ED-330052. See also Engineering Note - H970627A - R. Hance - Solenoid Ground Fault Detector Module Design Review.

16. 5/30/97 - General review and update of control signals and particulars. No architectural or philosophical changes.
17. 6/26/97 - Update of control signals to include design of ground fault detector module.
18. 7/2/97 - More ground fault detector control signals added.
19. 7/12/97 - Added "holec valid" and " $I < 0.1\%$ " signals to control signal list.
20. 8/26/97 - Added reversing switch status signal to control list.
21. 9/23/97 - Changed polarity of Remote QT from open contact causes trip, to closed contact causes trip.
22. 9/26/97 - Change the name of some control signals to match schematic.
23. 10/15/97 - Removed "Filter Status" input to control system. This signal is redundant to "Filter Pmt Intl".
24. 11/10/97 - First round of updates to "as built spec" ie. replace "shall be" to "are", "is" etc. Some minor additions to control signal table to match schematics.
25. 11/12/97 - Clarify purpose in "Quench Detector" section in compliance with recommendation from electrical safety review committee.
26. 12/02/97 - Change number of pages in schematic to 17.
27. 12/15/97 - Change system block diagram to correctly position reversing switch.
28. 01/06/98 - Update documentation index.
29. 02/17/98 - Add Cryo, Access Gate, Smoke to first fault table.
30. 02/18/97 - Update documentation index.
31. Separated "ground fault" protection from "Dump Resistor" section to get it into the table of contents.
32. Changed web address for documents to <http://www-d0.fnal.gov/~hance/solenoid.htm>
33. Changed polarity of "Interlock First Fault" description for clarity and compliance with PLC convention. Also made several minor changes through out.
34. 01/11/99 - Added reference in documentation index to operating procedures (H980826B)