

Rick Hance Engineering Note

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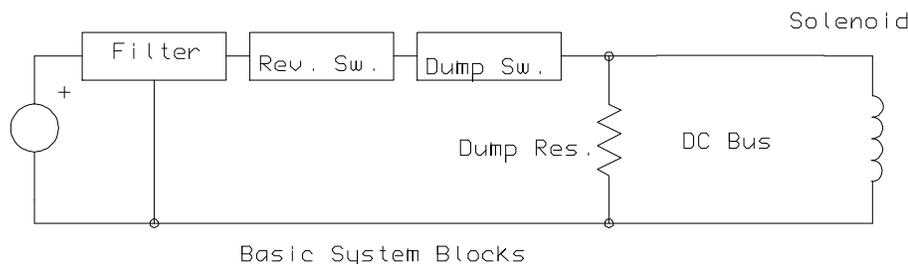
Project: Solenoid Energization and Controls
Doc. No: H960703A.DOC

Subject: Power Supply Filter Design

Introduction

The solenoid is to be powered by a 150 kW 12-phase thyristor power supply operating at approximately 15V and 5000A. The fundamental ripple frequency is 720 Hz with a possible ripple voltage of as high as 4.67 Vrms¹ for the 15V supply. The 720 Hz ripple and its harmonics are differential mode noise. The differential noise is not expected to be a problem given that the solenoid is a .48 Hy inductor in parallel with a 3.2 ohm resistance and shunted with 2 nF of capacitance². Furthermore, the detector electronics are relatively immune to noise at this low frequency. However, we do expect potential interference to the experiment's electronics from the high frequency common mode noise generated by dv/dt and di/dt as the power supply thyristors are triggered during normal operation. These spikes are expected to be in the order of 30 Vpp 10 KHz to 500 KHz damped oscillations³ with harmonics extending out toward 2 MHz. Thus a filter must be designed to reduce the 10 KHz and higher common mode noise being conducted out of the power supply along the DC power bus to the solenoid.

Our filter design is concerned with passing current from DC up to about 100 Hz (to avoid interfering with the power supply's current regulation loop) and attenuating all other frequencies. The amount of attenuation is strictly a function of the impedance of the filter with respect to the power supply, and the impedance of the load with respect to the filter. We have no need to match impedances in order to transfer maximum power at any frequency other than DC. Thus we want our filter to represent a low impedance to the power supply; and a high impedance to the load. The load consists of the reversing switch, dump switch, dump resistor, DC bus and finally, the solenoid itself.



Filter Specification:

The first step in designing a filter is normally to define its specifications. This consists of defining the input and output impedances, the attenuation desired; and the required behavior in the pass band (phase shift etc.). Defining the input impedance requires characterization of the power supply. Defining the output impedance requires characterization of the load. Defining the attenuation requires both of the foregoing and an additional

understanding of the final coupling mechanisms of noise to the experiment's electronics. Power supply and load characterizations are confounded by physical dimensions and operating levels. For example, the 15V 5000A power supply is comprised of components large enough to have significant parasitic reactances and resistances. These are likely to introduce large errors in the calculation of impedance and the construction of a mathematical model. Furthermore, active devices in the output circuits render the impedance rather dynamic i.e. it changes with operating level, source voltage etc. Likewise for the reversing switch, dump switch, dump resistor, DC bus; and especially the solenoid itself. For example, the AC resistance of the bus due to skin effect is a function of the frequency of the noise. An accurate characterization could only result from actual measurements which cannot be made until the installation itself is finished (unavailability of the solenoid, difficulty of configuring power supply for test etc.).

Thus we must choose a less theoretical and more pragmatic approach to the filter design while not discarding filter theory completely. We have available to us various coils and capacitors. Furthermore we have some understanding of voltage and impedance levels from our own measurements and the previous work of others. Our approach is thus to assemble a filter based on available parts, common knowledge; and first order mathematical models we have derived but may not have been able to verify. Then analyze the filters performance with respect to our best efforts at calculating a load model. This document will describe the filter design and the conclusions used to reach it.

Some Considerations:

The problem consists of determining what value and topography of capacitors to use with the coils to get maximum effectiveness against common mode noise while still providing some differential mode noise attenuation. Some issues of concern are as follows:

- The wavelength of the maximum frequency of interest (2 MHz) is 150 meters (492 feet). The DC bus from the power supply to the solenoid is expected to be about 200 feet including the filter inductor windings. Given that the bus length is a significant fraction of a wavelength, **transmission line** effects may contribute to final performance.
- Since the frequency spectrum of the noise exceeds 1 MHz, parasitic reactances and skin effects can be expected to be significant. Thus circuit modeling, design and analysis of the power supply, filter, DC bus and solenoid based solely on **lumped parameters** is not likely to be completely valid. Nevertheless, the solenoid and bus must be modeled using lumped parameters in order to have some starting point to work from.
- Two fixed air core coils of 25 UHy each (24 pf shunt capacitance and 19milli-Ohms series resistance at 10 kHz)⁴ are available for use as chokes.
- In order to avoid problems with the power supply regulation, any filter (and distributed reactances from other circuit components) placed between the power supply and its current sampling transducer must have its phase and amplitude response understood up to at least 100 Hz. To prevent power supply oscillations, the total phase shift in the regulation loop which includes the filter must be less than 360 degrees at all frequencies up to and including the point at which the loop gain decreases past zero. Good phase and amplitude response would be a maximally flat, Butterworth like response.

Modeling of the Power Supply:

The most important factor in the initial filter synthesis is to understand the characteristics of the power supply. Specifically, its impedance and noise spectrum. We wish to formulate a Thevenin equivalent circuit which is as accurate as possible at the 15V 5000A operating point.

- The common mode noise source -- which is due to di/dt and dv/dt from thyristors in the power supply -- is a high impedance source. Essentially a capacitance roughly equivalent to the power transformer secondary to frame capacitance⁵. Thus a low impedance pi filter is implicated. The "damped oscillation" described by Visser is what would be expected from a parallel LC circuit in series with a step generator. This indicates that the capacitance is in parallel with the output inductance of the supply and is logical given the construction of the supply.
- We were unable to measure the capacitance of a PEI 150 kW transformer. However we did measure a PEI 240 kW transformer. The PEI 150 is physically smaller than the PEI 240 kW but has a different winding topography (square conductors instead of round). We are concluding that the smaller size of the PEI 150 would be offset by the more even spacing of the square conductors versus round. The total capacitance to the

frame (ground), measured as "seen" by an SCR as it fires, was measured to be 6.65 nF @ 10 KHz. We will use 10 nF in our common mode model to include other stray capacitance from the SCRs to frame ground etc. The capacitance is part of a voltage divider in the final filter circuit. Choosing the larger source capacitance represents the worst case (less output attenuation).

- The expected common mode noise voltage is determined from information gathered in the past on other supplies⁶. This is typically a damped oscillation of 10 KHz to 500 kHz with an amplitude roughly equal to the DC operating voltage of the power supply i.e. 15 Vpp for a supply operated at 15 Vdc. We will base our design on 50 KHz. This is because it will be shown later to be somewhat substantiated by other observations. We will, of course, evaluate the performance at all frequencies including 10 KHz during the final SPICE analysis.
- Thus the output of the supply for a common mode source would be in series with a parallel LC circuit resonant at 50 KHz. With 10 nF of capacitance, the inductance is calculated to be 10 UHy, which is at the low end of the range specified by Visser⁷. The lower value is more likely than a higher value given the low voltage, high current configuration of the supply.
- The differential mode noise source - which is due to the firing angle ripple from thyristors in the power supply is a low impedance source, essentially a zero impedance voltage source in series with a 10 to 100 UHy inductor⁸. The inductor represents a series impedance to the filter circuit.
- Thus we can use the same source impedance in our differential mode model as we did for our common mode model. The 10 nF capacitor in parallel with the inductor has a high impedance and minimum effect at the low frequencies of concern for differential mode noise.

Modeling of the load:

The load consists of the reversing switch, dump switch, dump resistor, DC bus and solenoid. The DC bus and solenoid were analyzed and modeled to produce first order lumped component equivalent circuits. However, parasitic reactances and skin-effect resistance of the DC bus; and the parasitic reactances of the large solenoid will clearly diminish the validity of the model at the higher common mode frequencies. The insertion loss of the filter will depend upon the ratio of the filter impedance to the load impedance. For any given filter impedance, performance will be best with a low impedance load such that the noise voltage is predominately dropped across the filter chokes and returned to source by the filter capacitors. This assumes, of course that the filter and load impedance are not of opposite sign. For example, if the filter and load comprise a series resonant circuit, the noise across the load could actually increase dramatically. Thus we need to determine a value to use as a load impedance for filter synthesis. The reversing switch and dump switch should have minimal resistance and reactance compared to the dump resistor, DC bus and solenoid. We will reluctantly ignore them. Some considerations of the dump resistor, DC bus and solenoid are as follows:

- The dump resistor must be considered separately for its effect on common mode noise and differential mode noise. It is connected differentially across the input of the bus nearly at the output of the filter; but has no immediate connection to the common mode noise return point except through the center connected ground fault current limiter circuit. This resistor is only 48 milli-ohms at DC; but consists of 144 feet of 1/4" X 4" stainless steel bar stock and likely has considerable inductive reactance and skin-effect resistance at 50 KHz and above. Capacitance will not be a factor since the stainless steel conductors are arranged in a 12 conductor double-back configuration which places 11 capacitors in series thus reducing their effect ($C = 11 / [\text{permittivity} \times \text{area} / \text{distance}] = 0.6 \text{ pf}$). Thus the dump resistor is considered to be a 48 milli-ohm resistor for differential mode noise and a high impedance (open circuit) for common mode noise.
- The length of the DC bus is a significant fraction of the wavelength of the highest common mode frequencies which may produce unanticipated reflections and voltage nodes. It is not clear if any lumped component model is even usable to the first order at the highest frequencies. However, at the lower end of the spectrum, the DC bus of 150 feet provides 1.3 milli-ohms resistance at DC to the differential mode noise path (150' of bus = 300' of conductor); and it provides a .75 milli-ohms DC resistance to the common mode noise return path (150' of conductor). However, a first order analysis⁹ @ 50 KHz reveals series inductance to be about 12 UHy per conductor with the inductive reactance in the order of 3.8 ohms per conductor; and series resistance due to skin-effect of 41 milli-ohms (per conductor). As frequency increases, the inductance will remain the dominate factor. The analysis of the bus capacitive reactance @ 50 KHz reveals it to be in the order of 1.3 K ohms and is thus not considered a major factor. As frequency increases, the capacitive reactance would decrease resulting in improved filter performance as long as resonances do not occur. The

actual model normalized at 10 KHz will be used when the filter performance is analyzed so that the effects of the capacitance can be determined. For the filter design process, the DC bus is considered to be a 1.3 milli-ohm resistor for differential mode noise and a 40 milli-ohm resistor in series with a 12 UHy inductor for common mode noise.

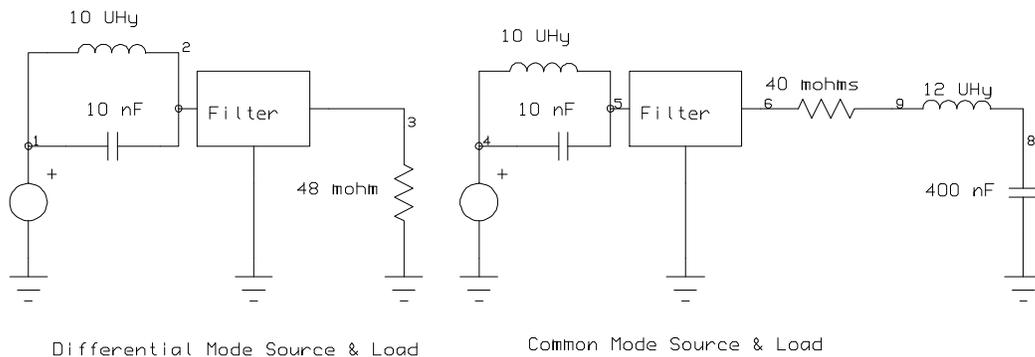
- The solenoid by virtue of its large dimensions, is likely dominated by parasitic impedances. However, a first order model of the solenoid¹⁰ and subsequent analysis at differential mode noise frequencies indicates it to be essentially resistive with a value of 3.2 ohms. Its model being dominated by the outside shell which acts as a shorted secondary turn. The differential impedance magnitude is relatively constant throughout the differential mode frequency range. An analysis of the common mode configuration and frequencies indicates the solenoid to be essentially capacitive due to the winding-to-shell capacitance of about 400 nF and the grounding of the shell. If this model were possibly correct, then At 50 KHz, the reactance would be about 8 ohms capacitive and would drop to < 0.2 ohms at 2 MHz. Thus the solenoid is considered as 3.2 ohms resistive to differential mode noise and 400 nF capacitive to common mode noise.

For the initial filter design, we are looking for the worst case load (highest impedance). This is because the higher the load impedance, the lesser will be the effect of the filter. The inductive reactance of the DC bus becomes a factor at common mode frequencies as does the resistance due to skin effect. The wavelength at 50 KHz is 19.6K feet. Thus transmission line effects will not be significant. However, at 2 MHz, the wavelength is 491 feet and at this point, transmission line effect could be a factor. Especially given the severe mismatch between the bus characteristic impedance of 98 ohms¹¹ and the solenoid impedance due to capacitance.

The capacitive solenoid and inductive/resistive bus would appear to dominate for the common mode frequencies up to 2 MHz -- remembering of course the previous caveats and disclaimers about the validity of the models.

The 48 milli-ohm dump resistor across the input to the bus/solenoid circuit would clearly dominate at the differential mode frequencies (720 Hz plus harmonics).

Thus we will use the following simplified equivalent circuits as a starting point for the filter design. The common mode equivalent circuit is based on 50 KHz because that is the most likely dominant noise frequency. However, we will use more extensive circuit models derived at 10 KHz for the analysis. The primary difference in the bus models being the resistance due to skin effect. The skin effect resistance increases with frequency providing more noise attenuation. The 10 KHz analysis will thus show the worst case performance.



Filter Design - Common Mode

Common mode noise is by definition common to both the + and - legs of the supply and relative to the power supply frame which is grounded. Thus the filter can be designed for one leg and duplicated for the other. The source impedance is high and capacitive, therefore we will use a pi filter topology. The pi filter has a low input impedance resulting in a high retention of the noise within the source due to the mismatching of impedances.

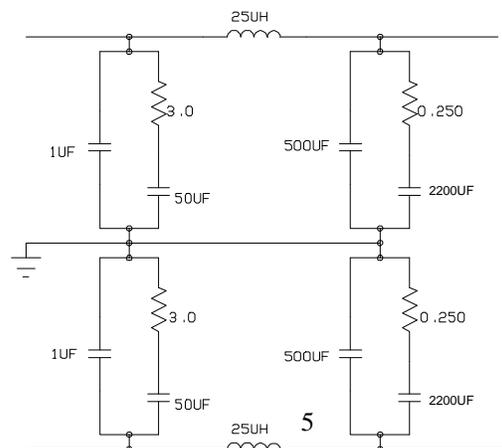
Input Capacitive element -- The filter input capacitance will provide the shortest return path for common mode noise currents. We choose from our ample supply of 1 UF 600 Vdc low ESR capacitors for the input of our pi filter. One of these in each leg can be easily mounted inside the power supply to minimize the return path. These capacitors are useful to about 1.5 MHz¹². These capacitors must accommodate the slight polarity reversal that occurs when the power supply is turned off or the dump switch is opened; due to the free wheeling diode forward voltage drop (1/2 of 1.1V). We also specify 0.01 UF 3 kV capacitors in parallel with the 1 UF capacitors to bypass the higher frequencies. The 1 UF capacitor will form a pole in series with the 10 UHy inductor of the power supply at approximately 50 KHz. At that frequency, the 1 UF capacitor would have a reactance of 3.16 ohm. We can adequately damp the pole by paralleling the 1 UF capacitor with approximately 3 ohms of resistance (Q=1). 3 ohms of resistance in each leg will provide a 6 ohm load to the power supply and result in 37.5 watts dissipated if connected directly to ground. However, the design of the ground fault detector (discussed in another note) cannot tolerate a direct connection to ground. A series blocking capacitor is required. The series blocking capacitor should be infinite to avoid degrading the filter performance. This is not practical; but as long as the series blocking capacitor is at least four times the primary capacitance, good performance will be obtained^{13, 14}. 50 UF is chosen because is available (same as filter output capacitor) and adequate.

Series Element -- We will use the 25 UHy air core coils mentioned previously for the series element. These coils have a measured shunt capacitance of 24 pf. The series reactance of the coils at 50 KHz is approximately 7.85 ohms inductive. The resistance is negligible compared to the reactance. However, for the final SPICE analysis, the series resistance of the coils at 10 KHz is approximately 19 milli-Ohms.

Output Capacitive Element -- The output capacitance is chosen to provide a breakpoint in the filter response that is well below our first frequency of interest and yet high enough to 1) stay above the power supply regulation loop cross over frequency and 2) be implemented with a minimum number of capacitors. Although other basic assumptions are being made at 50 KHz, our first frequency of interest is actually 10 KHz. Given the 40 dB per decade roll off of a 2nd order LC filter, we can place our breakpoint at 1 KHz and anticipate being 40 dB down at 10 kHz and more than 60 dB down at 50 KHz. Given the 10 UHy inductance of the supply and the 25 UHy inductance of the choke coil, we would require 720 UF of capacitance. However 500 UF would give us a breakpoint at 1.2 kHz and is obtainable in the high voltage low ESR package we require by paralleling 10, 50uF high voltage caps for each side of the filter.

The 500 UF capacitor will form a pole in series with the 10 UHy inductor of the supply and the 25 UHy inductor of the coil at 1.2 KHz. At that frequency, the reactance of the capacitor would be 0.265 ohm. We can adequately damp the pole (Q=1) with 0.250 ohms (four 1 Ohm resistors in parallel) resistance across the capacitance. This will minimize peaking to less than 1 db at 1.2 kHz. The 0.250 ohm resistance in each leg would provide a 0.500 ohm load to the power supply and would result in 450 watts dissipated from the filter output resistors if connected to ground during the worst case charging time when the power supply is delivering 15V. However, as described above, the ground fault detector cannot tolerate a direct connection to ground and a series blocking capacitor is required. 2200 UF is chosen because is available (non-polarized, high voltage, low inductance, oil-filled cap) and is at least four times the 500 UF capacitor it is helping to damp.

The output capacitance and resistance of the filter is in parallel with the load (bus and solenoid) to represent a low impedance to the filter series element. Thus they present a much lower resistance path for common mode noise to return to its source compared to the 7.85 ohms inductive reactance of the filter's series element and the 40 milli-Ohms + j0.754 - j39.8 of the load (calculated from the previously discussed models at 50 kHz). Thus, the common mode filter circuitry will initially appear lumped as follows:



Filter Design -- Differential Mode

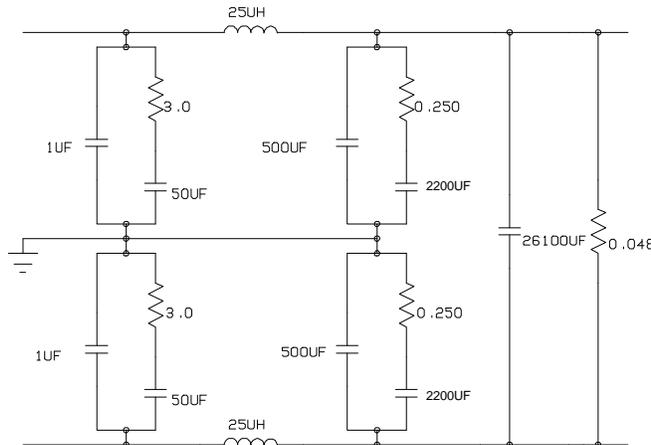
The differential and common mode filters are combined in one unit after being considered separately. The current path for differential noise is not to ground; but rather from one leg of the power supply to the other and passing through the filter and bus components in series.

The output impedance seen by the filter is dominated by the 48 milli-ohm dump resistor connected at all times across the input to the bus. The common mode filter just described also performs differential mode filtering. The 10 UHy of the supply in series with the two 25 UHy chokes form an LC filter with the two series connected 500 UF common mode capacitors (net capacitance = 250 UF). The break frequency of 1.70 KHz is too high to be of use against the 720 Hz ripple. However, the 48 milli-ohm dump resistor across the output of the filter works with the power supply and filter inductance to form a first order low pass LR filter. The filter breaks at 127 Hz and rolls off at 20 dB/decade. Thus it will be about 17 dB down at 720 Hz. The break frequency is safely beyond the power supply regulation loop frequency and the 17 dB attenuation at 720 Hz is significant.

The attenuation shall be increased to 40 dB/decade by adding sufficient capacitance across the output to form a second order LC filter. By matching the 48 milli-ohm dump resistance with 48 milli-ohms of capacitive reactance at the 127 Hz break frequency (26,108 UF), the filter will break at 127 Hz, be adequately damped ($Q=1$), and roll off at 40 dB/decade. By choosing 26,100 UF as an attainable number (nine 2900 UF capacitors in parallel) -- which is in parallel with the 250 UF from the series connected common mode 500 UF capacitors, the breakpoint becomes 166 Hz and the attenuation is greater than -30 dB at 720 Hz. -30 dB represents a ripple voltage reduction of approximately 30. The SPICE analysis of the complete filter and load model will provide the total expected reduction including any contribution from the bus.

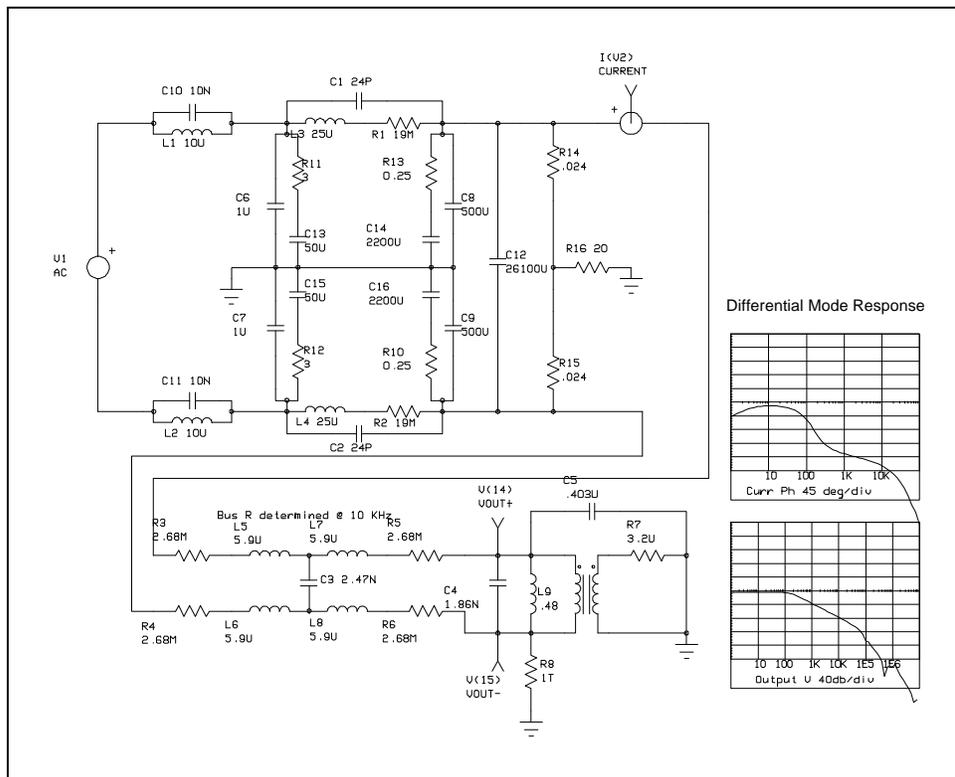
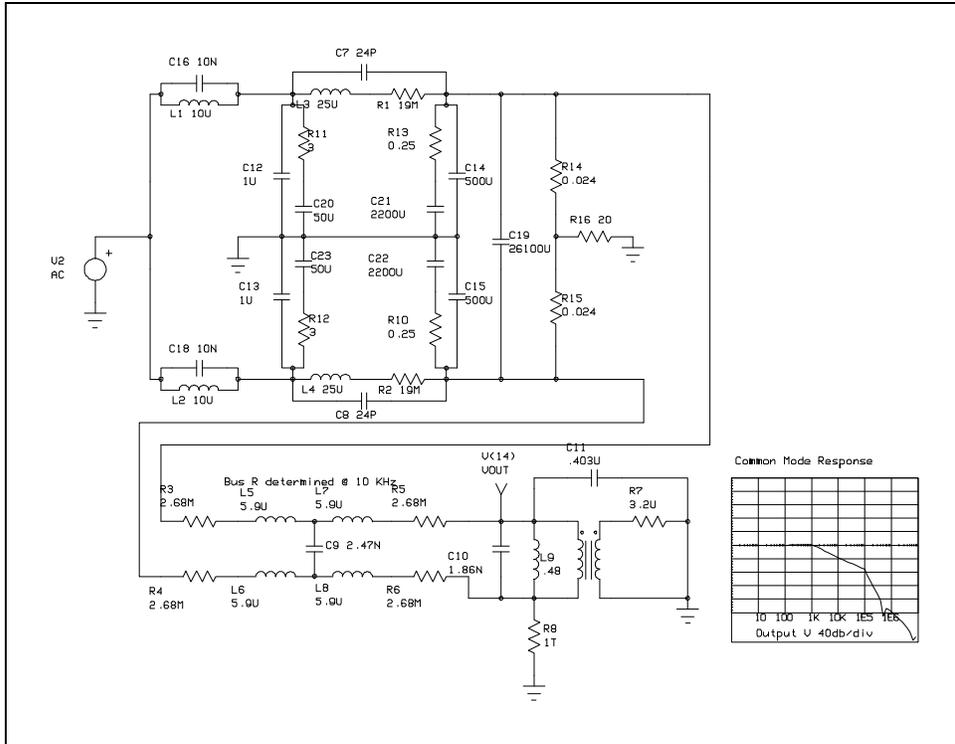
A quick review of the load model reveals that the dump resistor is dominant at differential noise frequencies. Thus the output impedance of the filter is much lower than the bus/solenoid combination and therefore should be relatively unaffected by them.

Thus, the entire common mode and differential mode filter appears as follows: Note this functional schematic does not show the high frequency capacitors nor does it show the multiple capacitors required to achieve the selected values. Please refer to the filter schematic for that information (Drawing #3823-111-ED-330052 sheet 8 of 14).



Performance Analysis:

The performance is analyzed using Berkeley SPICE. The complete equivalent circuits for common mode and differential mode analysis follow. Note that all series resistances are dominated by skin effect and are calculated at 10 KHz. SPICE does not dynamically change the resistance with frequency (although a more complex model could be presented that does). Thus, the results plotted are more valid at 10 KHz than at any other frequency. Results actually should be better than shown at the frequencies above 10 KHz.



Discussion of Analysis:

- The **common mode** performance is analyzed using SPICE by sweeping both sides of the circuit with a 1 VAC source from 1 Hz to 10 MHz and measuring the voltage to ground at the input to the solenoid. The results are presented in decibels ($20 \log v_o/v_i$) which is not completely valid in a system such as this with different source and load impedances. However, it provides an indication of the response slope and thus a relative figure of merit.

As shown on the Bode plot, the response is flat to approximately 1 kHz, then is attenuated at the rate of approximately 40 dB per decade with the slope becoming steeper as frequency increases. The response is attenuated approximately 40 dB at 10 kHz with a slope of approximately 40 dB/decade. Additional filtering is clearly provided by the 150' of DC bus. Caveats to be considered with these results are as previously discussed ie. parasitic inductances which result from the physical size of the components. Every effort must be made during construction to minimise stray inductance in the capacitors.

Most of the filtering is done directly by the filter with minimal contribution by the bus and solenoid model. The low voltage high current operation of the system has allowed the filter to be designed with very low impedances to tolerate wide variations in the source and load models.

More filtering can be provided by routing the ground return path with the DC bus and installing capacitors between the bus and the return path. Provisions will be made in the construction to add bus capacitance if necessary.

- The **differential mode** performance is analyzed using SPICE by sweeping the circuit differentially with a 1 VAC source from 1 Hz to 10 MHz and measuring the voltage ACROSS the input to the solenoid. The results are in decibels and the same disclaimer applies regarding unequal impedances.

As shown on the Bode plot, the response is flat to approximately 100 Hz, then is attenuated at 40 dB per decade initially with the slope increasing out beyond the range of the differential noise spectrum. The response is nearly 40 dB down at the 720 Hz primary ripple frequency. This attenuation is very likely to be valid given the extremely low parasitic capacitance (24 pF) of the filter coils.

The phase plot is included to show the phase shift of the current measured at the point where the power supply transducer is inserted. The filter provides less than 50 degrees of phase shift at 100 Hz. This should provide reasonable phase margin to the power supply regulation circuit which is understood to have less than unity gain well below 100 Hz. This information is of value to prevent regulation problems in the power supply due to the group delay introduced by the filter.

Construction:

- The filter is designed without regard for benefit of mutual inductance between the coils. This is because any orientation which optimizes for common mode induction would compromise differential mode and vice versa. Thus we wish to minimize mutual induction without requiring unusual techniques regarding coil orientation or separation. It will suffice to place the coils side by side with power connections on the same end for both coils. Slight advantage will result for common mode performance; but coupling should not be so tight as to cause noticeable degradation of the differential mode inductance.
- ALL capacitor and resistor components SHALL be connected with short twisted pair wires or wide flat conductors of minimum possible length to minimize inductance.
- Wide flat copper stock shall support the capacitors and provide the return path to the power supply frame.
- Not shown in this report; but shown on the schematic, is a free-wheeling diode across the output of the filter. This is in addition to the power supply's internal free-wheeling diode. The purpose of this diode is to shunt the solenoid discharge current around the filter during a slow dump; and to limit the reverse voltage across the filter output capacitors to safe values. Also shown on the schematic are bleeder resistors to discharge the filter capacitors once power is removed.

Final Note

This filter was originally designed and built without DC blocking capacitors in series with the damping resistors. Although the ramifications of connecting the damping resistors to ground were carefully evaluated from a power dissipation standpoint, the incompatibility of this approach to the ground fault detector design eluded the designer and all reviewers. The choice of $Q=1$ for damping was a compromise due to power dissipation considerations. Had the blocking capacitors been in the original design, $Q=.5$ would have been used and critical damping would have been achieved. The reason that blocking capacitors were not initially included in the design, was that they 1) they must withstand very high voltages in the event of a fast dump with particular ground faults, 2) they introduce additional components to reduce the MTBF, and 3) they provide somewhat of a reduction in performance due to added esr and inevitable parasitic inductance.. However, in retrospect, they should have been included in the original design.

¹Engineering note H960730A Rick Hance 7/30/96 "Power Supply Ripple Calculation"

²TM-1861 A.T. Visser date unknown "Energy losses in the D0 solenoid cryostat cause by current changes".

³TM-1690 A.T. Visser October 1990 "Description of a small commutation spike filter for D.C. Magnet power supplies"

⁴Engineering note H960625A Rick Hance 6/25/96 "CDF air core coil characteristics".

⁵Per Dan Wolff & Howard Pfeffer - Fermilab Accelerator Division.

⁶TM-1690 & follow-up Visser & Drennan October & November 1990 "Description of a small commutation spike filter for D.C. Magnet power supplies & P.S Filter-final design note" Also, discussions with W. Jaskierny & J. Lentz of the RD Power Supply Group.

⁷TM-1690 A.T. Visser October 1990 "Description of a small commutation spike filter for D.C. Magnet power supplies"

⁸TM-1690 A.T. Visser October 1990 "Description of a small commutation spike filter for D.C. Magnet power supplies"

⁹EN H950919A Hance 9/19/95 "Solenoid power bus characterization with 3 inch spacing".

¹⁰EN H951013A Hance 10/13/95 "Solenoid characterization (equivalent circuit)". Plus SPICE analysis.

¹¹EN H950919A Hance 9/19/95 "Solenoid power bus characterization with 3 inch spacing".

¹²GE 40L6101 Capacitor Impedance vs Frequency curve

¹³Design Considerations for a High-Current Low-Pass Filter - Walter F. Praeg - Argonne Natl. Lab. - from Power Conversion Intl Feb 1984

¹⁴Minimizing Input Filter Requirements In Military Power Supply Design - H. Dean Venable - from SATECH '86 -Oct 28-30 1986